



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	26
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 4x8b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc933fdh-529

2.2 Additional features

- A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz. This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- Serial flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Serial flash In-System Programming (ISP) allows coding while the device is mounted in the end application.
- In-Application Programming (IAP) of the flash code memory. This allows changing the code in a running application.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog prescaler is selectable from eight values.
- Low voltage reset (brownout detect) allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μ A (total power-down with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets. A software reset function is also available.
- Configurable on-chip oscillator with frequency range options selected by user programmed flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz.
- Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- Port 'input pattern match' detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- LED drive capability (20 mA) on all port pins. A maximum limit is specified for the entire chip.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC933/934/935/936 when internal reset option is selected.
- Four interrupt priority levels.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Schmitt trigger port inputs.
- Second data pointer.
- Emulation support.

6. Pinning information

6.1 Pinning

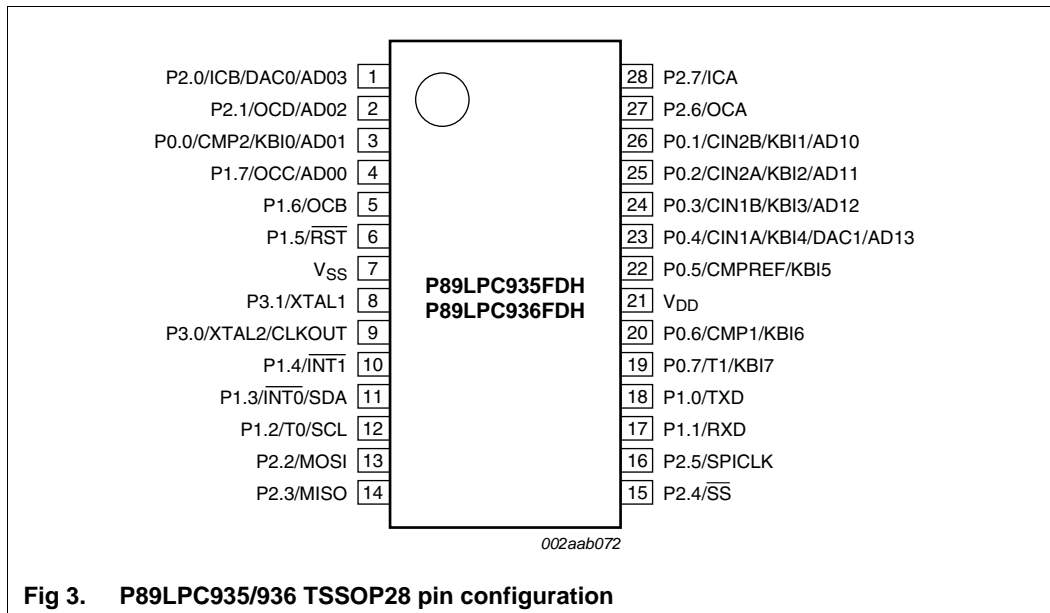
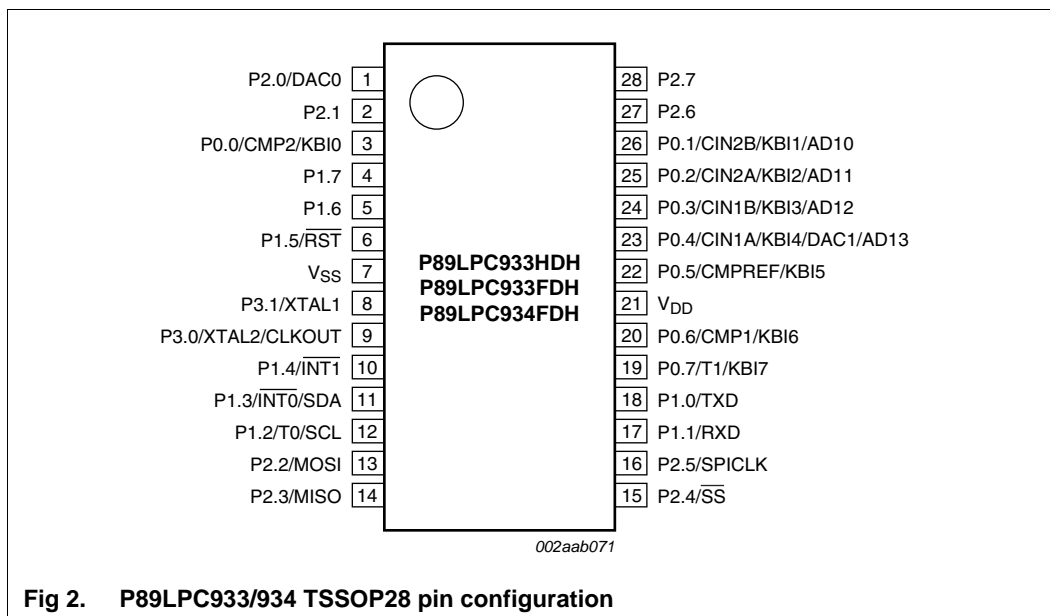


Table 4. Pin description ...continued

Symbol	Pin		Type	Description
	TSSOP28, PLCC28	HVQFN28		
P2.0 to P2.7			I/O	<p>Port 2: Port 2 is an 8-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.13.1 “Port configurations” and Table 11 “Static characteristics” for details.</p> <p>All pins have Schmitt trigger inputs.</p> <p>Port 2 also provides various special functions as described below:</p>
P2.0/ICB/ DAC0/AD03	1	25	I/O	P2.0 — Port 2 bit 0.
			I	ICB — Input Capture B. (P89LPC935/936)
			I	DAC0 — Digital-to-analog converter output.
			I	AD03 — ADC0 channel 3 analog input. (P89LPC935/936)
P2.1/OCD/ AD02	2	26	I/O	P2.1 — Port 2 bit 1.
			O	OCD — Output Compare D. (P89LPC935/936)
			I	AD02 — ADC0 channel 2 analog input. (P89LPC935/936)
P2.2/MOSI	13	9	I/O	P2.2 — Port 2 bit 2.
			I/O	MOSI — SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.3/MISO	14	10	I/O	P2.3 — Port 2 bit 3.
			I/O	MISO — When configured as master, this pin is input, when configured as slave, this pin is output.
P2.4/ $\overline{\text{SS}}$	15	11	I/O	P2.4 — Port 2 bit 4.
			I	$\overline{\text{SS}}$ — SPI Slave select.
P2.5/ SPICLK	16	12	I/O	P2.5 — Port 2 bit 5.
			I/O	SPICLK — SPI clock. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.6/OCA	27	23	I/O	P2.6 — Port 2 bit 6.
			O	OCA — Output Compare A. (P89LPC935/936)
P2.7/ICA	28	24	I/O	P2.7 — Port 2 bit 7.
			I	ICA — Input Capture A. (P89LPC935/936)

Table 4. Pin description ...continued

Symbol	Pin		Type	Description
	TSSOP28, PLCC28	HVQFN28		
P3.0 to P3.1			I/O	<p>Port 3: Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.13.1 “Port configurations” and Table 11 “Static characteristics” for details.</p> <p>All pins have Schmitt trigger inputs.</p> <p>Port 3 also provides various special functions as described below:</p>
P3.0/XTAL2/ CLKOUT	9	5	I/O	P3.0 — Port 3 bit 0.
			O	XTAL2 — Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration).
			O	CLKOUT — CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the RTC/system timer.
P3.1/XTAL1	8	4	I/O	P3.1 — Port 3 bit 1.
			I	XTAL1 — Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, and if XTAL1/XTAL2 are not used to generate the clock for the RTC/system timer.
V _{SS}	7	3	I	Ground: 0 V reference.
V _{DD}	21	17	I	Power supply: This is the power supply voltage for normal operation as well as Idle and Power-down modes.

[1] Input/output for P1.0 to P1.4, P1.6, P1.7. Input for P1.5.

7. Logic symbols

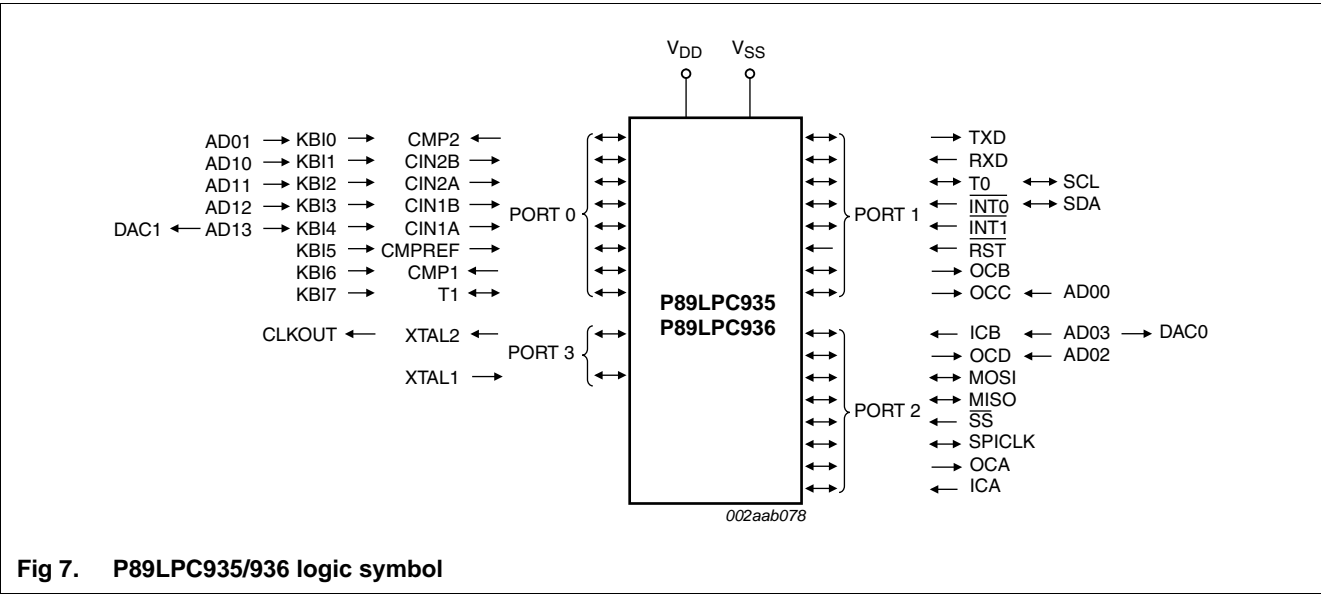
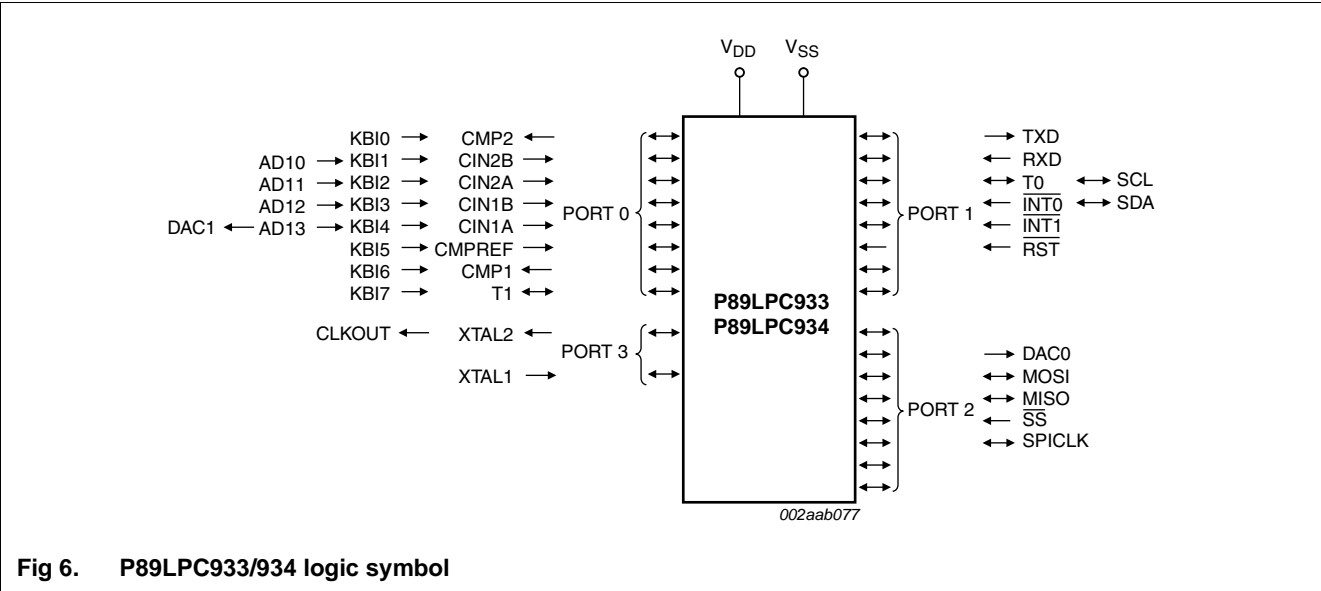


Table 5. Special function registers - P89LPC933/934 ...continued

* indicates SFRs that are bit addressable.

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB								Hex	Binary
FMADRL	Program flash address low	E6H									00	0000 0000
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)	E4H	FMCMD. 7	FMCMD. 6	FMCMD. 5	FMCMD. 4	FMCMD. 3	FMCMD. 2	FMCMD. 1	FMCMD. 0		
FMDATA	Program flash data	E5H									00	0000 0000
I2ADR	I ² C slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	0000 0000
	Bit address		DF	DE	DD	DC	DB	DA	D9	D8		
I2CON*	I ² C control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x000 00x0
I2DAT	I ² C data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH									00	0000 0000
I2SCLL	Serial clock generator/SCL duty cycle register low	DCH									00	0000 0000
I2STAT	I ² C status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	1111 1000
ICRAH	Input capture A register high	ABH									00	0000 0000
ICRAL	Input capture A register low	AAH									00	0000 0000
ICRBH	Input capture B register high	AFH									00	0000 0000
ICRBL	Input capture B register low	AEH									00	0000 0000
	Bit address		AF	AE	AD	AC	AB	AA	A9	A8		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0	EX0	00	0000 0000
	Bit address		EF	EE	ED	EC	EB	EA	E9	E8		
IEN1*	Interrupt enable 1	E8H	EAD	EST	-	-	ESPI	EC	EKBI	EI2C	00 ^[3]	00x0 0000
	Bit address		BF	BE	BD	BC	BB	BA	B9	B8		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0	PX0	00 ^[3]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRT H	PBOH	PSH/PSRH	PT1H	PX1H	PT0H	PX0H	00 ^[3]	x000 0000
	Bit address		FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	PAD	PST	-	-	PSPI	PC	PKBI	PI2C	00 ^[3]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	PADH	PSTH	-	-	PSPIH	PCH	PKBIH	PI2CH	00 ^[3]	00x0 0000

Table 6. Special function registers - P89LPC935/936 ...continued

* indicates SFRs that are bit addressable.

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB								Hex	Binary
CCCRB	Capture compare B control register	EBH	ICECB2	ICECB1	ICECB0	ICESB	ICNFB	FCOB	OCMB1	OCMB0	00	0000 0000
CCCRC	Capture compare C control register	ECH	-	-	-	-	-	FCOC	OCMC1	OCMC0	00	xxxx x000
CCCRD	Capture compare D control register	EDH	-	-	-	-	-	FCOD	OCMD1	OCMD0	00	xxxx x000
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	OE1	CO1	CMF1	00 ^[3]	xx00 0000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00 ^[3]	xx00 0000
DEECON	Data EEPROM control register	F1H	EEIF	HVERR	ECTL1	ECTL0	-	-	-	EADR8	0E	0000 1110
DEEDAT	Data EEPROM data register	F2H									00	0000 0000
DEEADR	Data EEPROM address register	F3H									00	0000 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H									00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)	E4H	FMCMD. 7	FMCMD. 6	FMCMD. 5	FMCMD. 4	FMCMD. 3	FMCMD. 2	FMCMD. 1	FMCMD. 0		
FMDATA	Program flash data	E5H									00	0000 0000
I2ADR	I ² C slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	0000 0000
	Bit address		DF	DE	DD	DC	DB	DA	D9	D8		
I2CON*	I ² C control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x000 00x0
I2DAT	I ² C data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH									00	0000 0000

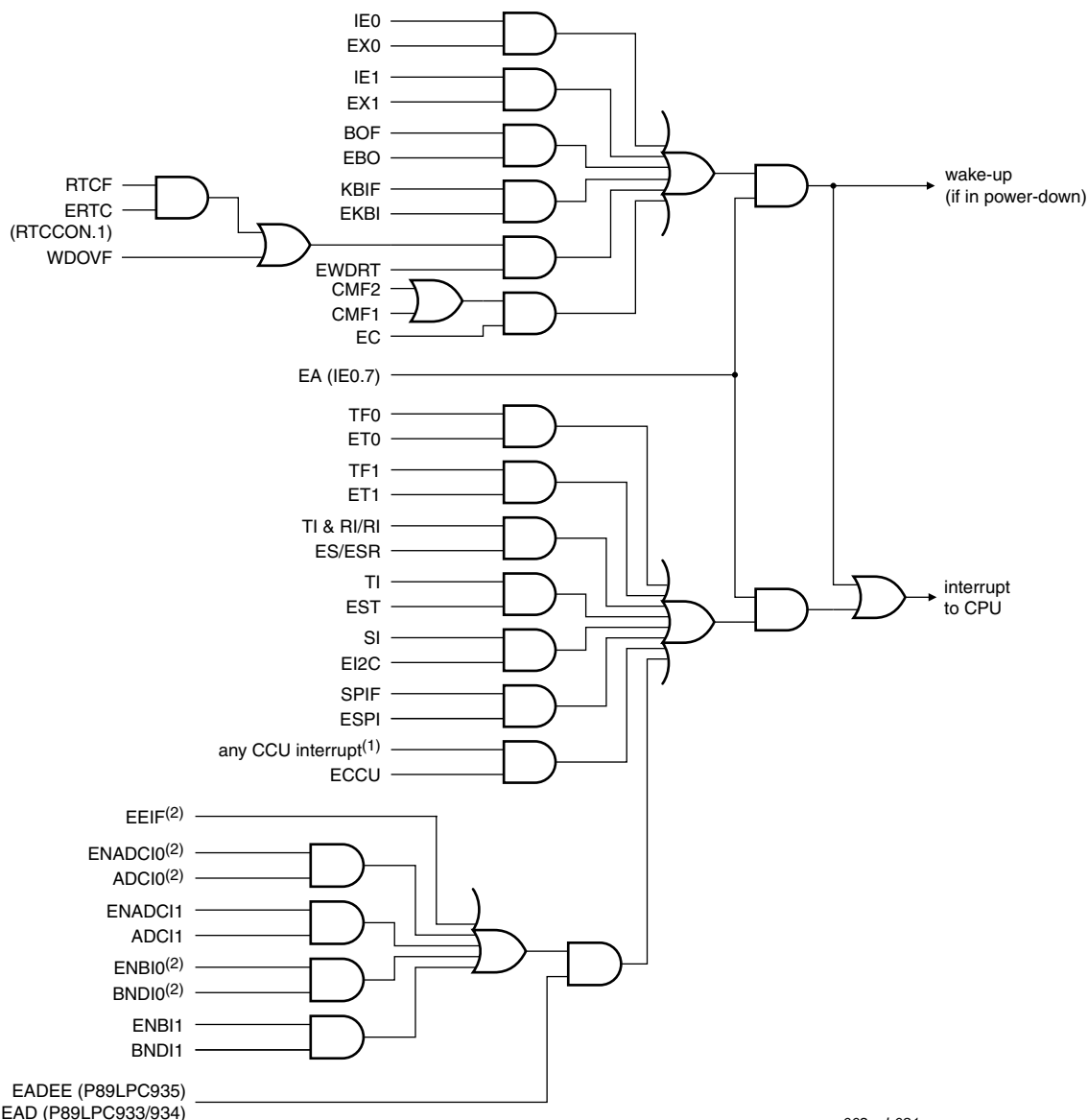
Table 6. Special function registers - P89LPC935/936 ...continued
** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB								Hex	Binary
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX		[4]
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60 ^{[3][5]}	011x xx00
RTCH	Real-time clock register high	D2H									00 ^[5]	0000 0000
RTCL	Real-time clock register low	D3H									00 ^[5]	0000 0000
SADDR	Serial port address register	A9H									00	0000 0000
SADEN	Serial port address enable	B9H									00	0000 0000
SBUF	Serial Port data buffer register	99H									xx	xxxx xxxx
Bit address			9F	9E	9D	9C	9B	9A	99	98		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	0000 0000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	0000 0100
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xx xxxx
SPDAT	SPI data register	E3H									00	0000 0000
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0 xxx0
Bit address			8F	8E	8D	8C	8B	8A	89	88		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	0000 0000
TCR20*	CCU control register 0	C8H	PLEEN	HLTRN	HLTEN	ALTCd	ALTAB	TDIR2	TMOD21	TMOD20	00	0000 0000
TCR21	CCU control register 1	F9H	TCOU2	-	-	-	PLLDV.3	PLLDV.2	PLLDV.1	PLLDV.0	00	0xxx 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TH2	CCU timer high	CDH									00	0000 0000
TICR2	CCU interrupt control register	C9H	TOIE2	TOCIE2 D	TOCIE2 C	TOCIE2B	TOCIE2A	-	TICIE2B	TICIE2A	00	0000 0x00
TIFR2	CCU interrupt flag register	E9H	TOIF2	TOCF2D	TOCF2C	TOCF2B	TOCF2A	-	TICF2B	TICF2A	00	0000 0x00
TISE2	CCU interrupt status encode register	DEH	-	-	-	-	-	ENCINT. 2	ENCINT. 1	ENCINT. 0	00	xxxx x000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000

These external interrupts can be programmed to be level-triggered or edge-triggered by setting or clearing bit IT1 or IT0 in register TCON.

In edge-triggered mode, if successive samples of the $\overline{\text{INTn}}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request flag IEn in TCON is set, causing an interrupt request.

If an external interrupt is enabled when the P89LPC933/934/935/936 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to [Section 8.15 "Power reduction modes"](#) for details.



(1) See [Section 8.19 "CCU \(P89LPC935/936\)"](#)

(2) P89LPC935/936

Fig 9. Interrupt sources, interrupt enables, and power-down wake-up sources

8.14.1 Brownout detection

The brownout detect function determines if the power supply voltage drops below a certain level. The default operation is for a brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt.

Brownout detection may be enabled or disabled in software.

If brownout detection is enabled the brownout condition occurs when V_{DD} falls below the brownout trip voltage, V_{bo} (see [Table 11 "Static characteristics"](#)), and is negated when V_{DD} rises above V_{bo} . If the P89LPC933/934/935/936 device is to operate with a power supply that can be below 2.7 V, BOE should be left in the unprogrammed state so that the device can operate at 2.4 V, otherwise continuous brownout reset may prevent the device from operating.

For correct activation of brownout detect, the V_{DD} rise and fall times must be observed. Please see [Table 11 "Static characteristics"](#) for specifications.

8.14.2 Power-on detection

The power-on detect has a function similar to the brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

8.15 Power reduction modes

The P89LPC933/934/935/936 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

8.15.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

8.15.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC933/934/935/936 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the RAM keep-alive voltage V_{RAM} . This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{DDR} , therefore it is highly recommended to wake-up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during power-down. These include: brownout detect, watchdog timer, Comparators (note that Comparators can be powered-down separately), and RTC/system timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock and the RTC is enabled.

8.19.9 CCU interrupts

There are seven interrupt sources on the CCU which share a common interrupt vector.

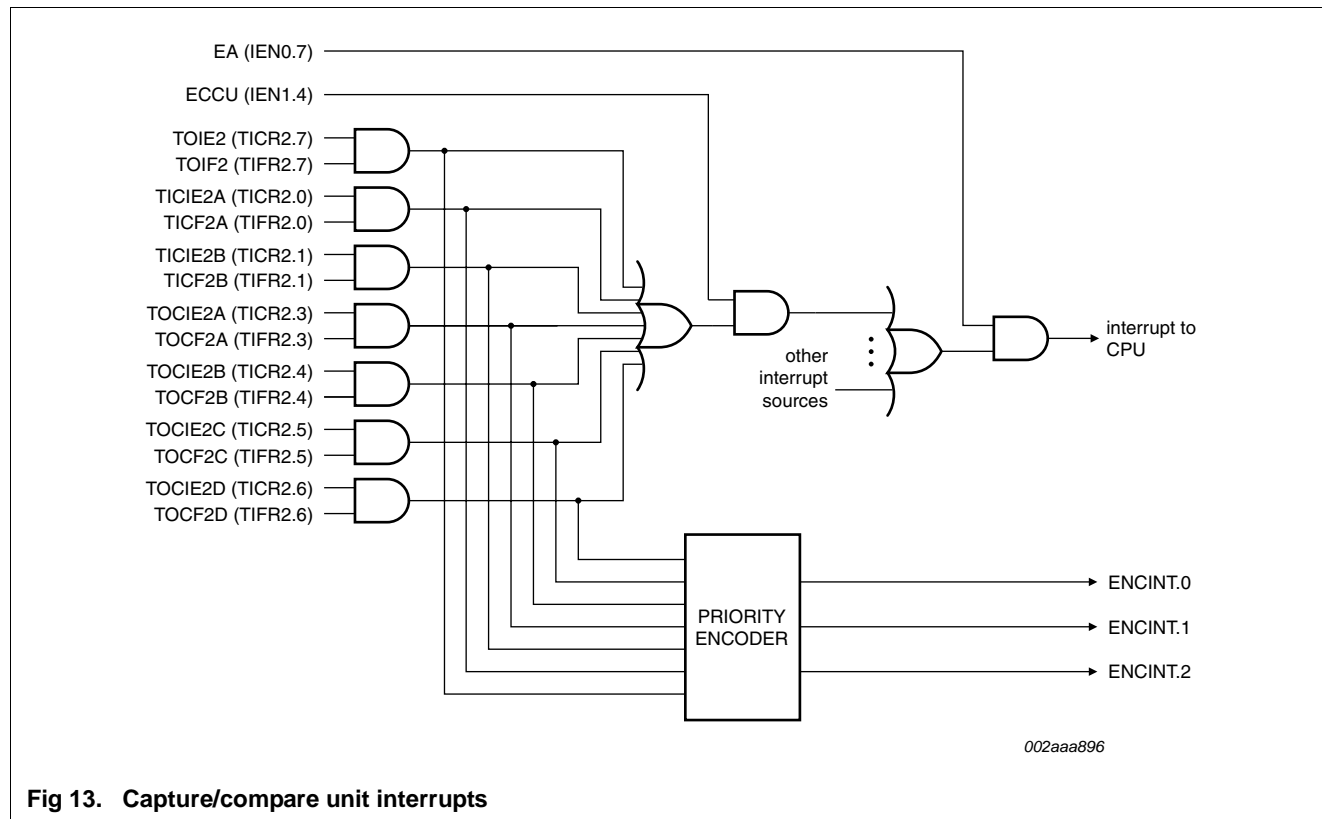


Fig 13. Capture/compare unit interrupts

8.20 UART

The P89LPC933/934/935/936 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC933/934/935/936 does include an independent baud rate generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent baud rate generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in four modes: shift register, 8-bit UART, 9-bit UART, and CPU $\text{clock}/_{32}$ or CPU $\text{clock}/_{16}$.

8.20.1 Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $1/_{16}$ of the CPU clock frequency.

8.20.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device and force the device into ISP mode.

8.20.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = 0).

8.20.9 Transmit interrupts with double buffering enabled (modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the Tx interrupt is generated when the double buffer is ready to receive new data.

8.20.10 The 9th bit (bit 8) in double buffering (modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the Tx interrupt.

If double buffering is enabled, TB8 **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

8.22 SPI

The P89LPC933/934/935/936 provides another high-speed serial communication interface—the SPI interface. SPI is a full-duplex, high-speed, synchronous communication bus with two operation modes: Master mode and Slave mode. Up to 3 Mbit/s can be supported in Master mode or up to 2 Mbit/s in Slave mode. It has a Transfer Completion Flag and Write Collision Flag Protection.

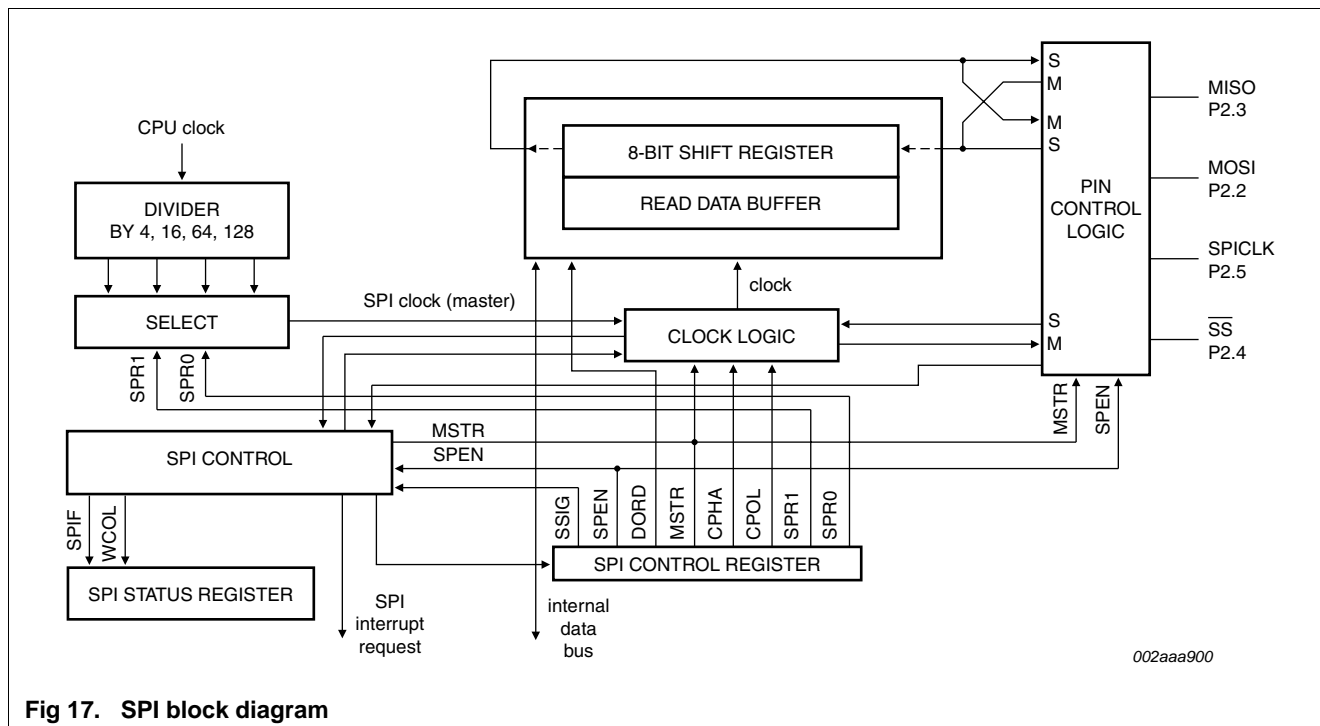


Fig 17. SPI block diagram

The SPI interface has four pins: SPICLK, MOSI, MISO and \overline{SS} :

- SPICLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on MOSI (Master Out Slave In) pin and flows from slave to master on MISO (Master In Slave Out) pin. The SPICLK signal is output in the master mode and is input in the slave mode. If the SPI system is disabled, i.e., SPEN (SPCTL.6) = 0 (reset value), these pins are configured for port functions.
- \overline{SS} is the optional slave select pin. In a typical configuration, an SPI master asserts one of its port pins to select one SPI device as the current slave. An SPI slave device uses its \overline{SS} pin to determine whether it is selected.

Typical connections are shown in [Figure 18](#) through [Figure 20](#).

8.28.3 Flash organization

The program memory consists of eight 2 kB sectors on the P89LPC936 device, eight 1 kB sectors on the P89LPC934/935 devices, and four 1 kB sectors on the P89LPC933 device. Each sector can be further divided into 64-byte pages. In addition to sector erase, page erase, and byte erase, a 64-byte page register is included which allows from 1 to 64 bytes of a given page to be programmed at the same time, substantially reducing overall programming time.

8.28.4 Using flash as data storage

The flash code memory array of this device supports individual byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

8.28.5 Flash programming and erasing

Four different methods of erasing or programming of the flash are available. The flash may be programmed or erased in the end-user application (IAP) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock - serial data interface. As shipped from the factory, the upper 512 bytes of user code space contains a serial ISP routine allowing the device to be programmed in circuit through the serial port. The flash may also be programmed or erased using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead, this device provides a 32-bit CRC result on either a sector or the entire user code space.

8.28.6 In-circuit programming

ICP is performed without removing the microcontroller from the system. The ICP facility consists of internal hardware resources to facilitate remote programming of the P89LPC933/934/935/936 through a two-wire serial interface. The Philips ICP facility has made ICP in an embedded application—using commercially available programmers—possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the P89LPC933/934/935/936 *User manual*.

8.28.7 In-application programming

IAP is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The Philips IAP has made IAP in an embedded application possible without additional components. Two methods are available to accomplish IAP. A set of predefined IAP functions are provided in a boot ROM and can be called through a common interface, PGM_MTP. Several IAP calls are available for use by an application program to permit selective erasing and programming of flash sectors, pages, security bits, configuration bytes, and device ID. These functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FF03H. The boot ROM occupies the program memory space at the top of the address space from FF00H to FFEFH, thereby not conflicting with the user program memory space.

11. Static characteristics

Table 11. Static characteristics

$V_{DD} = 2.4\text{ V}$ to 3.6 V unless otherwise specified.

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ for industrial, $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ for extended, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$I_{DD(oper)}$	operating supply current	$V_{DD} = 3.6\text{ V}$; $f_{osc} = 12\text{ MHz}$	[2] -	11	18	mA
		$V_{DD} = 3.6\text{ V}$; $f_{osc} = 18\text{ MHz}$	[2] -	14	23	mA
$I_{DD(idle)}$	Idle mode supply current	$V_{DD} = 3.6\text{ V}$; $f_{osc} = 12\text{ MHz}$	[2] -	3.25	5	mA
		$V_{DD} = 3.6\text{ V}$; $f_{osc} = 18\text{ MHz}$	[2] -	5	7	mA
$I_{DD(pd)}$	Power-down mode supply current	$V_{DD} = 3.6\text{ V}$; voltage comparators powered down	[2] -	55	80	μA
$I_{DD(tpd)}$	total Power-down mode supply current	all devices except P89LPC933HDH; $V_{DD} = 3.6\text{ V}$	[3] -	1	5	μA
		P89LPC933HDH only; $V_{DD} = 3.6\text{ V}$	[3] -	-	25	μA
$(dV/dt)_r$	rise rate	of V_{DD}	-	-	2	$\text{mV}/\mu\text{s}$
$(dV/dt)_f$	fall rate	of V_{DD}	-	-	50	$\text{mV}/\mu\text{s}$
V_{POR}	power-on reset voltage		-	-	0.5	V
V_{DDR}	data retention supply voltage		1.5	-	-	V
$V_{th(HL)}$	HIGH-LOW threshold voltage	except SCL, SDA	$0.22V_{DD}$	$0.4V_{DD}$	-	V
V_{IL}	LOW-level input voltage	SCL, SDA only	-0.5	-	$0.3V_{DD}$	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	except SCL, SDA	-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{IH}	HIGH-level input voltage	SCL, SDA only	$0.7V_{DD}$	-	5.5	V
V_{hys}	hysteresis voltage	port 1	-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage	$I_{OL} = 20\text{ mA}$; $V_{DD} = 2.4\text{ V}$ to 3.6 V all ports, all modes except high-Z	[4] -	0.6	1.0	V
		$I_{OL} = 3.2\text{ mA}$; $V_{DD} = 2.4\text{ V}$ to 3.6 V all ports, all modes except high-Z	-	0.2	0.3	V
V_{OH}	HIGH-level output voltage	$I_{OH} = -20\text{ }\mu\text{A}$; $V_{DD} = 2.4\text{ V}$ to 3.6 V ; all ports, quasi-bidirectional mode	$V_{DD} - 0.3$	$V_{DD} - 0.2$	-	V
		$I_{OH} = -3.2\text{ mA}$; $V_{DD} = 2.4\text{ V}$ to 3.6 V ; all ports, push-pull mode	$V_{DD} - 0.7$	$V_{DD} - 0.4$	-	V
		$I_{OH} = -10\text{ mA}$; $V_{DD} = 3.6\text{ V}$; all ports, push-pull mode	-	3.2	-	V
V_{xtal}	crystal voltage	on XTAL1, XTAL2 pins; with respect to V_{SS}	-0.5	-	+4.0	V
V_n	voltage on any other pin	except XTAL1, XTAL2, V_{DD} ; with respect to V_{SS}	[5] -0.5	-	+5.5	V
C_{iss}	input capacitance		[6] -	-	15	pF

Table 11. Static characteristics ...continued $V_{DD} = 2.4\text{ V}$ to 3.6 V unless otherwise specified. $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ for industrial, $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ for extended, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
I_{IL}	LOW-level input current	$V_I = 0.4\text{ V}$	[7] -	-	-80	μA
I_{LI}	input leakage current	$V_I = V_{IL}, V_{IH}$ or $V_{th(HL)}$	[8] -	-	± 10	μA
I_{THL}	HIGH-LOW transition current	all ports; $V_I = 1.5\text{ V}$ at $V_{DD} = 3.6\text{ V}$	[9] -30	-	-450	μA
$R_{RST_N(int)}$	internal pull-up resistance on pin \overline{RST}		10	-	30	$\text{k}\Omega$
V_{bo}	brownout trip voltage	$2.4\text{ V} < V_{DD} < 3.6\text{ V}$; with $BOV = 1$, $BOPD = 0$	2.40	-	2.70	V
$V_{ref(bg)}$	band gap reference voltage		1.11	1.23	1.34	V
TC_{bg}	band gap temperature coefficient		-	10	20	$\text{ppm}/^{\circ}\text{C}$

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$, and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, real-time clock, and watchdog timer.

[3] The $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.

[4] See Section 10 "Limiting values" for steady state (non-transient) limits on I_{OL} or I_{OH} . If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.

[5] This specification can be applied to pins which have A/D input or analog comparator input functions when the pin is not being used for those analog functions. When the pin is being used as an analog input pin, the maximum voltage on the pin must be limited to 4.0 V with respect to V_{SS} .

[6] Pin capacitance is characterized but not tested.

[7] Measured with port in quasi-bidirectional mode.

[8] Measured with port in high-impedance mode.

[9] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

11.1 I_{OH} as a function of V_{OH}

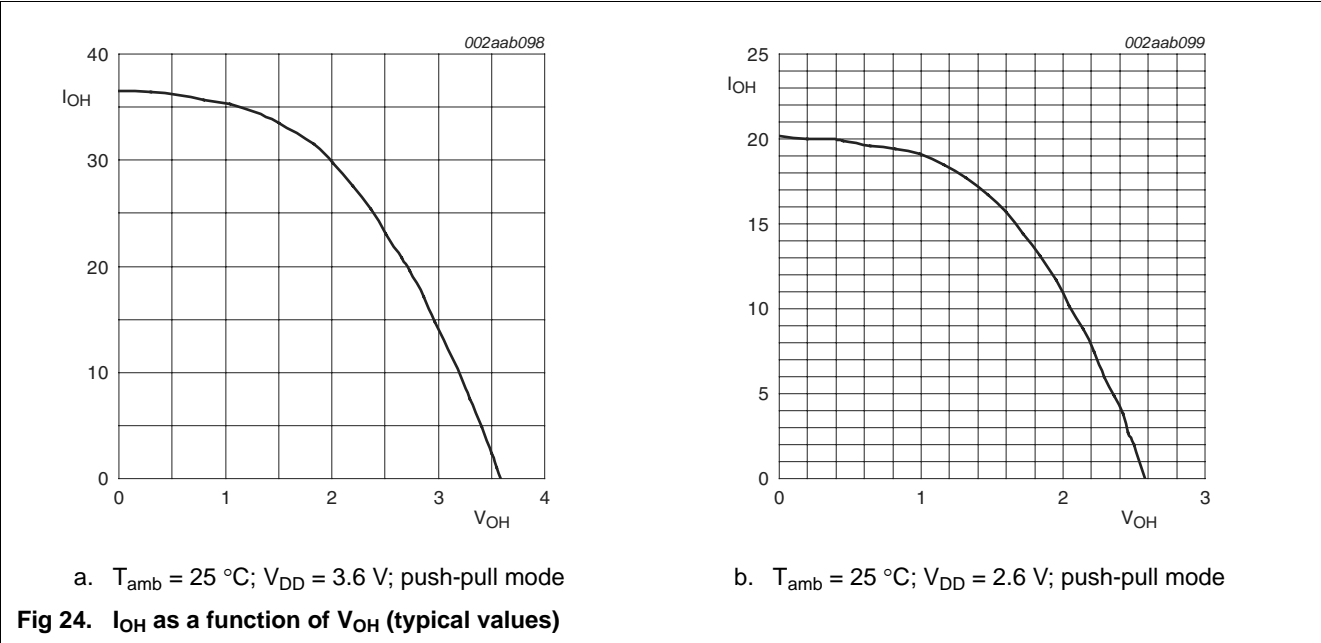
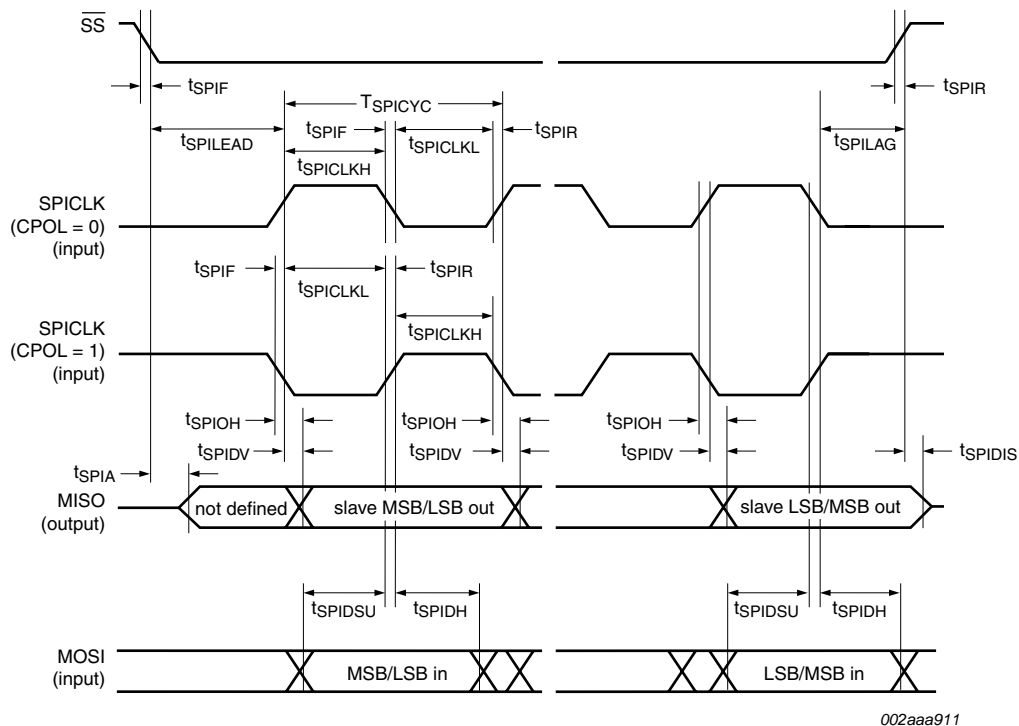


Table 13. Dynamic characteristics (18 MHz) $V_{DD} = 3.0\text{ V to }3.6\text{ V unless otherwise specified.}$ $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C for industrial, }-40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C for extended, unless otherwise specified. [1][2]}$

Symbol	Parameter	Conditions	Variable clock		f _{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
f _{osc(RC)}	internal RC oscillator frequency		7.189	7.557	7.189	7.557	MHz
f _{osc(WD)}	internal watchdog oscillator frequency		320	520	320	520	kHz
f _{osc}	oscillator frequency		0	18	-	-	MHz
T _{cy(CLK)}	clock cycle	see Figure 27	55	-	-	-	ns
f _{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t _{gr}	glitch rejection time	P1.5/ \overline{RST} pin	-	50	-	50	ns
		any pin except P1.5/ \overline{RST}	-	15	-	15	ns
t _{sa}	signal acceptance time	P1.5/ \overline{RST} pin	125	-	125	-	ns
		any pin except P1.5/ \overline{RST}	50	-	50	-	ns
External clock							
t _{CHCX}	clock HIGH time	see Figure 27	22	T _{cy(CLK)} – t _{CLCX}	22	-	ns
t _{CLCX}	clock LOW time	see Figure 27	22	T _{cy(CLK)} – t _{CHCX}	22	-	ns
t _{CLCH}	clock rise time	see Figure 27	-	5	-	5	ns
t _{CHCL}	clock fall time	see Figure 27	-	5	-	5	ns
Shift register (UART mode 0)							
T _{XLXL}	serial port clock cycle time	see Figure 25	16T _{cy(CLK)}	-	888	-	ns
t _{QVXH}	output data set-up to clock rising edge time	see Figure 25	13T _{cy(CLK)}	-	722	-	ns
t _{XHQX}	output data hold after clock rising edge time	see Figure 25	-	T _{cy(CLK)} + 20	-	75	ns
t _{XHDX}	input data hold after clock rising edge time	see Figure 25	-	0	-	0	ns
t _{XHDV}	input data valid to clock rising edge time	see Figure 25	150	-	150	-	ns
SPI interface							
f _{SPI}	SPI operating frequency						
	slave		0	CCLK _{/6}	0	3.0	MHz
	master		-	CCLK _{/4}	-	4.5	MHz
T _{SPICYC}	SPI cycle time		see Figure 26 , 28 , 29 , 30				
	slave		⁶ / _{CCLK}	-	333	-	ns
	master		⁴ / _{CCLK}	-	222	-	ns
t _{SPILEAD}	SPI enable lead time		see Figure 29 , 30				
	slave		250	-	250	-	ns
t _{SPILAG}	SPI enable lag time		see Figure 29 , 30				
	slave		250	-	250	-	ns



002aaa911

Fig 30. SPI slave timing (CPHA = 1)

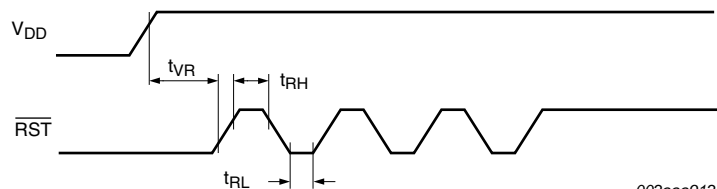
12.2 ISP entry mode

Table 14. Dynamic characteristics, ISP entry mode

$V_{DD} = 2.4\text{ V to }3.6\text{ V}$, unless otherwise specified.

$T_{amb} = -40\text{ °C to }+85\text{ °C}$ for industrial, $-40\text{ °C to }+125\text{ °C}$ for extended, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VR}	$\overline{\text{RST}}$ delay from V_{DD} active time		50	-	-	μs
t_{RH}	$\overline{\text{RST}}$ HIGH time		1	-	32	μs
t_{RL}	$\overline{\text{RST}}$ LOW time		1	-	-	μs

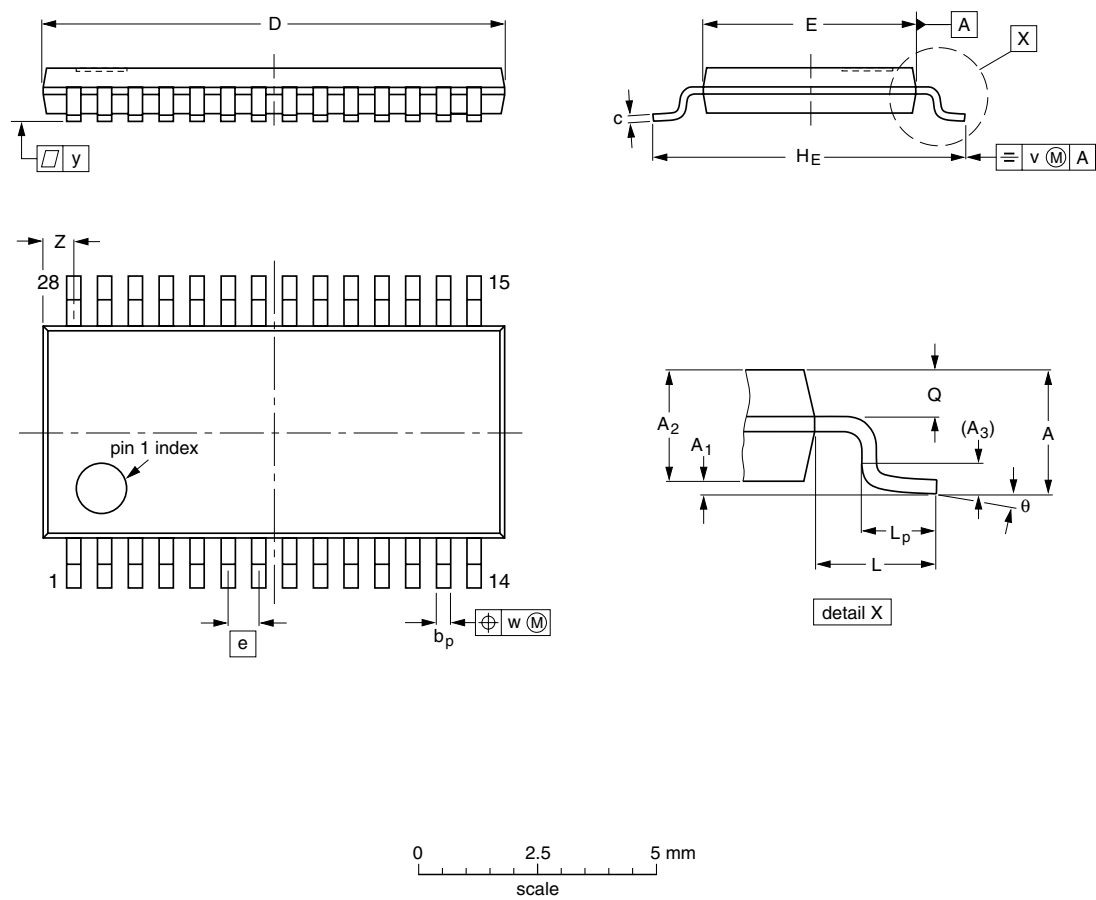


002aaa912

Fig 31. ISP entry timing

TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm

SOT361-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	9.8 9.6	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.8 0.5	8° 0°

- Notes
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

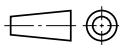
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT361-1		MO-153				-99-12-27- 03-02-19

Fig 33. Package outline SOT361-1 (TSSOP28)