



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	12MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x8b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc935fdh-518

6.2 Pin description**Table 4. Pin description**

Symbol	Pin		Type	Description
	TSSOP28, PLCC28	HVQFN28		
P0.0 to P0.7			I/O	<p>Port 0: Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.13.1 “Port configurations” and Table 11 “Static characteristics” for details.</p> <p>The Keypad Interrupt feature operates with Port 0 pins.</p> <p>All pins have Schmitt trigger inputs.</p> <p>Port 0 also provides various special functions as described below:</p>
P0.0/CMP2/ KBI0/AD01	3	27	I/O	P0.0 — Port 0 bit 0.
			O	CMP2 — Comparator 2 output.
			I	KBI0 — Keyboard input 0.
			I	AD01 — ADC0 channel 1 analog input. (P89LPC935/936)
P0.1/CIN2B/ KBI1/AD10	26	22	I/O	P0.1 — Port 0 bit 1.
			I	CIN2B — Comparator 2 positive input B.
			I	KBI1 — Keyboard input 1.
			I	AD10 — ADC1 channel 0 analog input.
P0.2/CIN2A/ KBI2/AD11	25	21	I/O	P0.2 — Port 0 bit 2.
			I	CIN2A — Comparator 2 positive input A.
			I	KBI2 — Keyboard input 2.
			I	AD11 — ADC1 channel 1 analog input.
P0.3/CIN1B/ KBI3/AD12	24	20	I/O	P0.3 — Port 0 bit 3.
			I	CIN1B — Comparator 1 positive input B.
			I	KBI3 — Keyboard input 3.
			I	AD12 — ADC1 channel 2 analog input.
P0.4/CIN1A/ KBI4/DAC1/ AD13	23	19	I/O	P0.4 — Port 0 bit 4.
			I	CIN1A — Comparator 1 positive input A.
			I	KBI4 — Keyboard input 4.
			O	DAC1 — Digital-to-analog converter output 1.
			I	AD13 — ADC1 channel 3 analog input.
P0.5/ CMPREF/ KBI5	22	18	I/O	P0.5 — Port 0 bit 5.
			I	CMPREF — Comparator reference (negative) input.
			I	KBI5 — Keyboard input 5.
P0.6/CMP1/ KBI6	20	16	I/O	P0.6 — Port 0 bit 6.
			O	CMP1 — Comparator 1 output.
			I	KBI6 — Keyboard input 6.
P0.7/T1/ KBI7	19	15	I/O	P0.7 — Port 0 bit 7.
			I/O	T1 — Timer/counter 1 external count input or overflow output.
			I	KBI7 — Keyboard input 7.

8. Functional description

Remark: Please refer to the P89LPC933/934/935/936 *User manual* for a more detailed functional description.

8.1 Special function registers

Remark: SFR accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', logic 0 or logic 1 can **only** be written and read as follows:
 - '-' Unless otherwise specified, **must** be written with logic 0, but can return any value when read (even if it was written with logic 0). It is a reserved bit and may be used in future derivatives.
 - Logic 0 **must** be written with logic 0, and will return a logic 0 when read.
 - Logic 1 **must** be written with logic 1, and will return a logic 1 when read.

Table 5. Special function registers - P89LPC933/934

* indicates SFRs that are bit addressable.

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB				LSB				Hex	Binary
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	0000 0000
ADCON0	A/D control register 0	8EH	-	-	-	-	-	ENADC0	-	-	00	0000 0000
ADCON1	A/D control register 1	97H	ENBI1	ENADCI 1	TMM1	EDGE1	ADCI1	ENADC1	ADCS11	ADCS10	00	0000 0000
ADINS	A/D input select	A3H	ADI13	ADI12	ADI11	ADI10	-	-	-	-	00	0000 0000
ADMODA	A/D mode register A	C0H	BNDI1	BURST1	SCC1	SCAN1	-	-	-	-	00	0000 0000
ADMODB	A/D mode register B	A1H	CLK2	CLK1	CLK0	-	ENDAC1	ENDAC0	BSA1	-	00	000x 0000
AD0DAT3	A/D_0 data register 3	F4H									00	0000 0000
AD1BH	A/D_1 boundary high register	C4H									FF	1111 1111
AD1BL	A/D_1 boundary low register	BCH									00	0000 0000
AD1DAT0	A/D_1 data register 0	D5H									00	0000 0000
AD1DAT1	A/D_1 data register 1	D6H									00	0000 0000
AD1DAT2	A/D_1 data register 2	D7H									00	0000 0000
AD1DAT3	A/D_1 data register 3	F5H									00	0000 0000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS	00 ^[1]	0000 00x0
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	0000 0000
BRGR0	Baud rate generator rate low	BEH									00 ^[2]	0000 0000
BRGR1	Baud rate generator rate high	BFH									00 ^{[1][2]}	0000 0000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00 ^[2]	xxxx xx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	OE1	CO1	CMF1	00 ^[1]	xx00 0000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00 ^[1]	xx00 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H									00	0000 0000

Table 6. Special function registers - P89LPC935/936 ...continued

* indicates SFRs that are bit addressable.

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB								Hex	Binary
I2SCLL	Serial clock generator/SCL duty cycle register low	DCH									00	0000 0000
I2STAT	I ² C status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	1111 1000
ICRAH	Input capture A register high	ABH									00	0000 0000
ICRAL	Input capture A register low	AAH									00	0000 0000
ICRBH	Input capture B register high	AFH									00	0000 0000
ICRBL	Input capture B register low	AEH									00	0000 0000
Bit address			AF	AE	AD	AC	AB	AA	A9	A8		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0	EX0	00	0000 0000
Bit address			EF	EE	ED	EC	EB	EA	E9	E8		
IEN1*	Interrupt enable 1	E8H	EADEE	EST	-	ECCU	ESPI	EC	EKBI	EI2C	00 ^[3]	00x0 0000
Bit address			BF	BE	BD	BC	BB	BA	B9	B8		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0	PX0	00 ^[3]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRT H	PBOH	PSH/ PSRH	PT1H	PX1H	PT0H	PX0H	00 ^[3]	x000 0000
Bit address			FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	PADEE	PST	-	PCCU	PSPI	PC	PKBI	PI2C	00 ^[3]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	PAEEH	PSTH	-	PCCUH	PSPIH	PCH	PKBIH	PI2CH	00 ^[3]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN _SEL	KBIF	00 ^[3]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register	93H									FF	1111 1111
OCRAH	Output compare A register high	EFH									00	0000 0000
OCRAL	Output compare A register low	EEH									00	0000 0000
OCRBH	Output compare B register high	FBH									00	0000 0000
OCRBL	Output compare B register low	FAH									00	0000 0000

Table 6. Special function registers - P89LPC935/936 ...continued
** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB								Hex	Binary
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX		[4]
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60 ^{[3][5]}	011x xx00
RTCH	Real-time clock register high	D2H									00 ^[5]	0000 0000
RTCL	Real-time clock register low	D3H									00 ^[5]	0000 0000
SADDR	Serial port address register	A9H									00	0000 0000
SADEN	Serial port address enable	B9H									00	0000 0000
SBUF	Serial Port data buffer register	99H									xx	xxxx xxxx
Bit address			9F	9E	9D	9C	9B	9A	99	98		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	0000 0000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	0000 0100
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xx xxxx
SPDAT	SPI data register	E3H									00	0000 0000
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0 xxx0
Bit address			8F	8E	8D	8C	8B	8A	89	88		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	0000 0000
TCR20*	CCU control register 0	C8H	PLEEN	HLTRN	HLTEN	ALTCd	ALTAB	TDIR2	TMOD21	TMOD20	00	0000 0000
TCR21	CCU control register 1	F9H	TCOU2	-	-	-	PLLDV.3	PLLDV.2	PLLDV.1	PLLDV.0	00	0xxx 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TH2	CCU timer high	CDH									00	0000 0000
TICR2	CCU interrupt control register	C9H	TOIE2	TOCIE2 D	TOCIE2 C	TOCIE2B	TOCIE2A	-	TICIE2B	TICIE2A	00	0000 0x00
TIFR2	CCU interrupt flag register	E9H	TOIF2	TOCF2D	TOCF2C	TOCF2B	TOCF2A	-	TICF2B	TICF2A	00	0000 0x00
TISE2	CCU interrupt status encode register	DEH	-	-	-	-	-	ENCINT. 2	ENCINT. 1	ENCINT. 0	00	xxxx x000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000

Table 6. Special function registers - P89LPC935/936 ...continued

* indicates SFRs that are bit addressable.

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB				LSB				Hex	Binary
TL2	CCU timer low	CCH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	0000 0000
TOR2H	CCU reload register high	CFH									00	0000 0000
TOR2L	CCU reload register low	CEH									00	0000 0000
TPCR2H	Prescaler control register high	CBH	-	-	-	-	-	-	TPCR2H. 1	TPCR2H. 0	00	xxxx xx00
TPCR2L	Prescaler control register low	CAH	TPCR2L. 7	TPCR2L. 6	TPCR2L. 5	TPCR2L. 4	TPCR2L. 3	TPCR2L. 2	TPCR2L. 1	TPCR2L. 0	00	0000 0000
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[6] [5]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[7] [5]	
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] Unimplemented bits in SFRs (labeled '-') are X (unknown) at all times. Unless otherwise specified, ones should not be written to these bits since they may be used for other purposes in future derivatives. The reset values shown for these bits are logic 0s although they are unknown when read.

[2] All ports are in input only (high-impedance) state after power-up.

[3] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.

[4] The RSTSRC register reflects the cause of the P89LPC933/934/935/936 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx11 0000.

[5] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

[6] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[7] The only reset source that affects these SFRs is power-on reset.

8.7 CCLK wake-up delay

The P89LPC933/934/935/936 has an internal wake-up timer that delays the clock until it stabilizes depending on the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 992 OSCCLK cycles plus 60 μ s to 100 μ s. If the clock source is either the internal RC oscillator, watchdog oscillator, or external clock, the delay is 224 OSCCLK cycles plus 60 μ s to 100 μ s.

8.8 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

8.9 Low power select

The P89LPC933/934/935/936 is designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to lower the power consumption further. On any reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

8.10 Memory organization

The various P89LPC933/934/935/936 memory spaces are as follows:

- DATA
128 bytes of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.
- IDATA
Indirect Data. 256 bytes of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.
- SFR
Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.
- XDATA (P89LPC935/936)
'External' Data or Auxiliary RAM. Duplicates the classic 80C51 64 kB memory space addressed via the MOVX instruction using the SPTR, R0, or R1. All or part of this space could be implemented on-chip. The P89LPC935/936 has 512 bytes of on-chip XDATA memory.

8.13 I/O ports

The P89LPC933/934/935/936 has four I/O ports: Port 0, Port 1, Port 2, and Port 3. Ports 0, 1 and 2 are 8-bit ports, and Port 3 is a 2-bit port. The exact number of I/O pins available depends upon the clock and reset options chosen, as shown in [Table 8](#).

Table 8. Number of I/O pins available

Clock source	Reset option	Number of I/O pins (28-pin package)
On-chip oscillator or watchdog oscillator	No external reset (except during power-up)	26
	External $\overline{\text{RST}}$ pin supported	25
External clock input	No external reset (except during power-up)	25
	External $\overline{\text{RST}}$ pin supported ^[1]	24
Low/medium/high speed oscillator (external crystal or resonator)	No external reset (except during power-up)	24
	External $\overline{\text{RST}}$ pin supported ^[1]	23

[1] Required for operation above 12 MHz.

8.13.1 Port configurations

All but three I/O port pins on the P89LPC933/934/935/936 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

1. P1.5 ($\overline{\text{RST}}$) can only be an input and cannot be configured.
2. P1.2 (SCL/T0) and P1.3 (SDA/ $\overline{\text{INT0}}$) may only be configured to be either input-only or open-drain.

8.13.1.1 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC933/934/935/936 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD} , causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt trigger input that also has a glitch suppression circuit.

8.13.1.2 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD} .

8.17 Timers/counters 0 and 1

The P89LPC933/934/935/936 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate either as timers or event counter. An option to automatically toggle the T0 and/or T1 pins upon timer overflow has been added.

In the 'timer' function, the register is incremented every machine cycle.

In the 'counter' function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle.

Timer 0 and Timer 1 have five operating modes (modes 0, 1, 2, 3 and 6). Modes 0, 1, 2 and 6 are the same for both timers/counters. Mode 3 is different.

8.17.1 Mode 0

Putting either timer into Mode 0 makes it look like an 8048 timer, which is an 8-bit counter with a divide-by-32 prescaler. In this mode, the timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

8.17.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

8.17.3 Mode 2

Mode 2 configures the timer register as an 8-bit counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

8.17.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

8.17.5 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

8.17.6 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

8.18 RTC/system timer

The P89LPC933/934/935/936 has a simple RTC that allows a user to continue running an accurate timer while the rest of the device is powered-down. The RTC can be a wake-up or an interrupt source. The RTC is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all logic 0s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is

8.21 I²C-bus serial interface

The I²C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between masters and slaves
- Multi master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I²C-bus may be used for test and diagnostic purposes.

A typical I²C-bus configuration is shown in [Figure 15](#). The P89LPC933/934/935/936 device provides a byte-oriented I²C-bus interface that supports data transfers up to 400 kHz.

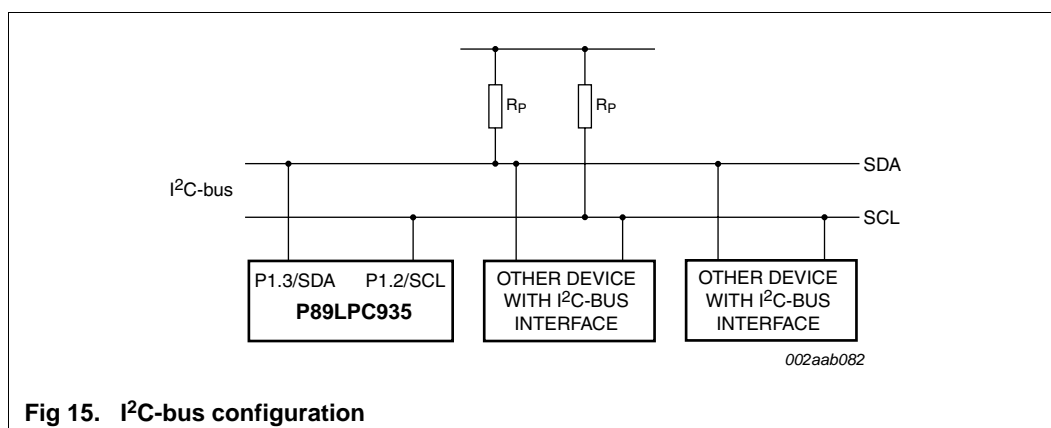
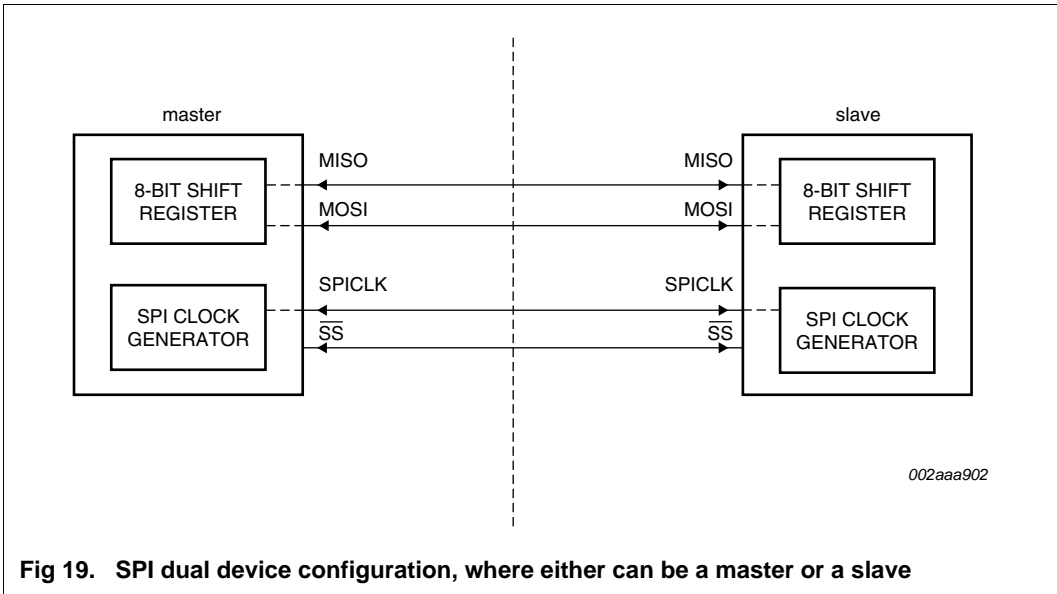
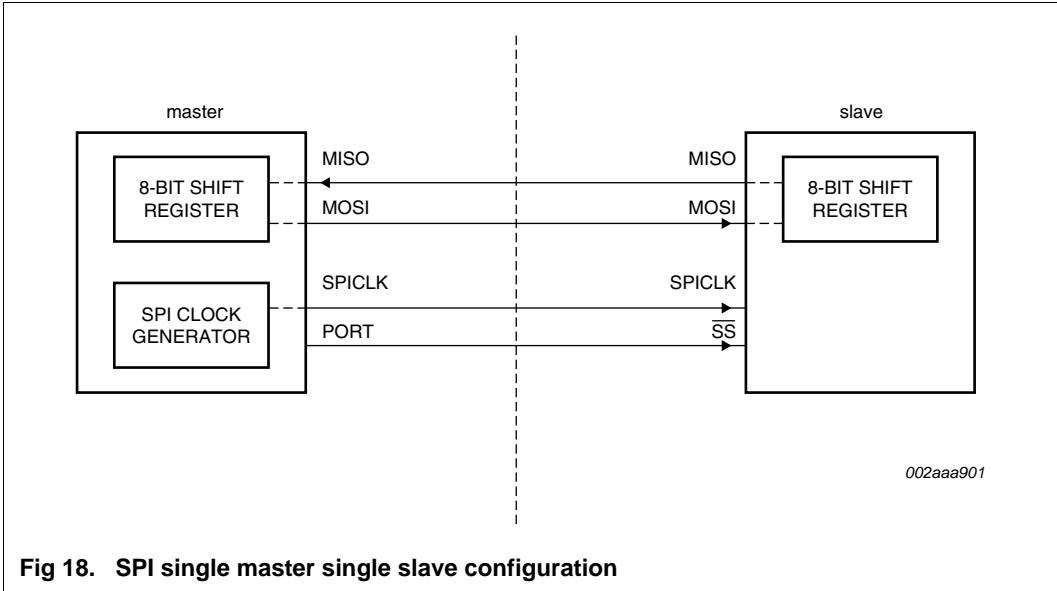


Fig 15. I²C-bus configuration

8.22.1 Typical SPI configurations



8.23 Analog comparators

Two analog comparators are provided on the P89LPC933/934/935/936. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logic 1 (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable pins) is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes.

The overall connections to both comparators are shown in [Figure 21](#). The comparators function to $V_{DD} = 2.4$ V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 microseconds. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

When a comparator is disabled the comparator's output, CO_n , goes HIGH. If the comparator output was LOW and then is disabled, the resulting transition of the comparator output from a LOW to HIGH state will set the comparator flag, CMF_n . This will cause an interrupt if the comparator interrupt is enabled. The user should therefore disable the comparator interrupt prior to disabling the comparator. Additionally, the user should clear the comparator flag, CMF_n , after disabling the comparator.

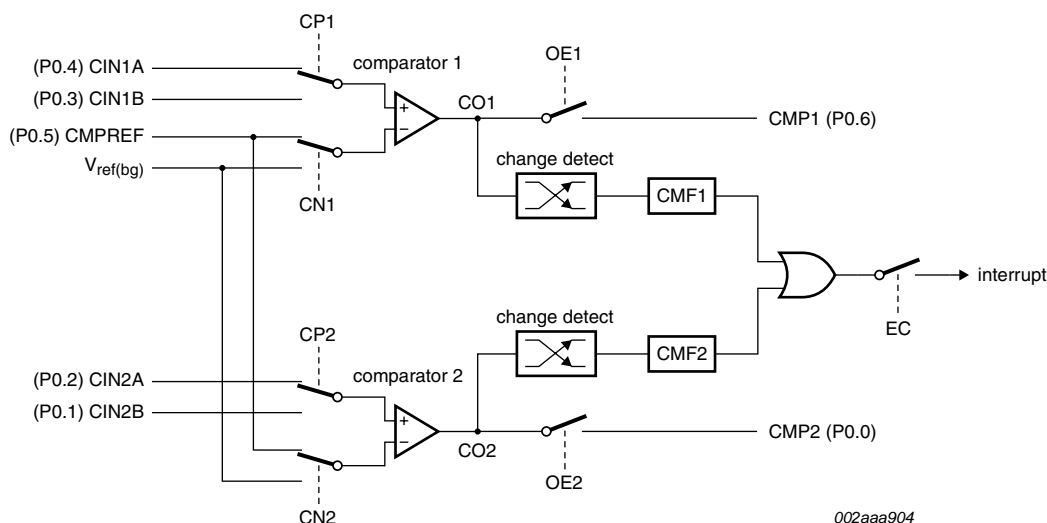


Fig 21. Comparator input and output connections

8.23.1 Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as $V_{ref(bg)}$, is $1.23\text{ V} \pm 10\%$.

8.23.2 Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The two comparators use one common interrupt vector. If both comparators enable interrupts, after entering the interrupt service routine, the user needs to read the flags to determine which comparator caused the interrupt.

8.23.3 Comparators and power reduction modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated, but both comparators are disabled automatically in Total Power-down mode.

If a comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake-up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the **oscillator** stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparators via PCONA.5, or put the device in Total Power-down mode.

8.24 Keypad interrupt

The Keypad Interrupt (KBI) function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

The Keypad Interrupt Mask register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake-up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery-powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than six CCLKs.

8.28.10 Hardware activation of the boot loader

The boot loader can also be executed by forcing the device into ISP mode during a power-on sequence (see the P89LPC933/934/935/936 *User manual* for specific information). This has the same effect as having a non-zero status byte. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting for the boot vector is changed, it will no longer point to the factory preprogrammed ISP boot loader code. After programming the flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

8.29 User configuration bytes

Some user-configurable features of the P89LPC933/934/935/936 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1. Please see the P89LPC933/934/935/936 *User manual* for additional details.

8.30 User sector security bytes

There are eight User Sector Security Bytes on the P89LPC933/934/935/936 device. Each byte corresponds to one sector. Please see the P89LPC933/934/935/936 *User manual* for additional details.

9. A/D converter

9.1 General description

The P89LPC935/936 have two 8-bit, 4-channel multiplexed successive approximation analog-to-digital converter modules sharing common control logic. The P89LPC933/934 have a single 8-bit, 4-channel multiplexed analog-to-digital converter and an additional DAC module. A block diagram of the A/D converter is shown in [Figure 23](#). Each A/D consists of a 4-input multiplexer which feeds a sample-and-hold circuit providing an input signal to one of two comparator inputs. The control logic in combination with the SAR drives a digital-to-analog converter which provides the other input to the comparator. The output of the comparator is fed to the SAR.

9.2 Features and benefits

- › Two (P89LPC935/936) 8-bit, 4-channel multiplexed input, successive approximation A/D converters with common control logic (one A/D on the P89LPC933/934).
- › Four result registers for each A/D.
- › Six operating modes:
 - ¥ Fixed channel, single conversion mode.
 - ¥ Fixed channel, continuous conversion mode.
 - ¥ Auto scan, single conversion mode.
 - ¥ Auto scan, continuous conversion mode.
 - ¥ Dual channel, continuous conversion mode.
 - ¥ Single step mode.
- › Four conversion start modes:
 - ¥ Timer triggered start.

10. Limiting values

Table 10. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).^[1]

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{\text{amb(bias)}}$	bias ambient temperature		-55	+125	°C
T_{stg}	storage temperature		-65	+150	°C
$I_{\text{OH(I/O)}}$	HIGH-level output current per input/output pin		-	20	mA
$I_{\text{OL(I/O)}}$	LOW-level output current per input/output pin		-	20	mA
$I_{\text{I/Otot(max)}}$	maximum total input/output current		-	100	mA
V_{xtal}	crystal voltage	on XTAL1, XTAL2 pin to V_{SS}	-	$V_{\text{DD}} + 0.5$	V
V_{n}	voltage on any other pin	except XTAL1, XTAL2 to V_{SS}	-0.5	+5.5	V
$P_{\text{tot(pack)}}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W

[1] The following applies to [Table 10](#):

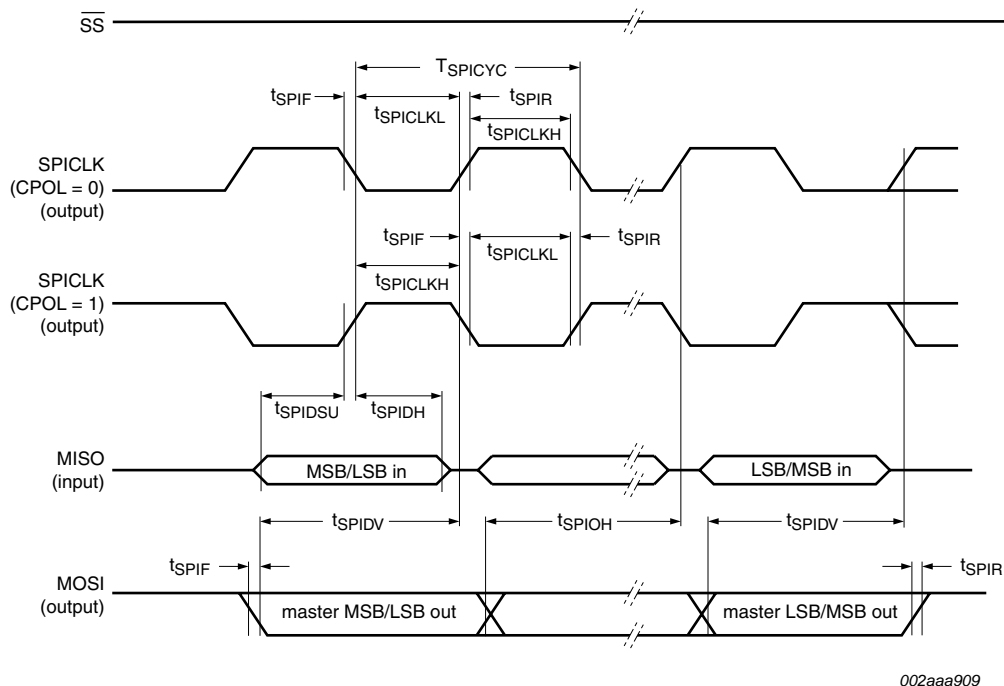
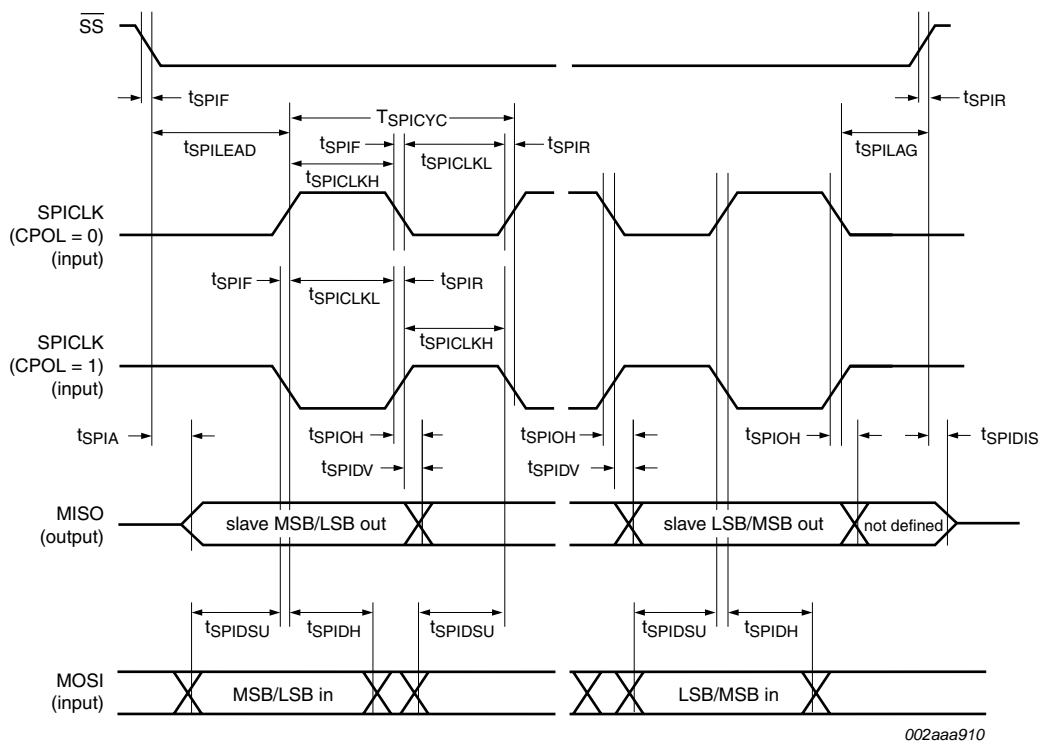
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
- Parameters are valid over ambient temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

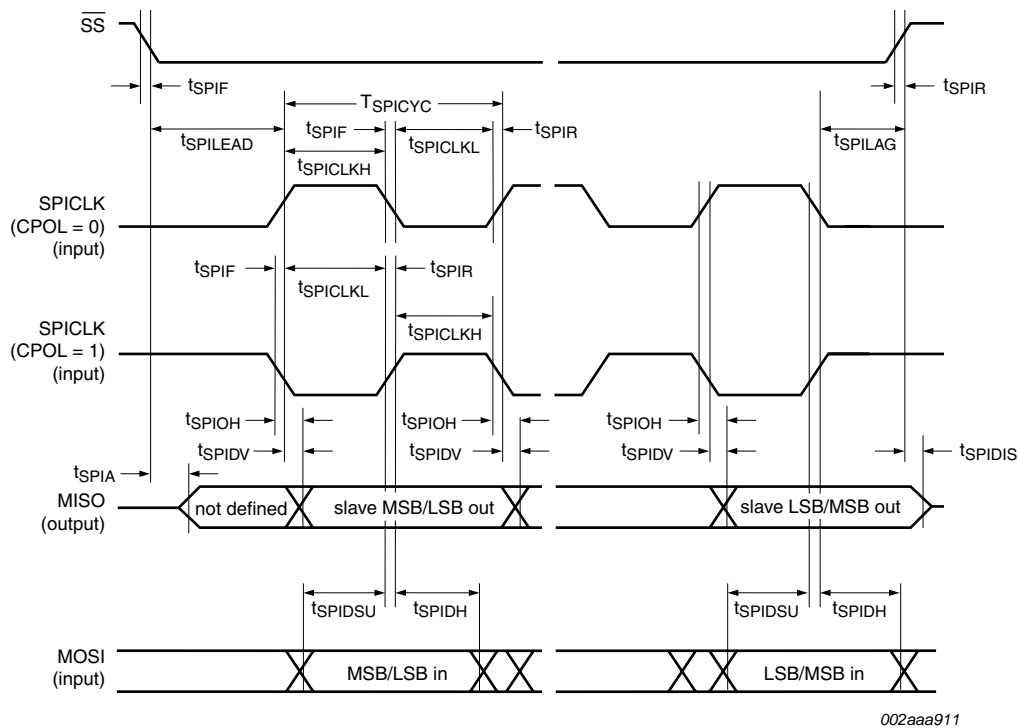
Table 13. Dynamic characteristics (18 MHz) ...continued $V_{DD} = 3.0\text{ V to } 3.6\text{ V unless otherwise specified.}$ $T_{amb} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C for industrial, } -40\text{ }^{\circ}\text{C to } +125\text{ }^{\circ}\text{C for extended, unless otherwise specified.}[1][2]$

Symbol	Parameter	Conditions	Variable clock		$f_{osc} = 18\text{ MHz}$		Unit
			Min	Max	Min	Max	
t_{SPICKH}	SPICK HIGH time	see Figure 26, 28, 29, 30					
	master		$\frac{2}{CCLK}$	-	111	-	ns
	slave		$\frac{3}{CCLK}$	-	167	-	ns
t_{SPICKL}	SPICK LOW time	see Figure 26, 28, 29, 30					
	master		$\frac{2}{CCLK}$	-	111	-	ns
	slave		$\frac{3}{CCLK}$	-	167	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 26, 28, 29, 30	100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 26, 28, 29, 30	100	-	100	-	ns
t_{SPIA}	SPI access time	see Figure 29, 30	0	80	0	80	ns
t_{SPIDIS}	SPI disable time	see Figure 29, 30	0	160	-	160	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 26, 28, 29, 30					
	slave		-	160	-	160	ns
	master		-	111	-	111	ns
t_{SPIOH}	SPI output data hold time	see Figure 26, 28, 29, 30	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 26, 28, 29, 30					
	SPI outputs (SPICK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICK, MOSI, MISO, \overline{SS})		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 26, 28, 29, 30					
	SPI outputs (SPICK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICK, MOSI, MISO, \overline{SS})		-	2000	-	2000	ns

[1] Parameters are valid over ambient temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

**Fig 28. SPI master timing (CPHA = 1)****Fig 29. SPI slave timing (CPHA = 0)**



002aaa911

Fig 30. SPI slave timing (CPHA = 1)

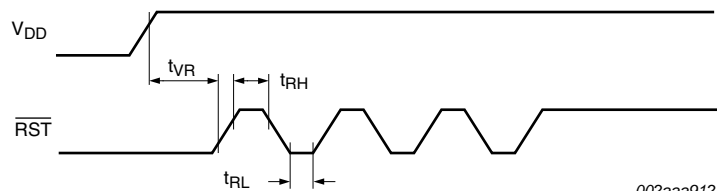
12.2 ISP entry mode

Table 14. Dynamic characteristics, ISP entry mode

$V_{DD} = 2.4\text{ V to }3.6\text{ V}$, unless otherwise specified.

$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ for industrial, $-40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C}$ for extended, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VR}	$\overline{\text{RST}}$ delay from V_{DD} active time		50	-	-	μs
t_{RH}	$\overline{\text{RST}}$ HIGH time		1	-	32	μs
t_{RL}	$\overline{\text{RST}}$ LOW time		1	-	-	μs



002aaa912

Fig 31. ISP entry timing

14. Package outline

PLCC28: plastic leaded chip carrier; 28 leads

SOT261-2

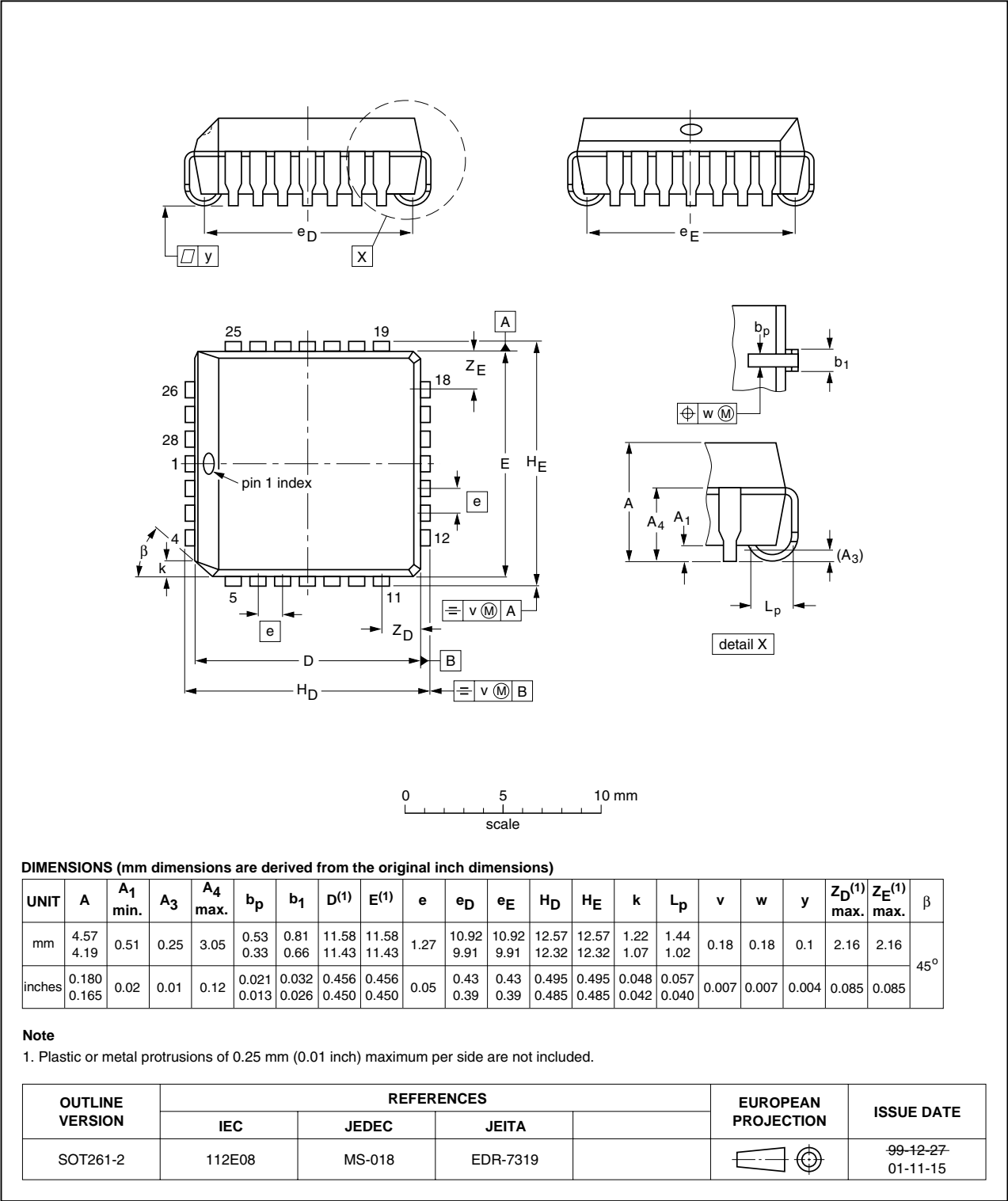


Fig 32. Package outline SOT261-2 (PLCC28)

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's

own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

18. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com