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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 12MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, LED, POR, PWM, WDT |
| Number of I/O | 26 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 512 x 8 |
| RAM Size | 768 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 3.6V |
| Data Converters | A/D 8x8b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-TSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | 28-TSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc935fdh-529 |

**Table 4. Pin description** *…continued*

| Symbol | Pin | | Type | Description |
|---|---|---|---|---|
| | TSSOP28, PLCC28 | HVQFN28 | | |
| P1.0 to P1.7 | | | I/O, I [1] | **Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.13.1 "Port configurations" and Table 11 "Static characteristics" for details. P1.2 and P1.3 are open drain when used as outputs. P1.5 is input only.<br>All pins have Schmitt trigger inputs.<br>Port 1 also provides various special functions as described below: |
| P1.0/TXD | 18 | 14 | I/O | **P1.0 —** Port 1 bit 0. |
| | | | O | **TXD —** Transmitter output for the serial port. |
| P1.1/RXD | 17 | 13 | I/O | **P1.1 —** Port 1 bit 1. |
| | | | I | **RXD —** Receiver input for the serial port. |
| P1.2/T0/SCL | 12 | 8 | I/O | **P1.2 —** Port 1 bit 2 (open-drain when used as output). |
| | | | I/O | **T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output). |
| | | | I/O | **SCL —** $I^2C$ serial clock input/output. |
| P1.3/$\overline{\text{INT0}}$/SDA | 11 | 7 | I/O | **P1.3 —** Port 1 bit 3 (open-drain when used as output). |
| | | | I | **$\overline{\text{INT0}}$ —** External interrupt 0 input. |
| | | | I/O | **SDA —** $I^2C$ serial data input/output. |
| P1.4/$\overline{\text{INT1}}$ | 10 | 6 | I | **P1.4 —** Port 1 bit 4. |
| | | | I | **$\overline{\text{INT1}}$ —** External interrupt 1 input. |
| P1.5/$\overline{\text{RST}}$ | 6 | 2 | I | **P1.5 —** Port 1 bit 5 (input only). |
| | | | I | **$\overline{\text{RST}}$ —** External reset input during power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until VDD has reached its specified level. When system power is removed VDD will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when VDD falls below the minimum specified operating voltage.** |
| P1.6/OCB | 5 | 1 | I/O | **P1.6 —** Port 1 bit 6. |
| | | | O | **OCB —** Output Compare B. (P89LPC935/936) |
| P1.7/OCC/AD00 | 4 | 28 | I/O | **P1.7 —** Port 1 bit 7. |
| | | | O | **OCC —** Output Compare C. (P89LPC935/936) |
| | | | I | **AD00 —** ADC0 channel 0 analog input. (P89LPC935/936) |

**Table 4. Pin description** *…continued*

| Symbol | Pin | | Type | Description |
|---|---|---|---|---|
| | TSSOP28, PLCC28 | HVQFN28 | | |
| P3.0 to P3.1 | | | I/O | **Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.13.1 “Port configurations” and Table 11 “Static characteristics” for details.<br>All pins have Schmitt trigger inputs.<br>Port 3 also provides various special functions as described below: |
| P3.0/XTAL2/ CLKOUT | 9 | 5 | I/O | **P3.0 —** Port 3 bit 0. |
| | | | O | **XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration. |
| | | | O | **CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the RTC/system timer. |
| P3.1/XTAL1 | 8 | 4 | I/O | **P3.1 —** Port 3 bit 1. |
| | | | I | **XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the RTC/system timer. |
| $V_{SS}$ | 7 | 3 | I | **Ground:** 0 V reference. |
| $V_{DD}$ | 21 | 17 | I | **Power supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes. |

[1] Input/output for P1.0 to P1.4, P1.6, P1.7. Input for P1.5.

# 7. Logic symbols

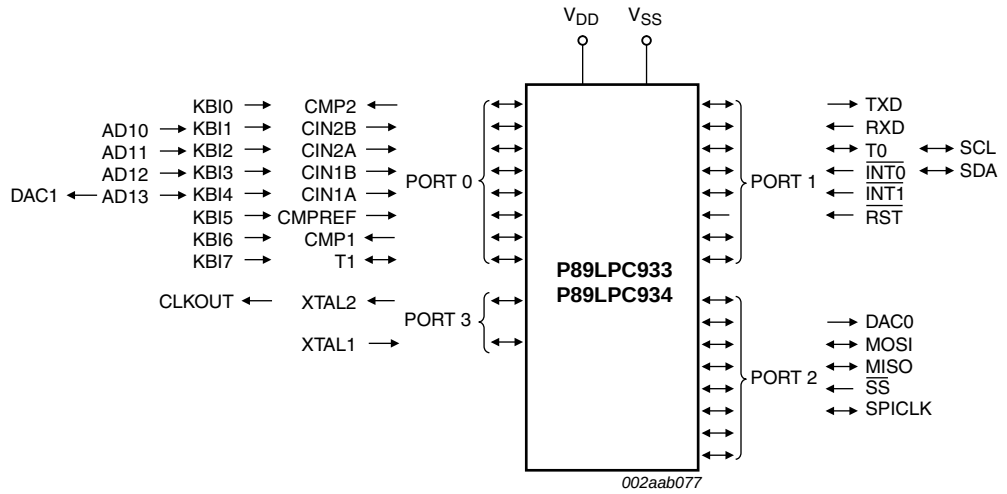



**Fig 6. P89LPC933/934 logic symbol**

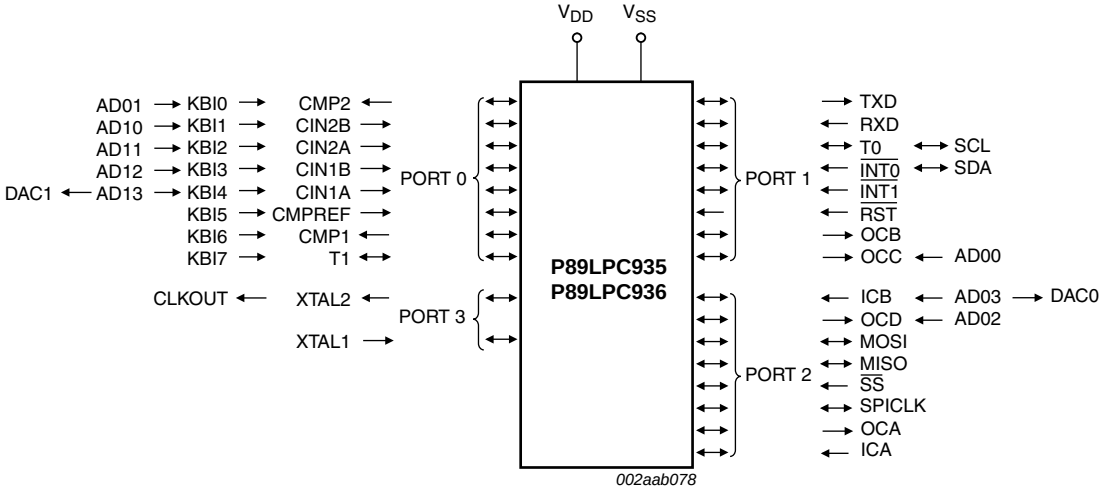



**Fig 7. P89LPC935/936 logic symbol**

**Table 5. Special function registers - P89LPC933/934** *…continued*

** indicates SFRs that are bit addressable.*

| Name | Description | SFR addr. | Bit functions and addresses | | Reset value | |
|---|---|---|---|---|---|---|
| | | | MSB | LSB | Hex | Binary |
| WDL | Watchdog load | C1H | | | FF | 1111 1111 |
| WFEED1 | Watchdog feed 1 | C2H | | | | |
| WFEED2 | Watchdog feed 2 | C3H | | | | |

[1] Unimplemented bits in SFRs (labeled '-') are X (unknown) at all times. Unless otherwise specified, ones should not be written to these bits since they may be used for other purposes in future derivatives. The reset values shown for these bits are logic 0s although they are unknown when read.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.

[3] All ports are in input only (high-impedance) state after power-up.

[4] The RSTSRC register reflects the cause of the P89LPC933/934/935/936 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx11 0000.

[5] The only reset source that affects these SFRs is power-on reset.

[6] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[7] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

## 8.7 CCLK wake-up delay

The P89LPC933/934/935/936 has an internal wake-up timer that delays the clock until it stabilizes depending on the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 992 OSCCLK cycles plus 60 μs to 100 μs. If the clock source is either the internal RC oscillator, watchdog oscillator, or external clock, the delay is 224 OSCCLK cycles plus 60 μs to 100 μs.

## 8.8 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

## 8.9 Low power select

The P89LPC933/934/935/936 is designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to lower the power consumption further. On any reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

## 8.10 Memory organization

The various P89LPC933/934/935/936 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 bytes of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.

- SFR

  Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

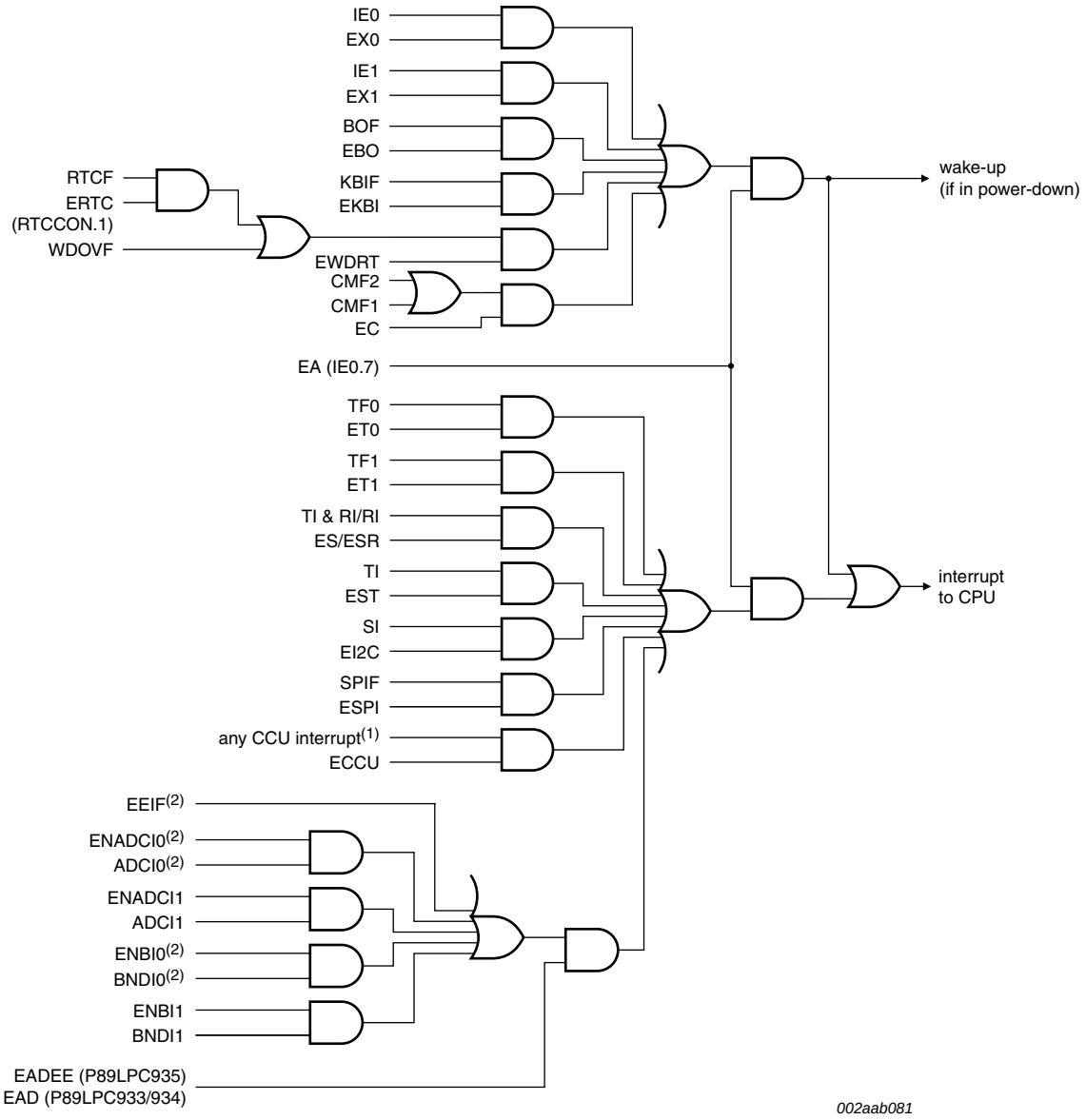
- XDATA (P89LPC935/936)

  ‘External’ Data or Auxiliary RAM. Duplicates the classic 80C51 64 kB memory space addressed via the MOVX instruction using the SPTR, R0, or R1. All or part of this space could be implemented on-chip. The P89LPC935/936 has 512 bytes of on-chip XDATA memory.

These external interrupts can be programmed to be level-triggered or edge-triggered by setting or clearing bit IT1 or IT0 in register TCON.

In edge-triggered mode, if successive samples of the $\overline{\text{INTn}}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request flag IEn in TCON is set, causing an interrupt request.

If an external interrupt is enabled when the P89LPC933/934/935/936 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 8.15 “Power reduction modes” for details.




(1) See Section 8.19 “CCU (P89LPC935/936)”

(2) P89LPC935/936

**Fig 9. Interrupt sources, interrupt enables, and power-down wake-up sources**

### 8.14.1 Brownout detection

The brownout detect function determines if the power supply voltage drops below a certain level. The default operation is for a brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt.

Brownout detection may be enabled or disabled in software.

If brownout detection is enabled the brownout condition occurs when $V_{DD}$ falls below the brownout trip voltage, $V_{bo}$ (see Table 11 “Static characteristics”), and is negated when $V_{DD}$ rises above $V_{bo}$. If the P89LPC933/934/935/936 device is to operate with a power supply that can be below 2.7 V, BOE should be left in the unprogrammed state so that the device can operate at 2.4 V, otherwise continuous brownout reset may prevent the device from operating.

For correct activation of brownout detect, the $V_{DD}$ rise and fall times must be observed. Please see Table 11 “Static characteristics” for specifications.

### 8.14.2 Power-on detection

The power-on detect has a function similar to the brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

## 8.15 Power reduction modes

The P89LPC933/934/935/936 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

### 8.15.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

### 8.15.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC933/934/935/936 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the RAM keep-alive voltage $V_{RAM}$. This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after $V_{DD}$ has been lowered to $V_{DDR}$, therefore it is highly recommended to wake-up the processor via reset in this case. $V_{DD}$ must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during power-down. These include: brownout detect, watchdog timer, Comparators (note that Comparators can be powered-down separately), and RTC/system timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock and the RTC is enabled.

not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source. Only power-on reset will reset the RTC and its associated SFRs to the default state.

## 8.19 CCU (P89LPC935/936)

This unit features:

- A 16-bit timer with 16-bit reload on overflow.
- Selectable clock, with prescaler to divide clock source by any integral number between 1 and 1024.
- Four compare/PWM outputs with selectable polarity.
- Symmetrical/asymmetrical PWM selection.
- Two capture inputs with event counter and digital noise rejection filter.
- Seven interrupts with common interrupt vector (one overflow, two capture, four compare).
- Safe 16-bit read/write via shadow registers.

### 8.19.1 CCU clock

The CCU runs on the CCUCLK, which is either PCLK in basic timer mode, or the output of a Phase-Locked Loop (PLL). The PLL is designed to use a clock source between 0.5 MHz to 1 MHz that is multiplied by 32 to produce a CCUCLK between 16 MHz and 32 MHz in PWM mode (asymmetrical or symmetrical). The PLL contains a 4-bit divider to help divide PCLK into a frequency between 0.5 MHz and 1 MHz.

### 8.19.2 CCUCLK prescaling

This CCUCLK can further be divided down by a prescaler. The prescaler is implemented as a 10-bit free-running counter with programmable reload at overflow.

### 8.19.3 Basic timer operation

The timer is a free-running up/down counter with a direction control bit. If the timer counting direction is changed while the counter is running, the count sequence will be reversed. The timer can be written or read at any time.

When a reload occurs, the CCU Timer Overflow Interrupt Flag will be set, and an interrupt generated if enabled. The 16-bit CCU timer may also be used as an 8-bit up/down timer.

### 8.19.4 Output compare

There are four output compare channels A, B, C and D. Each output compare channel needs to be enabled in order to operate and the user will have to set the associated I/O pin to the desired output mode to connect the pin. When the contents of the timer matches that of a capture compare control register, the Timer Output Compare Interrupt Flag (TOCFx) becomes set. An interrupt will occur if enabled.

### 8.19.5 Input capture

Input capture is always enabled. Each time a capture event occurs on one of the two input capture pins, the contents of the timer is transferred to the corresponding 16-bit input capture register. The capture event can be programmed to be either rising or falling edge triggered. A simple noise filter can be enabled on the input capture by enabling the Input

### 8.19.7 Alternating output mode

In asymmetrical mode, the user can set up PWM channels A/B and C/D as alternating pairs for bridge drive control. In this mode the output of these PWM channels are alternately gated on every counter cycle.

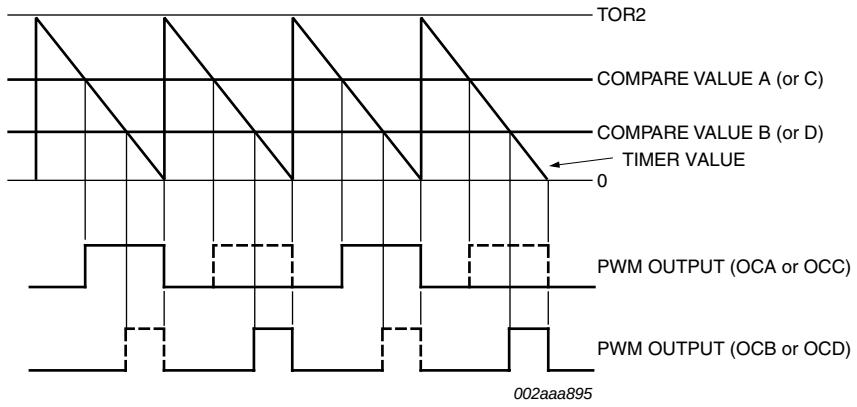



**Fig 12. Alternate output mode**

### 8.19.8 PLL operation

The PWM module features a PLL that can be used to generate a CCUCLK frequency between 16 MHz and 32 MHz. At this frequency the PWM module provides ultrasonic PWM frequency with 10-bit resolution provided that the crystal frequency is 1 MHz or higher. The PLL is fed an input signal from 0.5 MHz to 1 MHz and generates an output signal of 32 times the input frequency. This signal is used to clock the timer. The user will have to set a divider that scales PCLK by a factor from 1 to 16. This divider is found in the SFR register TCR21. The PLL frequency can be expressed as shown in Equation 1.

$$\text{PLL frequency} = \frac{\text{PCLK}}{(N+1)} \quad (1)$$

Where: N is the value of PLLDV.3 to PLLDV.0.

Since N ranges from 0 to 15, the CCLK frequency can be in the range of PCLK to $^{PCLK}/_{16}$.

### 8.19.9 CCU interrupts

There are seven interrupt sources on the CCU which share a common interrupt vector.

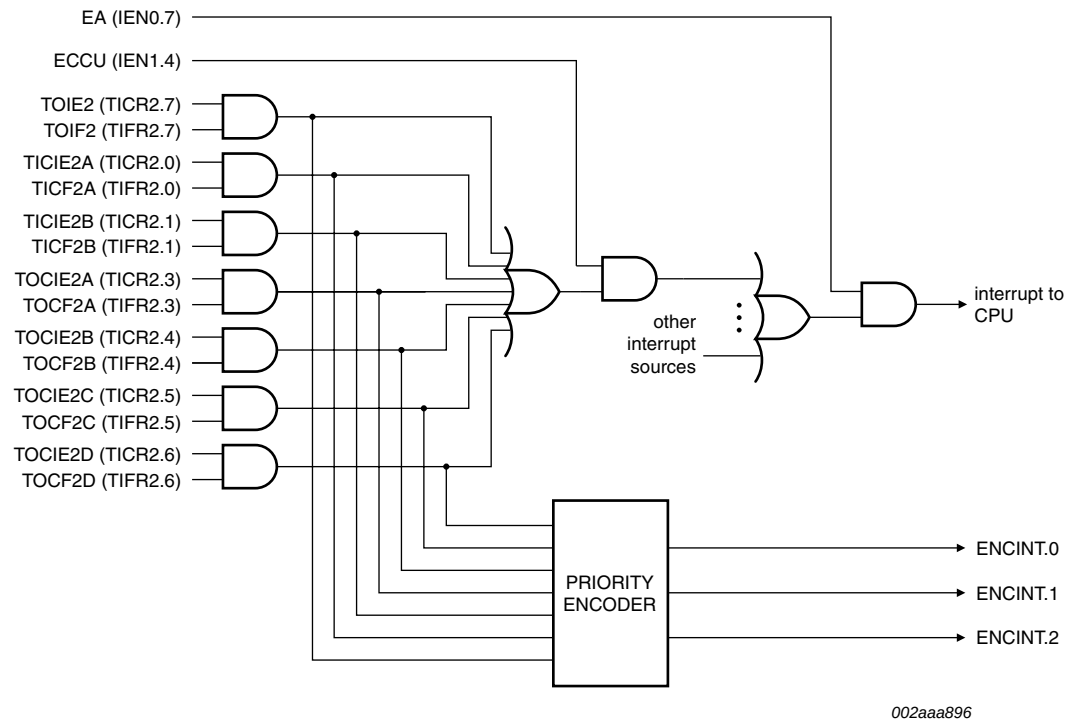



**Fig 13. Capture/compare unit interrupts**

## 8.20 UART

The P89LPC933/934/935/936 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC933/934/935/936 does include an independent baud rate generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent baud rate generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in four modes: shift register, 8-bit UART, 9-bit UART, and CPU $^{clock}/_{32}$ or CPU $^{clock}/_{16}$.

### 8.20.1 Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $^{1}/_{16}$ of the CPU clock frequency.

### 8.20.2 Mode 1

10 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). When data is received, the stop bit is stored in RB8 in special function register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the baud rate generator (described in Section 8.20.5 “Baud rate generator and selection”).

### 8.20.3 Mode 2

11 bits are transmitted (through TXD) or received (through RXD): start bit (logic 0), 8 data bits (LSB first), a programmable 9$^{th}$ data bit, and a stop bit (logic 1). When data is transmitted, the 9$^{th}$ data bit (TB8 in SCON) can be assigned the value of logic 0 or logic 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9$^{th}$ data bit goes into RB8 in special function register SCON, while the stop bit is not saved. The baud rate is programmable to either $^{1}/_{16}$ or $^{1}/_{32}$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

### 8.20.4 Mode 3

11 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), a programmable 9$^{th}$ data bit, and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the baud rate generator (described in Section 8.20.5 “Baud rate generator and selection”).

### 8.20.5 Baud rate generator and selection

The P89LPC933/934/935/936 enhanced UART has an independent baud rate generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1 but is much more accurate. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see Figure 14). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is cleared. The independent baud rate generator uses CCLK.

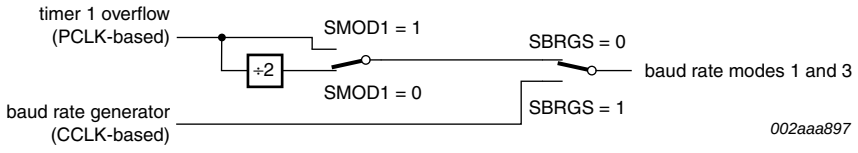



**Fig 14. Baud rate sources for UART (Modes 1, 3)**

### 8.20.6 Framing error

Framing error is reported in the status register (SSTAT). In addition, if SMOD0 (PCON.6) is logic 1, framing errors can be made available in SCON.7 respectively. If SMOD0 is logic 0, SCON.7 is SM0. It is recommended that SM0 and SM1 (SCON.7:6) are set up when SMOD0 is logic 0.

### 8.22.1 Typical SPI configurations

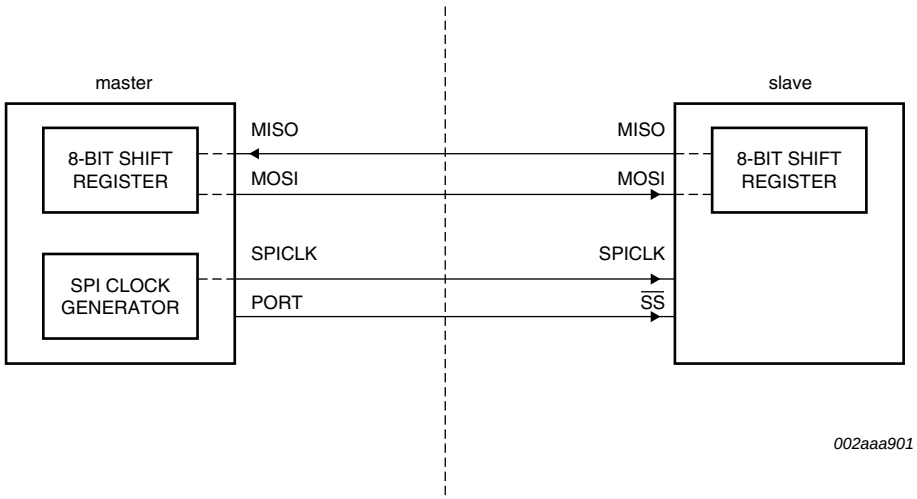



**Fig 18. SPI single master single slave configuration**

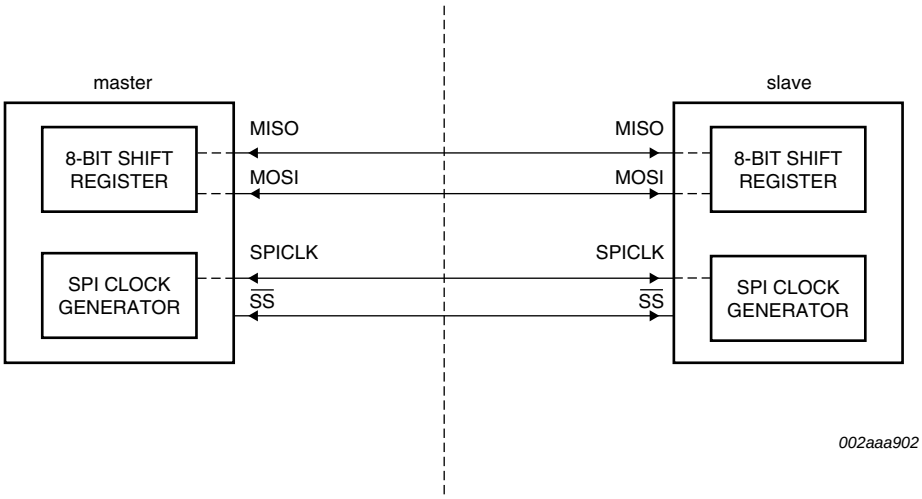



**Fig 19. SPI dual device configuration, where either can be a master or a slave**

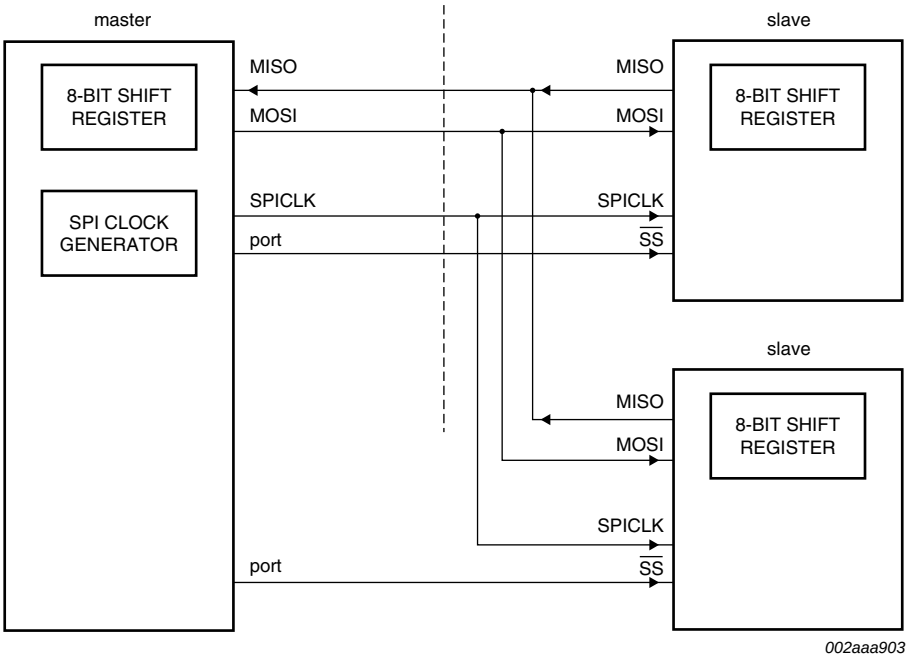



**Fig 20. SPI single master multiple slaves configuration**

### 8.28.3 Flash organization

The program memory consists of eight 2 kB sectors on the P89LPC936 device, eight 1 kB sectors on the P89LPC934/935 devices, and four 1 kB sectors on the P89LPC933 device. Each sector can be further divided into 64-byte pages. In addition to sector erase, page erase, and byte erase, a 64-byte page register is included which allows from 1 to 64 bytes of a given page to be programmed at the same time, substantially reducing overall programming time.

### 8.28.4 Using flash as data storage

The flash code memory array of this device supports individual byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

### 8.28.5 Flash programming and erasing

Four different methods of erasing or programming of the flash are available. The flash may be programmed or erased in the end-user application (IAP) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock - serial data interface. As shipped from the factory, the upper 512 bytes of user code space contains a serial ISP routine allowing the device to be programmed in circuit through the serial port. The flash may also be programmed or erased using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead, this device provides a 32-bit CRC result on either a sector or the entire user code space.

### 8.28.6 In-circuit programming

ICP is performed without removing the microcontroller from the system. The ICP facility consists of internal hardware resources to facilitate remote programming of the P89LPC933/934/935/936 through a two-wire serial interface. The Philips ICP facility has made ICP in an embedded application—using commercially available programmers—possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the P89LPC933/934/935/936 *User manual*.

### 8.28.7 In-application programming

IAP is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The Philips IAP has made IAP in an embedded application possible without additional components. Two methods are available to accomplish IAP. A set of predefined IAP functions are provided in a boot ROM and can be called through a common interface, PGM_MTP. Several IAP calls are available for use by an application program to permit selective erasing and programming of flash sectors, pages, security bits, configuration bytes, and device ID. These functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FF03H. The boot ROM occupies the program memory space at the top of the address space from FF00H to FFEFH, thereby not conflicting with the user program memory space.

In addition, IAP operations can be accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the P89LPC933/934/935/936 *User manual*.

### 8.28.8 ISP

ISP is performed without removing the microcontroller from the system. The ISP facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89LPC933/934/935/936 through the serial port. This firmware is provided by Philips and embedded within each P89LPC933/934/935/936 device. The Philips ISP facility has made ISP in an embedded application possible with a minimum of additional expense in components and circuit board area. The ISP function uses five pins ($V_{DD}$, $V_{SS}$, TXD, RXD, and $\overline{RST}$). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature.

### 8.28.9 Power-on reset code execution

The P89LPC933/934/935/936 contains two special flash elements: the boot vector and the boot status bit. Following reset, the P89LPC933/934/935/936 examines the contents of the boot status bit. If the boot status bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the boot status bit is set to a value other than zero, the contents of the boot vector are used as the high byte of the execution address and the low byte is set to 00H.

Table 9 shows the factory default boot vector settings for these devices.

**Remark:** These settings are different than the original P89LPC932. Tools designed to support the P89LPC933/934/935/936 should be used to program this device, such as Flash Magic version 1.98, or later.

A factory-provided boot loader is preprogrammed into the address space indicated and uses the indicated boot loader entry point to perform ISP functions. This code can be erased by the user.

**Remark:** Users who wish to use this loader should take precautions to avoid erasing the sector that contains this boot loader. Instead, the page erase function can be used to erase the pages located in this sector which are not used by the boot loader.

A custom boot loader can be written with the boot vector set to the custom boot loader, if desired.

**Table 9. Default boot vector values and ISP entry points**

| Device | Default boot vector | Default boot loader entry point | Default boot loader code range | Boot sector range |
|---|---|---|---|---|
| P89LPC933 | 0FH | 0F00H | 0E00H to 0FFFH | 0C00H to 0FFFH |
| P89LPC934 | 1FH | 1F00H | 1E00H to 1FFFH | 1C00H to 1FFFH |
| P89LPC935 | 1FH | 1F00H | 1E00H to 1FFFH | 1C00H to 1FFFH |
| P89LPC936 | 3FH | 3F00H | 3E00H to 3FFFH | 3C00H to 3FFFH |

**Table 11. Static characteristics** *…continued*

*$V_{DD}$ = 2.4 V to 3.6 V unless otherwise specified.*
*$T_{amb}$ = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{IL}$ | LOW-level input current | $V_I$ = 0.4 V | [7] | - | - | −80 | μA |
| $I_{LI}$ | input leakage current | $V_I = V_{IL}$, $V_{IH}$ or $V_{th(HL)}$ | [8] | - | - | ±10 | μA |
| $I_{THL}$ | HIGH-LOW transition current | all ports; $V_I$ = 1.5 V at $V_{DD}$ = 3.6 V | [9] | −30 | - | −450 | μA |
| $R_{RST\_N(int)}$ | internal pull-up resistance on pin $\overline{RST}$ | | | 10 | - | 30 | kΩ |
| $V_{bo}$ | brownout trip voltage | 2.4 V < $V_{DD}$ < 3.6 V; with BOV = 1, BOPD = 0 | | 2.40 | - | 2.70 | V |
| $V_{ref(bg)}$ | band gap reference voltage | | | 1.11 | 1.23 | 1.34 | V |
| $TC_{bg}$ | band gap temperature coefficient | | | - | 10 | 20 | ppm/°C |

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$, and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, real-time clock, and watchdog timer.

[3] The $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.

[4] See Section 10 “Limiting values” for steady state (non-transient) limits on $I_{OL}$ or $I_{OH}$. If $I_{OL}/I_{OH}$ exceeds the test condition, $V_{OL}/V_{OH}$ may exceed the related specification.

[5] This specification can be applied to pins which have A/D input or analog comparator input functions when the pin is not being used for those analog functions. When the pin is being used as an analog input pin, the maximum voltage on the pin must be limited to 4.0 V with respect to $V_{SS}$.

[6] Pin capacitance is characterized but not tested.

[7] Measured with port in quasi-bidirectional mode.

[8] Measured with port in high-impedance mode.

[9] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when $V_I$ is approximately 2 V.

# 12. Dynamic characteristics

**Table 12. Dynamic characteristics (12 MHz)**

*$V_{DD}$ = 2.4 V to 3.6 V unless otherwise specified.*

*$T_{amb}$ = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.*[1][2]

| Symbol | Parameter | Conditions | Variable clock | | $f_{osc}$ = 12 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $f_{osc(RC)}$ | internal RC oscillator frequency | | 7.189 | 7.557 | 7.189 | 7.557 | MHz |
| $f_{osc(WD)}$ | internal watchdog oscillator frequency | | 320 | 520 | 320 | 520 | kHz |
| $f_{osc}$ | oscillator frequency | | 0 | 12 | - | - | MHz |
| $T_{cy(clk)}$ | clock cycle time | see Figure 27 | 83 | - | - | - | ns |
| $f_{CLKLP}$ | low-power select clock frequency | | 0 | 8 | - | - | MHz |
| **Glitch filter** | | | | | | | |
| $t_{gr}$ | glitch rejection time | P1.5/$\overline{RST}$ pin | - | 50 | - | 50 | ns |
| | | any pin except P1.5/$\overline{RST}$ | - | 15 | - | 15 | ns |
| $t_{sa}$ | signal acceptance time | P1.5/$\overline{RST}$ pin | 125 | - | 125 | - | ns |
| | | any pin except P1.5/$\overline{RST}$ | 50 | - | 50 | - | ns |
| **External clock** | | | | | | | |
| $t_{CHCX}$ | clock HIGH time | see Figure 27 | 33 | $T_{cy(CLK)} - t_{CLCX}$ | 33 | - | ns |
| $t_{CLCX}$ | clock LOW time | see Figure 27 | 33 | $T_{cy(CLK)} - t_{CHCX}$ | 33 | - | ns |
| $t_{CLCH}$ | clock rise time | see Figure 27 | - | 8 | - | 8 | ns |
| $t_{CHCL}$ | clock fall time | see Figure 27 | - | 8 | - | 8 | ns |
| **Shift register (UART mode 0)** | | | | | | | |
| $T_{XLXL}$ | serial port clock cycle time | see Figure 25 | $16T_{cy(CLK)}$ | - | 1333 | - | ns |
| $t_{QVXH}$ | output data set-up to clock rising edge time | see Figure 25 | $13T_{cy(CLK)}$ | - | 1083 | - | ns |
| $t_{XHQX}$ | output data hold after clock rising edge time | see Figure 25 | - | $T_{cy(CLK)}$ + 20 | - | 103 | ns |
| $t_{XHDX}$ | input data hold after clock rising edge time | see Figure 25 | - | 0 | - | 0 | ns |
| $t_{XHDV}$ | input data valid to clock rising edge time | see Figure 25 | 150 | - | 150 | - | ns |
| **SPI interface** | | | | | | | |
| $f_{SPI}$ | SPI operating frequency | | | | | | |
| | slave | | 0 | $^{CCLK}/_{6}$ | 0 | 2.0 | MHz |
| | master | | - | $^{CCLK}/_{4}$ | - | 3.0 | MHz |
| $T_{SPICYC}$ | SPI cycle time | see Figure 26, 28, 29, 30 | | | | | |
| | slave | | $^{6}/_{CCLK}$ | - | 500 | - | ns |
| | master | | $^{4}/_{CCLK}$ | - | 333 | - | ns |
| $t_{SPILEAD}$ | SPI enable lead time | see Figure 29, 30 | | | | | |
| | slave | | 250 | - | 250 | - | ns |

**Table 12. Dynamic characteristics (12 MHz)** *…continued*

*$V_{DD}$ = 2.4 V to 3.6 V unless otherwise specified.*

*$T_{amb}$ = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.*[1][2]

| Symbol | Parameter | Conditions | Variable clock | | $f_{osc}$ = 12 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{SPILAG}$ | SPI enable lag time | see Figure 29, 30 | | | | | |
| | slave | | 250 | - | 250 | - | ns |
| $t_{SPICLKH}$ | SPICLK HIGH time | see Figure 26, 28, 29, 30 | | | | | |
| | master | | $^{2}/_{CCLK}$ | - | 165 | - | ns |
| | slave | | $^{3}/_{CCLK}$ | - | 250 | - | ns |
| $t_{SPICLKL}$ | SPICLK LOW time | see Figure 26, 28, 29, 30 | | | | | |
| | master | | $^{2}/_{CCLK}$ | - | 165 | - | ns |
| | slave | | $^{3}/_{CCLK}$ | - | 250 | - | ns |
| $t_{SPIDSU}$ | SPI data set-up time | see Figure 26, 28, 29, 30 | | | | | |
| | master or slave | | 100 | - | 100 | - | ns |
| $t_{SPIDH}$ | SPI data hold time | see Figure 26, 28, 29, 30 | | | | | |
| | master or slave | | 100 | - | 100 | - | ns |
| $t_{SPIA}$ | SPI access time | see Figure 29, 30 | | | | | |
| | slave | | 0 | 120 | 0 | 120 | ns |
| $t_{SPIDIS}$ | SPI disable time | see Figure 29, 30 | | | | | |
| | slave | | 0 | 240 | - | 240 | ns |
| $t_{SPIDV}$ | SPI enable to output data valid time | see Figure 26, 28, 29, 30 | | | | | |
| | slave | | - | 240 | - | 240 | ns |
| | master | | - | 167 | - | 167 | ns |
| $t_{SPIOH}$ | SPI output data hold time | see Figure 26, 28, 29, 30 | 0 | - | 0 | - | ns |
| $t_{SPIR}$ | SPI rise time | see Figure 26, 28, 29, 30 | | | | | |
| | SPI outputs (SPICLK, MOSI, MISO) | | - | 100 | - | 100 | ns |
| | SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$) | | - | 2000 | - | 2000 | ns |
| $t_{SPIF}$ | SPI fall time | see Figure 26, 28, 29, 30 | | | | | |
| | SPI outputs (SPICLK, MOSI, MISO) | | - | 100 | - | 100 | ns |
| | SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$) | | - | 2000 | - | 2000 | ns |

[1] Parameters are valid over ambient temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

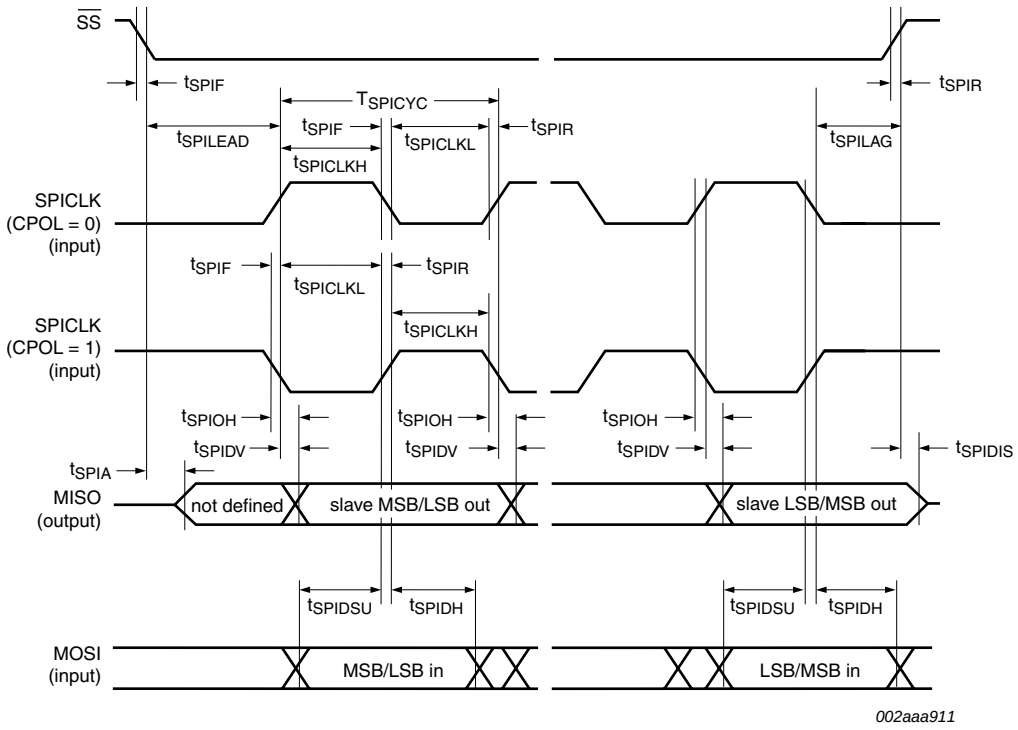



**Fig 30. SPI slave timing (CPHA = 1)**

## 12.2 ISP entry mode

**Table 14. Dynamic characteristics, ISP entry mode**

*$V_{DD}$ = 2.4 V to 3.6 V, unless otherwise specified.*
*$T_{amb}$ = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{VR}$ | $\overline{RST}$ delay from $V_{DD}$ active time | | 50 | - | - | µs |
| $t_{RH}$ | $\overline{RST}$ HIGH time | | 1 | - | 32 | µs |
| $t_{RL}$ | $\overline{RST}$ LOW time | | 1 | - | - | µs |

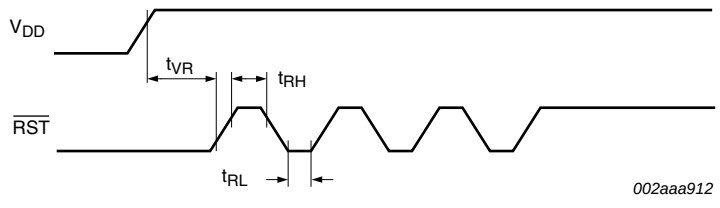



**Fig 31. ISP entry timing**

# 13. Other characteristics

## 13.1 Comparator electrical characteristics

**Table 15. Comparator electrical characteristics**

*$V_{DD}$ = 2.4 V to 3.6 V, unless otherwise specified.*
*$T_{amb}$ = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IO}$ | input offset voltage | | - | - | ±20 | mV |
| $V_{IC}$ | common-mode input voltage | | 0 | - | $V_{DD}$ − 0.3 | V |
| CMRR | common-mode rejection ratio | [1] | - | - | −50 | dB |
| $t_{res(tot)}$ | total response time | | - | 250 | 500 | ns |
| $t_{(CE-OV)}$ | chip enable to output valid time | | - | - | 10 | μs |
| $I_{LI}$ | input leakage current | $0 < V_I < V_{DD}$ | - | - | ±10 | μA |

[1] This parameter is characterized, but not tested in production.