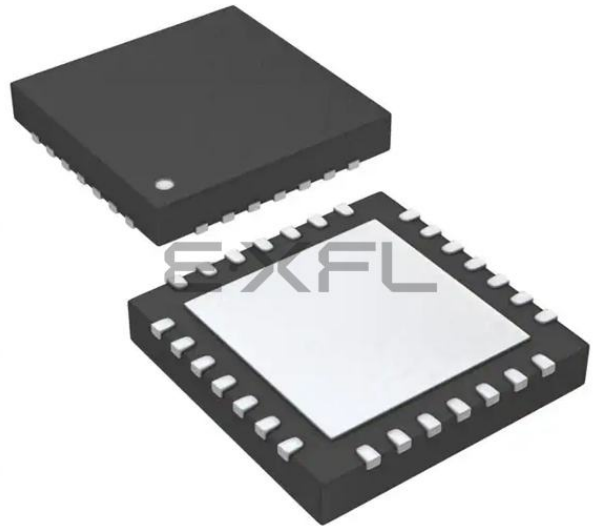

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Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	12MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x8b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-HVQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc935fhn-151

5. Block diagram

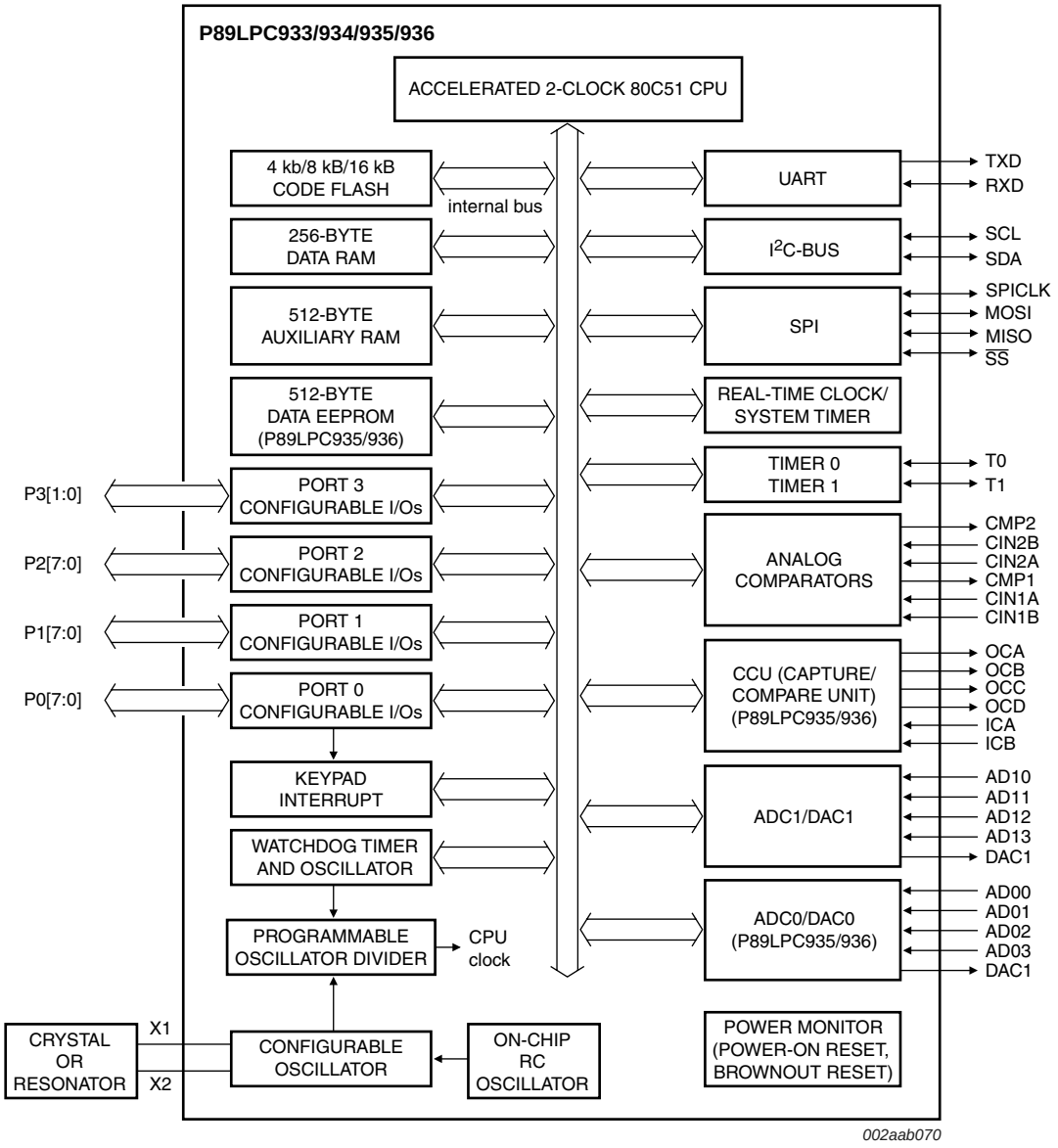

Fig 1. Block diagram

6.2 Pin description

Table 4. Pin description

Symbol	Pin		Type	Description
	TSSOP28, PLCC28	HVQFN28		
P0.0 to P0.7			I/O	**Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.13.1 “Port configurations” and Table 11 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt trigger inputs. Port 0 also provides various special functions as described below:
P0.0/CMP2/ KBI0/AD01	3	27	I/O	**P0.0 —** Port 0 bit 0.
			O	**CMP2 —** Comparator 2 output.
			I	**KBI0 —** Keyboard input 0.
			I	**AD01 —** ADC0 channel 1 analog input. (P89LPC935/936)
P0.1/CIN2B/ KBI1/AD10	26	22	I/O	**P0.1 —** Port 0 bit 1.
			I	**CIN2B —** Comparator 2 positive input B.
			I	**KBI1 —** Keyboard input 1.
			I	**AD10 —** ADC1 channel 0 analog input.
P0.2/CIN2A/ KBI2/AD11	25	21	I/O	**P0.2 —** Port 0 bit 2.
			I	**CIN2A —** Comparator 2 positive input A.
			I	**KBI2 —** Keyboard input 2.
			I	**AD11 —** ADC1 channel 1 analog input.
P0.3/CIN1B/ KBI3/AD12	24	20	I/O	**P0.3 —** Port 0 bit 3.
			I	**CIN1B —** Comparator 1 positive input B.
			I	**KBI3 —** Keyboard input 3.
			I	**AD12 —** ADC1 channel 2 analog input.
P0.4/CIN1A/ KBI4/DAC1/ AD13	23	19	I/O	**P0.4 —** Port 0 bit 4.
			I	**CIN1A —** Comparator 1 positive input A.
			I	**KBI4 —** Keyboard input 4.
			O	**DAC1 —** Digital-to-analog converter output 1.
			I	**AD13 —** ADC1 channel 3 analog input.
P0.5/ CMPREF/ KBI5	22	18	I/O	**P0.5 —** Port 0 bit 5.
			I	**CMPREF —** Comparator reference (negative) input.
			I	**KBI5 —** Keyboard input 5.
P0.6/CMP1/ KBI6	20	16	I/O	**P0.6 —** Port 0 bit 6.
			O	**CMP1 —** Comparator 1 output.
			I	**KBI6 —** Keyboard input 6.
P0.7/T1/ KBI7	19	15	I/O	**P0.7 —** Port 0 bit 7.
			I/O	**T1 —** Timer/counter 1 external count input or overflow output.
			I	**KBI7 —** Keyboard input 7.

Table 4. Pin description *…continued*

Symbol	Pin		Type	Description
	TSSOP28, PLCC28	HVQFN28		
P1.0 to P1.7			I/O, I [1]	**Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.13.1 "Port configurations" and Table 11 "Static characteristics" for details. P1.2 and P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt trigger inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	18	14	I/O	**P1.0 —** Port 1 bit 0.
			O	**TXD —** Transmitter output for the serial port.
P1.1/RXD	17	13	I/O	**P1.1 —** Port 1 bit 1.
			I	**RXD —** Receiver input for the serial port.
P1.2/T0/SCL	12	8	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
			I/O	**T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output).
			I/O	**SCL —** I^2C serial clock input/output.
P1.3/$\overline{\text{INT0}}$/SDA	11	7	I/O	**P1.3 —** Port 1 bit 3 (open-drain when used as output).
			I	**$\overline{\text{INT0}}$ —** External interrupt 0 input.
			I/O	**SDA —** I^2C serial data input/output.
P1.4/$\overline{\text{INT1}}$	10	6	I	**P1.4 —** Port 1 bit 4.
			I	**$\overline{\text{INT1}}$ —** External interrupt 1 input.
P1.5/$\overline{\text{RST}}$	6	2	I	**P1.5 —** Port 1 bit 5 (input only).
			I	**$\overline{\text{RST}}$ —** External reset input during power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until VDD has reached its specified level. When system power is removed VDD will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when VDD falls below the minimum specified operating voltage.**
P1.6/OCB	5	1	I/O	**P1.6 —** Port 1 bit 6.
			O	**OCB —** Output Compare B. (P89LPC935/936)
P1.7/OCC/AD00	4	28	I/O	**P1.7 —** Port 1 bit 7.
			O	**OCC —** Output Compare C. (P89LPC935/936)
			I	**AD00 —** ADC0 channel 0 analog input. (P89LPC935/936)

Table 5. Special function registers - P89LPC933/934 *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses		Reset value	
			MSB	LSB	Hex	Binary
WDL	Watchdog load	C1H			FF	1111 1111
WFEED1	Watchdog feed 1	C2H				
WFEED2	Watchdog feed 2	C3H				

[1] Unimplemented bits in SFRs (labeled '-') are X (unknown) at all times. Unless otherwise specified, ones should not be written to these bits since they may be used for other purposes in future derivatives. The reset values shown for these bits are logic 0s although they are unknown when read.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.

[3] All ports are in input only (high-impedance) state after power-up.

[4] The RSTSRC register reflects the cause of the P89LPC933/934/935/936 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx11 0000.

[5] The only reset source that affects these SFRs is power-on reset.

[6] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[7] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

Table 6. Special function registers - P89LPC935/936

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		**E7**	**E6**	**E5**	**E4**	**E3**	**E2**	**E1**	**E0**		
ACC*	Accumulator	E0H									00	0000 0000
ADCON0	A/D control register 0	8EH	ENBI0	ENADCI 0	TMM0	EDGE0	ADCI0	ENADC0	ADCS01	ADCS00	00	0000 0000
ADCON1	A/D control register 1	97H	ENBI1	ENADCI 1	TMM1	EDGE1	ADCI1	ENADC1	ADCS11	ADCS10	00	0000 0000
ADINS	A/D input select	A3H	ADI13	ADI12	ADI11	ADI10	ADI03	ADI02	ADI01	ADI00	00	0000 0000
ADMODA	A/D mode register A	C0H	BNDI1	BURST1	SCC1	SCAN1	BNDI0	BURST0	SCC0	SCAN0	00	0000 0000
ADMODB	A/D mode register B	A1H	CLK2	CLK1	CLK0	-	ENDAC1	ENDAC0	BSA1	BSA0	00	000x 0000
AD0BH	A/D_0 boundary high register	BBH									FF	1111 1111
AD0BL	A/D_0 boundary low register	A6H									00	0000 0000
AD0DAT0	A/D_0 data register 0	C5H									00	0000 0000
AD0DAT1	A/D_0 data register 1	C6H									00	0000 0000
AD0DAT2	A/D_0 data register 2	C7H									00	0000 0000
AD0DAT3	A/D_0 data register 3	F4H									00	0000 0000
AD1BH	A/D_1 boundary high register	C4H									FF	1111 1111
AD1BL	A/D_1 boundary low register	BCH									00	0000 0000
AD1DAT0	A/D_1 data register 0	D5H									00	0000 0000
AD1DAT1	A/D_1 data register 1	D6H									00	0000 0000
AD1DAT2	A/D_1 data register 2	D7H									00	0000 0000
AD1DAT3	A/D_1 data register 3	F5H									00	0000 0000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS	00	0000 00x0
	Bit address		**F7**	**F6**	**F5**	**F4**	**F3**	**F2**	**F1**	**F0**		
B*	B register	F0H									00	0000 0000
BRGR0[2]	Baud rate generator rate low	BEH									00	0000 0000
BRGR1[2]	Baud rate generator rate high	BFH									00	0000 0000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[2]	xxxx xx00
CCCRA	Capture compare A control register	EAH	ICECA2	ICECA1	ICECA0	ICESA	ICNFA	FCOA	OCMA1	OCMA0	00	0000 0000

Table 6. Special function registers - P89LPC935/936 *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
CCCRB	Capture compare B control register	EBH	ICECB2	ICECB1	ICECB0	ICESB	ICNFB	FCOB	OCMB1	OCMB0	00	0000 0000
CCCRC	Capture compare C control register	ECH	-	-	-	-	-	FCOC	OCMC1	OCMC0	00	xxxx x000
CCCRD	Capture compare D control register	EDH	-	-	-	-	-	FCOD	OCMD1	OCMD0	00	xxxx x000
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	OE1	CO1	CMF1	00[3]	xx00 0000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00[3]	xx00 0000
DEECON	Data EEPROM control register	F1H	EEIF	HVERR	ECTL1	ECTL0	-	-	-	EADR8	0E	0000 1110
DEEDAT	Data EEPROM data register	F2H									00	0000 0000
DEEADR	Data EEPROM address register	F3H									00	0000 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H									00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)	E4H	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program flash data	E5H									00	0000 0000
I2ADR	I^2C slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	0000 0000
	Bit address		**DF**	**DE**	**DD**	**DC**	**DB**	**DA**	**D9**	**D8**		
I2CON*	I^2C control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x000 00x0
I2DAT	I^2C data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH									00	0000 0000

Table 6. Special function registers - P89LPC935/936 *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
OCRCH	Output compare C register high	FDH									00	0000 0000
OCRCL	Output compare C register low	FCH									00	0000 0000
OCRDH	Output compare D register high	FFH									00	0000 0000
OCRDL	Output compare D register low	FEH									00	0000 0000
	Bit address		**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		
P0*	Port 0	80H	T1/KB7	CMP1 /KB6	CMPREF /KB5	CIN1A /KB4	CIN1B /KB3	CIN2A /KB2	CIN2B /KB1	CMP2 /KB0		[3]
	Bit address		**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P1*	Port 1	90H	OCC	OCB	$\overline{\text{RST}}$	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$/ SDA	T0/SCL	RXD	TXD		[3]
	Bit address		**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**		
P2*	Port 2	A0H	ICA	OCA	SPICLK	$\overline{\text{SS}}$	MISO	MOSI	OCD	ICB		[3]
	Bit address		**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
P3*	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2		[3]
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF[3]	1111 1111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00[3]	0000 0000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[3]	11x1 xx11
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[3]	00x0 xx00
P2M1	Port 2 output mode 1	A4H	(P2M1.7)	(P2M1.6)	(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)	(P2M1.1)	(P2M1.0)	FF[3]	1111 1111
P2M2	Port 2 output mode 2	A5H	(P2M2.7)	(P2M2.6)	(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)	(P2M2.1)	(P2M2.0)	00[3]	0000 0000
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03[3]	xxxx xx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00[3]	xxxx xx00
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	DEEPD	VCPD	ADPD	I2PD	SPPD	SPD	CCUPD	00[3]	0000 0000
	Bit address		**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x

Table 6. Special function registers - P89LPC935/936 *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX		[4]
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[3][5]	011x xx00
RTCH	Real-time clock register high	D2H									00[5]	0000 0000
RTCL	Real-time clock register low	D3H									00[5]	0000 0000
SADDR	Serial port address register	A9H									00	0000 0000
SADEN	Serial port address enable	B9H									00	0000 0000
SBUF	Serial Port data buffer register	99H									xx	xxxx xxxx
	Bit address		**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	0000 0000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	0000 0100
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xx xxxx
SPDAT	SPI data register	E3H									00	0000 0000
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0 xxx0
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	0000 0000
TCR20*	CCU control register 0	C8H	PLEEN	HLTRN	HLTEN	ALTCD	ALTAB	TDIR2	TMOD21	TMOD20	00	0000 0000
TCR21	CCU control register 1	F9H	TCOU2	-	-	-	PLLDV.3	PLLDV.2	PLLDV.1	PLLDV.0	00	0xxx 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TH2	CCU timer high	CDH									00	0000 0000
TICR2	CCU interrupt control register	C9H	TOIE2	TOCIE2D	TOCIE2C	TOCIE2B	TOCIE2A	-	TICIE2B	TICIE2A	00	0000 0x00
TIFR2	CCU interrupt flag register	E9H	TOIF2	TOCF2D	TOCF2C	TOCF2B	TOCF2A	-	TICF2B	TICF2A	00	0000 0x00
TISE2	CCU interrupt status encode register	DEH	-	-	-	-	-	ENCINT.2	ENCINT.1	ENCINT.0	00	xxxx x000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000

8.13 I/O ports

The P89LPC933/934/935/936 has four I/O ports: Port 0, Port 1, Port 2, and Port 3. Ports 0, 1 and 2 are 8-bit ports, and Port 3 is a 2-bit port. The exact number of I/O pins available depends upon the clock and reset options chosen, as shown in Table 8.

Table 8. Number of I/O pins available

Clock source	Reset option	Number of I/O pins (28-pin package)
On-chip oscillator or watchdog oscillator	No external reset (except during power-up)	26
	External $\overline{\text{RST}}$ pin supported	25
External clock input	No external reset (except during power-up)	25
	External $\overline{\text{RST}}$ pin supported[1]	24
Low/medium/high speed oscillator (external crystal or resonator)	No external reset (except during power-up)	24
	External $\overline{\text{RST}}$ pin supported[1]	23

[1] Required for operation above 12 MHz.

8.13.1 Port configurations

All but three I/O port pins on the P89LPC933/934/935/936 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

1. P1.5 ($\overline{\text{RST}}$) can only be an input and cannot be configured.
2. P1.2 (SCL/T0) and P1.3 (SDA/$\overline{\text{INT0}}$) may only be configured to be either input-only or open-drain.

8.13.1.1 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC933/934/935/936 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt trigger input that also has a glitch suppression circuit.

8.13.1.2 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

8.15.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the RTC running during power-down.

8.16 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either a LOW-active reset input or as a digital input, P1.5. The Reset Pin Enable (RPE) bit in UCFG1, when set to logic 1, enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, the RPE selection is overridden and this pin will always functions as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this input will function either as an external reset input or as a digital input as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit. When this pin functions as a reset input, an internal pull-up resistance is connected (see Table 11 “Static characteristics”).

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1).
- Power-on detect.
- Brownout detect.
- Watchdog timer.
- Software reset.
- UART break character detect reset.

For every reset source, there is a flag in the reset register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a logic 0 to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

8.16.1 Reset vector

Following reset, the P89LPC933/934/935/936 will fetch instructions from either address 0000H or the boot address. The boot address is formed by using the boot vector as the high byte of the address and the low byte of the address = 00H.

The boot address will be used if a UART break reset occurs, or the non-volatile boot status bit (BOOTSTAT.0) = 1, or the device is forced into ISP mode during power-on (see P89LPC933/934/935/936 *User manual*). Otherwise, instructions will be fetched from address 0000H.

Capture Noise Filter bit. If set, the capture logic needs to see four consecutive samples of the same value in order to recognize an edge as a capture event. An event counter can be set to delay a capture by a number of capture events.

8.19.6 PWM operation

PWM operation has two main modes, symmetrical and asymmetrical.

In asymmetrical PWM operation the CCU timer operates in down-counting mode regardless of the direction control bit.

In symmetrical mode, the timer counts up/down alternately. The main difference from basic timer operation is the operation of the compare module, which in PWM mode is used for PWM waveform generation.

As with basic timer operation, when the PWM (compare) pins are connected to the compare logic, their logic state remains unchanged. However, since bit FCO is used to hold the halt value, only a compare event can change the state of the pin.

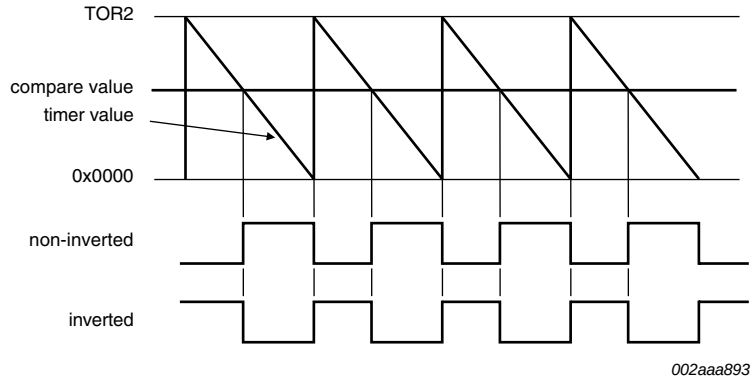

Fig 10. Asymmetrical PWM, down-counting mode

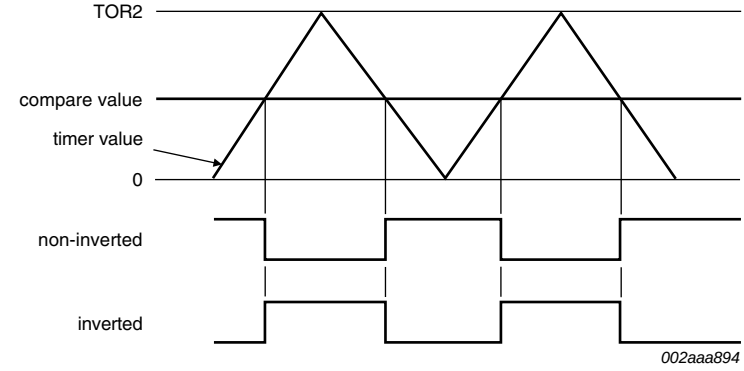

Fig 11. Symmetrical PWM

8.19.7 Alternating output mode

In asymmetrical mode, the user can set up PWM channels A/B and C/D as alternating pairs for bridge drive control. In this mode the output of these PWM channels are alternately gated on every counter cycle.

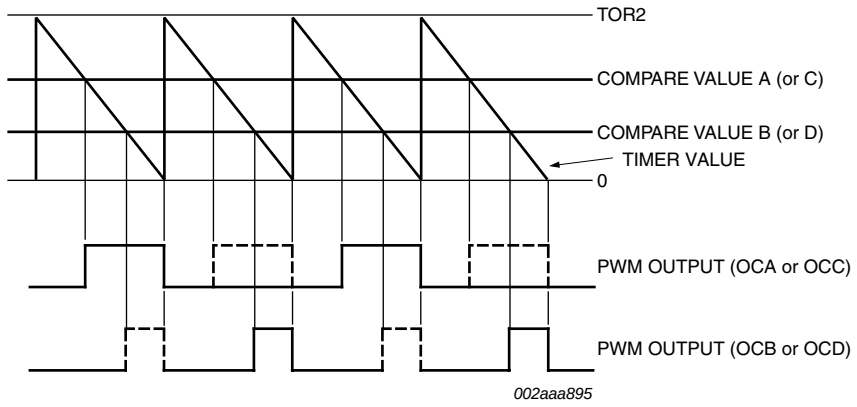

Fig 12. Alternate output mode

8.19.8 PLL operation

The PWM module features a PLL that can be used to generate a CCUCLK frequency between 16 MHz and 32 MHz. At this frequency the PWM module provides ultrasonic PWM frequency with 10-bit resolution provided that the crystal frequency is 1 MHz or higher. The PLL is fed an input signal from 0.5 MHz to 1 MHz and generates an output signal of 32 times the input frequency. This signal is used to clock the timer. The user will have to set a divider that scales PCLK by a factor from 1 to 16. This divider is found in the SFR register TCR21. The PLL frequency can be expressed as shown in Equation 1.

$$\text{PLL frequency} = \frac{\text{PCLK}}{(N+1)} \quad (1)$$

Where: N is the value of PLLDV.3 to PLLDV.0.

Since N ranges from 0 to 15, the CCLK frequency can be in the range of PCLK to $^{PCLK}/_{16}$.

8.19.9 CCU interrupts

There are seven interrupt sources on the CCU which share a common interrupt vector.

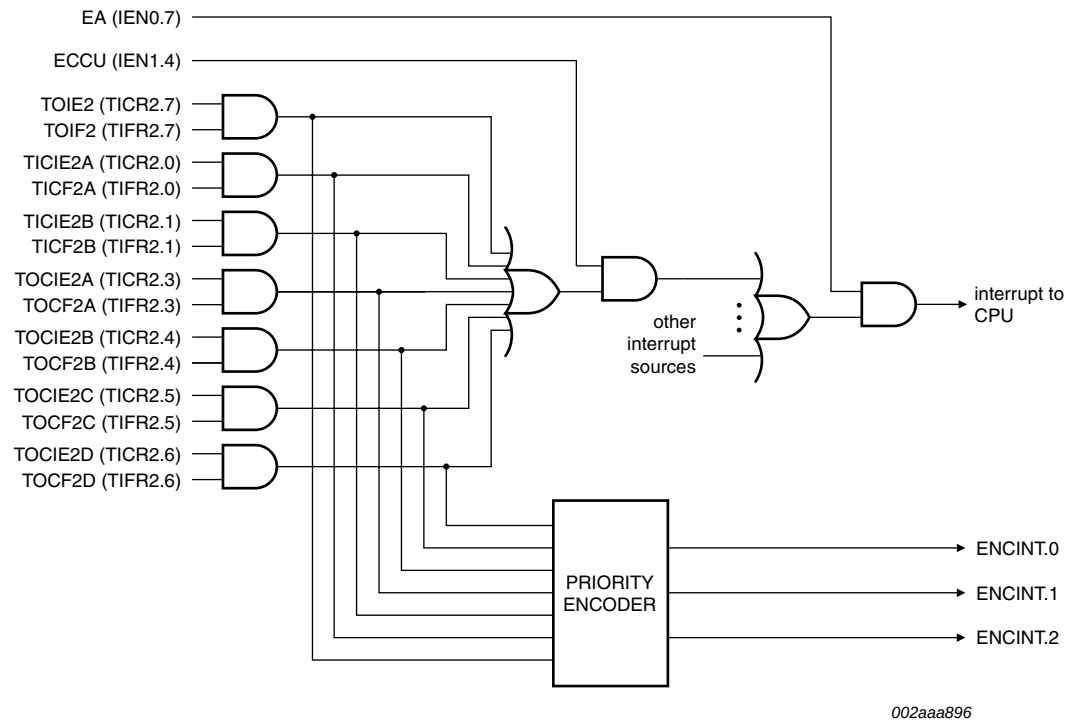

Fig 13. Capture/compare unit interrupts

8.20 UART

The P89LPC933/934/935/936 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC933/934/935/936 does include an independent baud rate generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent baud rate generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in four modes: shift register, 8-bit UART, 9-bit UART, and CPU $^{clock}/_{32}$ or CPU $^{clock}/_{16}$.

8.20.1 Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $^{1}/_{16}$ of the CPU clock frequency.

8.21 I²C-bus serial interface

The I²C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between masters and slaves
- Multi master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I²C-bus may be used for test and diagnostic purposes.

A typical I²C-bus configuration is shown in Figure 15. The P89LPC933/934/935/936 device provides a byte-oriented I²C-bus interface that supports data transfers up to 400 kHz.

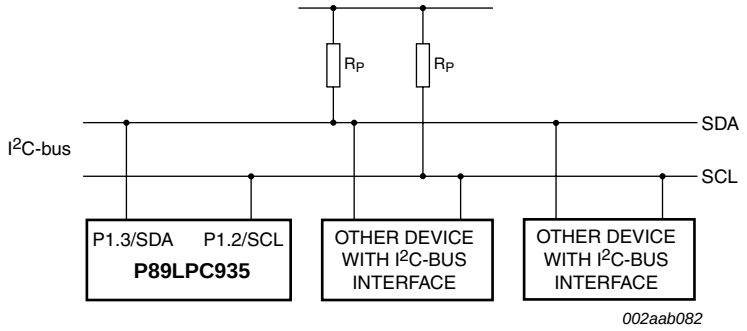

Fig 15. I²C-bus configuration

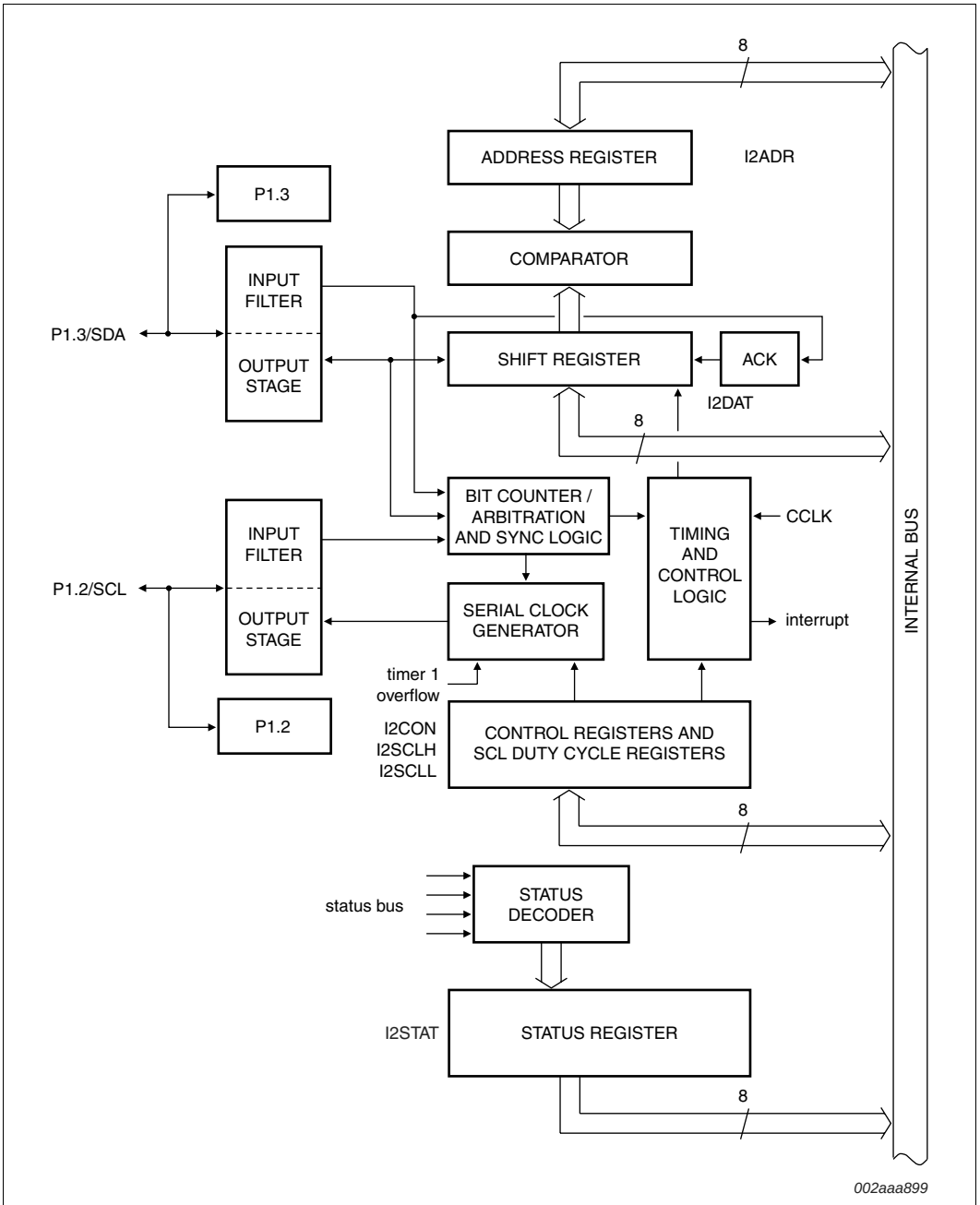

Fig 16. I²C-bus serial interface block diagram

8.27 Data EEPROM (P89LPC935/936)

The P89LPC935/936 has 512 bytes of on-chip Data EEPROM. The Data EEPROM is SFR based, byte readable, byte writable, and erasable (via row fill and sector fill). The user can read, write and fill the memory via SFRs and one interrupt. This Data EEPROM provides 100,000 minimum erase/program cycles for each byte.

- **Byte mode:** In this mode, data can be read and written one byte at a time.
- **Row fill:** In this mode, the addressed row (64 bytes) is filled with a single value. The entire row can be erased by writing 00H.
- **Sector fill:** In this mode, all 512 bytes are filled with a single value. The entire sector can be erased by writing 00H.

After the operation finishes, the hardware will set the EEIF bit, which if enabled will generate an interrupt. The flag is cleared by software.

8.28 Flash program memory

8.28.1 General description

The P89LPC933/934/935/936 flash memory provides in-circuit electrical erasure and programming. The flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any flash sector (1 kB or 2 kB depending on the device) or page (64 bytes). The Chip Erase operation will erase the entire program memory. ICP using standard commercial programmers is available. In addition, IAP and byte-erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC933/934/935/936 flash reliably stores memory contents even after 100,000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC933/934/935/936 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

8.28.2 Features

- Programming and erase over the full operating voltage range.
- Byte erase allows code memory to be used for data storage.
- Read/Programming/Erase using ISP/IAP/ICP.
- Internal fixed boot ROM, containing low-level IAP routines available to user code.
- Default loader providing ISP via the serial port, located in upper end of user program memory.
- Boot vector allows user-provided flash loader code to reside anywhere in the flash memory space, providing flexibility to the user.
- Any flash program/erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the flash for each sector.
- 100,000 typical erase/program cycles for each byte.
- 10 year minimum data retention.

12. Dynamic characteristics

Table 12. Dynamic characteristics (12 MHz)

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency		7.189	7.557	7.189	7.557	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency		320	520	320	520	kHz
f_{osc}	oscillator frequency		0	12	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 27	83	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection time	P1.5/$\overline{RST}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$	-	15	-	15	ns
t_{sa}	signal acceptance time	P1.5/$\overline{RST}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$	50	-	50	-	ns
External clock							
t_{CHCX}	clock HIGH time	see Figure 27	33	$T_{cy(CLK)} - t_{CLCX}$	33	-	ns
t_{CLCX}	clock LOW time	see Figure 27	33	$T_{cy(CLK)} - t_{CHCX}$	33	-	ns
t_{CLCH}	clock rise time	see Figure 27	-	8	-	8	ns
t_{CHCL}	clock fall time	see Figure 27	-	8	-	8	ns
Shift register (UART mode 0)							
T_{XLXL}	serial port clock cycle time	see Figure 25	$16T_{cy(CLK)}$	-	1333	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 25	$13T_{cy(CLK)}$	-	1083	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 25	-	$T_{cy(CLK)}$ + 20	-	103	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 25	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 25	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	slave		0	$^{CCLK}/_{6}$	0	2.0	MHz
	master		-	$^{CCLK}/_{4}$	-	3.0	MHz
T_{SPICYC}	SPI cycle time	see Figure 26, 28, 29, 30					
	slave		$^{6}/_{CCLK}$	-	500	-	ns
	master		$^{4}/_{CCLK}$	-	333	-	ns
$t_{SPILEAD}$	SPI enable lead time	see Figure 29, 30					
	slave		250	-	250	-	ns

Table 12. Dynamic characteristics (12 MHz) *…continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
t_{SPILAG}	SPI enable lag time	see Figure 29, 30					
	slave		250	-	250	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 26, 28, 29, 30					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 26, 28, 29, 30					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 26, 28, 29, 30					
	master or slave		100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 26, 28, 29, 30					
	master or slave		100	-	100	-	ns
t_{SPIA}	SPI access time	see Figure 29, 30					
	slave		0	120	0	120	ns
t_{SPIDIS}	SPI disable time	see Figure 29, 30					
	slave		0	240	-	240	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 26, 28, 29, 30					
	slave		-	240	-	240	ns
	master		-	167	-	167	ns
t_{SPIOH}	SPI output data hold time	see Figure 26, 28, 29, 30	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 26, 28, 29, 30					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 26, 28, 29, 30					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over ambient temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

13. Other characteristics

13.1 Comparator electrical characteristics

Table 15. Comparator electrical characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IO}	input offset voltage		-	-	±20	mV
V_{IC}	common-mode input voltage		0	-	V_{DD} − 0.3	V
CMRR	common-mode rejection ratio	[1]	-	-	−50	dB
$t_{res(tot)}$	total response time		-	250	500	ns
$t_{(CE-OV)}$	chip enable to output valid time		-	-	10	μs
I_{LI}	input leakage current	$0 < V_I < V_{DD}$	-	-	±10	μA

[1] This parameter is characterized, but not tested in production.

15. Abbreviations

Table 17. Acronym list

Acronym	Description
A/D	Analog to Digital
CPU	Central Processing Unit
DAC	Digital to Analog Converter
EPROM	Erasable Programmable Read-Only Memory
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Electro-Magnetic Interference
LED	Light Emitting Diode
PWM	Pulse Width Modulator
RAM	Random Access Memory
RC	Resistance-Capacitance
RTC	Real-Time Clock
SAR	Successive Approximation Register
SFR	Special Function Register
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter