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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	26
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x8b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	28-PLCC (11.48x11.48)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc936fa-529

6. Pinning information

6.1 Pinning

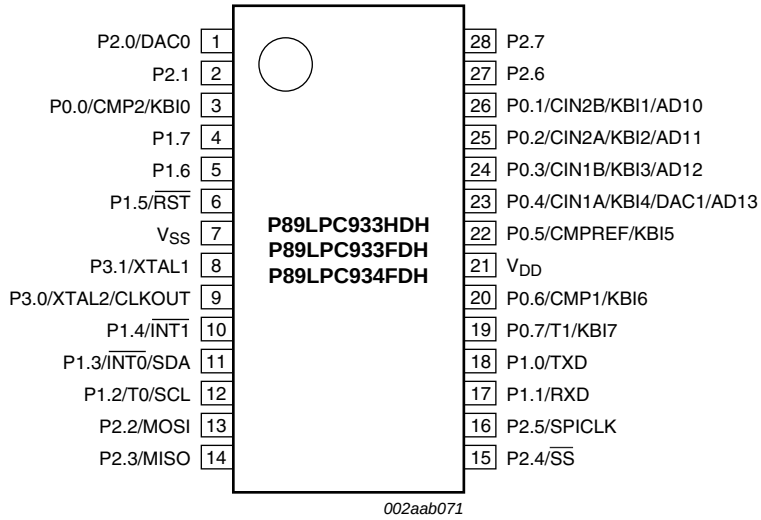


Fig 2. P89LPC933/934 TSSOP28 pin configuration

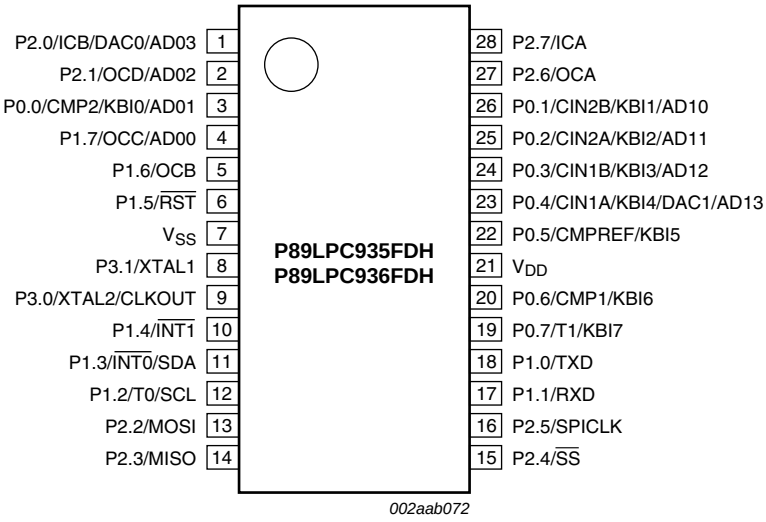


Fig 3. P89LPC935/936 TSSOP28 pin configuration

Table 4. Pin description *…continued*

Symbol	Pin		Type	Description
	TSSOP28, PLCC28	HVQFN28		
P2.0 to P2.7			I/O	**Port 2:** Port 2 is an 8-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.13.1 “Port configurations” and Table 11 “Static characteristics” for details. All pins have Schmitt trigger inputs. Port 2 also provides various special functions as described below:
P2.0/ICB/ DAC0/AD03	1	25	I/O	**P2.0 —** Port 2 bit 0.
			I	**ICB —** Input Capture B. (P89LPC935/936)
			I	**DAC0 —** Digital-to-analog converter output.
			I	**AD03 —** ADC0 channel 3 analog input. (P89LPC935/936)
P2.1/OCD/ AD02	2	26	I/O	**P2.1 —** Port 2 bit 1.
			O	**OCD —** Output Compare D. (P89LPC935/936)
			I	**AD02 —** ADC0 channel 2 analog input. (P89LPC935/936)
P2.2/MOSI	13	9	I/O	**P2.2 —** Port 2 bit 2.
			I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.3/MISO	14	10	I/O	**P2.3 —** Port 2 bit 3.
			I/O	**MISO —** When configured as master, this pin is input, when configured as slave, this pin is output.
P2.4/$\overline{SS}$	15	11	I/O	**P2.4 —** Port 2 bit 4.
			I	**$\overline{SS}$ —** SPI Slave select.
P2.5/ SPICLK	16	12	I/O	**P2.5 —** Port 2 bit 5.
			I/O	**SPICLK —** SPI clock. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.6/OCA	27	23	I/O	**P2.6 —** Port 2 bit 6.
			O	**OCA —** Output Compare A. (P89LPC935/936)
P2.7/ICA	28	24	I/O	**P2.7 —** Port 2 bit 7.
			I	**ICA —** Input Capture A. (P89LPC935/936)

Table 5. Special function registers - P89LPC933/934 *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
RTCH	Real-time clock register high	D2H									00[5]	0000 0000
RTCL	Real-time clock register low	D3H									00[5]	0000 0000
SADDR	Serial port address register	A9H									00	0000 0000
SADEN	Serial port address enable	B9H									00	0000 0000
SBUF	Serial Port data buffer register	99H									xx	xxxx xxxx
	Bit address		**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	0000 0000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	0000 0100
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xx xxxx
SPDAT	SPI data register	E3H									00	0000 0000
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0 xxx0
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	0000 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	0000 0000
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0		[6] [5]
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK		[7] [5]

Table 6. Special function registers - P89LPC935/936

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		**E7**	**E6**	**E5**	**E4**	**E3**	**E2**	**E1**	**E0**		
ACC*	Accumulator	E0H									00	0000 0000
ADCON0	A/D control register 0	8EH	ENBI0	ENADCI 0	TMM0	EDGE0	ADCI0	ENADC0	ADCS01	ADCS00	00	0000 0000
ADCON1	A/D control register 1	97H	ENBI1	ENADCI 1	TMM1	EDGE1	ADCI1	ENADC1	ADCS11	ADCS10	00	0000 0000
ADINS	A/D input select	A3H	ADI13	ADI12	ADI11	ADI10	ADI03	ADI02	ADI01	ADI00	00	0000 0000
ADMODA	A/D mode register A	C0H	BNDI1	BURST1	SCC1	SCAN1	BNDI0	BURST0	SCC0	SCAN0	00	0000 0000
ADMODB	A/D mode register B	A1H	CLK2	CLK1	CLK0	-	ENDAC1	ENDAC0	BSA1	BSA0	00	000x 0000
AD0BH	A/D_0 boundary high register	BBH									FF	1111 1111
AD0BL	A/D_0 boundary low register	A6H									00	0000 0000
AD0DAT0	A/D_0 data register 0	C5H									00	0000 0000
AD0DAT1	A/D_0 data register 1	C6H									00	0000 0000
AD0DAT2	A/D_0 data register 2	C7H									00	0000 0000
AD0DAT3	A/D_0 data register 3	F4H									00	0000 0000
AD1BH	A/D_1 boundary high register	C4H									FF	1111 1111
AD1BL	A/D_1 boundary low register	BCH									00	0000 0000
AD1DAT0	A/D_1 data register 0	D5H									00	0000 0000
AD1DAT1	A/D_1 data register 1	D6H									00	0000 0000
AD1DAT2	A/D_1 data register 2	D7H									00	0000 0000
AD1DAT3	A/D_1 data register 3	F5H									00	0000 0000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS	00	0000 00x0
	Bit address		**F7**	**F6**	**F5**	**F4**	**F3**	**F2**	**F1**	**F0**		
B*	B register	F0H									00	0000 0000
BRGR0[2]	Baud rate generator rate low	BEH									00	0000 0000
BRGR1[2]	Baud rate generator rate high	BFH									00	0000 0000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[2]	xxxx xx00
CCCRA	Capture compare A control register	EAH	ICECA2	ICECA1	ICECA0	ICESA	ICNFA	FCOA	OCMA1	OCMA0	00	0000 0000

Table 6. Special function registers - P89LPC935/936 *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX		[4]
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[3][5]	011x xx00
RTCH	Real-time clock register high	D2H									00[5]	0000 0000
RTCL	Real-time clock register low	D3H									00[5]	0000 0000
SADDR	Serial port address register	A9H									00	0000 0000
SADEN	Serial port address enable	B9H									00	0000 0000
SBUF	Serial Port data buffer register	99H									xx	xxxx xxxx
	Bit address		**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	0000 0000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	0000 0100
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xx xxxx
SPDAT	SPI data register	E3H									00	0000 0000
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0 xxx0
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	0000 0000
TCR20*	CCU control register 0	C8H	PLEEN	HLTRN	HLTEN	ALTCD	ALTAB	TDIR2	TMOD21	TMOD20	00	0000 0000
TCR21	CCU control register 1	F9H	TCOU2	-	-	-	PLLDV.3	PLLDV.2	PLLDV.1	PLLDV.0	00	0xxx 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TH2	CCU timer high	CDH									00	0000 0000
TICR2	CCU interrupt control register	C9H	TOIE2	TOCIE2D	TOCIE2C	TOCIE2B	TOCIE2A	-	TICIE2B	TICIE2A	00	0000 0x00
TIFR2	CCU interrupt flag register	E9H	TOIF2	TOCF2D	TOCF2C	TOCF2B	TOCF2A	-	TICF2B	TICF2A	00	0000 0x00
TISE2	CCU interrupt status encode register	DEH	-	-	-	-	-	ENCINT.2	ENCINT.1	ENCINT.0	00	xxxx x000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000

- CODE

  64 kB of code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC933/934/935/936 have 4 KB/8 kB/16 kB of on-chip Code memory.

The P89LPC935/936 also has 512 bytes of on-chip data EEPROM that is accessed via SFRs (see Section 8.27 “Data EEPROM (P89LPC935/936)”).

8.11 Data RAM arrangement

The 768 bytes of on-chip RAM are organized as shown in Table 7.

Table 7. On-chip data memory usages

Type	Data RAM	Size (bytes)
DATA	Memory that can be addressed directly and indirectly	128
IDATA	Memory that can be addressed indirectly	256
XDATA	Auxiliary (‘External Data’) on-chip memory that is accessed using the MOVX instructions (P89LPC935/936)	512

8.12 Interrupts

The P89LPC933/934/935/936 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC933/934/935/936 supports 15 interrupt sources: external interrupts 0 and 1, timers 0 and 1, serial port Tx, serial port Rx, combined serial port Rx/Tx, brownout detect, watchdog/Real-Time clock, I^2C-bus, keyboard, comparators 1 and 2, SPI, CCU, data EEPROM write/ADC completion.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking.

Remark: The arbitration ranking is only used to resolve pending requests of the same priority level.

8.12.1 External interrupt inputs

The P89LPC933/934/935/936 has two external interrupt inputs as well as the Keypad Interrupt function. The two interrupt inputs are identical to those present on the standard 80C51 microcontrollers.

8.14.1 Brownout detection

The brownout detect function determines if the power supply voltage drops below a certain level. The default operation is for a brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt.

Brownout detection may be enabled or disabled in software.

If brownout detection is enabled the brownout condition occurs when V_{DD} falls below the brownout trip voltage, V_{bo} (see Table 11 “Static characteristics”), and is negated when V_{DD} rises above V_{bo}. If the P89LPC933/934/935/936 device is to operate with a power supply that can be below 2.7 V, BOE should be left in the unprogrammed state so that the device can operate at 2.4 V, otherwise continuous brownout reset may prevent the device from operating.

For correct activation of brownout detect, the V_{DD} rise and fall times must be observed. Please see Table 11 “Static characteristics” for specifications.

8.14.2 Power-on detection

The power-on detect has a function similar to the brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

8.15 Power reduction modes

The P89LPC933/934/935/936 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

8.15.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

8.15.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC933/934/935/936 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the RAM keep-alive voltage V_{RAM}. This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{DDR}, therefore it is highly recommended to wake-up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during power-down. These include: brownout detect, watchdog timer, Comparators (note that Comparators can be powered-down separately), and RTC/system timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock and the RTC is enabled.

8.19.9 CCU interrupts

There are seven interrupt sources on the CCU which share a common interrupt vector.

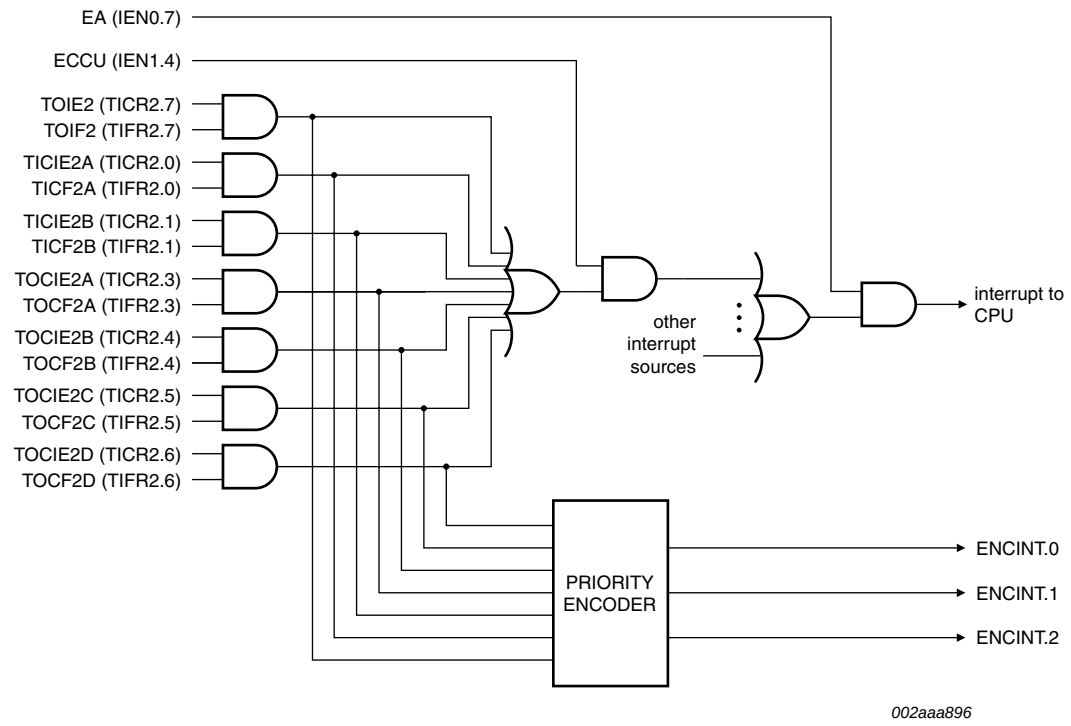


Fig 13. Capture/compare unit interrupts

8.20 UART

The P89LPC933/934/935/936 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC933/934/935/936 does include an independent baud rate generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent baud rate generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in four modes: shift register, 8-bit UART, 9-bit UART, and CPU $^{clock}/_{32}$ or CPU $^{clock}/_{16}$.

8.20.1 Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $^{1}/_{16}$ of the CPU clock frequency.

8.27 Data EEPROM (P89LPC935/936)

The P89LPC935/936 has 512 bytes of on-chip Data EEPROM. The Data EEPROM is SFR based, byte readable, byte writable, and erasable (via row fill and sector fill). The user can read, write and fill the memory via SFRs and one interrupt. This Data EEPROM provides 100,000 minimum erase/program cycles for each byte.

- **Byte mode:** In this mode, data can be read and written one byte at a time.
- **Row fill:** In this mode, the addressed row (64 bytes) is filled with a single value. The entire row can be erased by writing 00H.
- **Sector fill:** In this mode, all 512 bytes are filled with a single value. The entire sector can be erased by writing 00H.

After the operation finishes, the hardware will set the EEIF bit, which if enabled will generate an interrupt. The flag is cleared by software.

8.28 Flash program memory

8.28.1 General description

The P89LPC933/934/935/936 flash memory provides in-circuit electrical erasure and programming. The flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any flash sector (1 kB or 2 kB depending on the device) or page (64 bytes). The Chip Erase operation will erase the entire program memory. ICP using standard commercial programmers is available. In addition, IAP and byte-erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC933/934/935/936 flash reliably stores memory contents even after 100,000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC933/934/935/936 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

8.28.2 Features

- Programming and erase over the full operating voltage range.
- Byte erase allows code memory to be used for data storage.
- Read/Programming/Erase using ISP/IAP/ICP.
- Internal fixed boot ROM, containing low-level IAP routines available to user code.
- Default loader providing ISP via the serial port, located in upper end of user program memory.
- Boot vector allows user-provided flash loader code to reside anywhere in the flash memory space, providing flexibility to the user.
- Any flash program/erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the flash for each sector.
- 100,000 typical erase/program cycles for each byte.
- 10 year minimum data retention.

8.28.3 Flash organization

The program memory consists of eight 2 kB sectors on the P89LPC936 device, eight 1 kB sectors on the P89LPC934/935 devices, and four 1 kB sectors on the P89LPC933 device. Each sector can be further divided into 64-byte pages. In addition to sector erase, page erase, and byte erase, a 64-byte page register is included which allows from 1 to 64 bytes of a given page to be programmed at the same time, substantially reducing overall programming time.

8.28.4 Using flash as data storage

The flash code memory array of this device supports individual byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

8.28.5 Flash programming and erasing

Four different methods of erasing or programming of the flash are available. The flash may be programmed or erased in the end-user application (IAP) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock - serial data interface. As shipped from the factory, the upper 512 bytes of user code space contains a serial ISP routine allowing the device to be programmed in circuit through the serial port. The flash may also be programmed or erased using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead, this device provides a 32-bit CRC result on either a sector or the entire user code space.

8.28.6 In-circuit programming

ICP is performed without removing the microcontroller from the system. The ICP facility consists of internal hardware resources to facilitate remote programming of the P89LPC933/934/935/936 through a two-wire serial interface. The Philips ICP facility has made ICP in an embedded application—using commercially available programmers—possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the P89LPC933/934/935/936 *User manual*.

8.28.7 In-application programming

IAP is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The Philips IAP has made IAP in an embedded application possible without additional components. Two methods are available to accomplish IAP. A set of predefined IAP functions are provided in a boot ROM and can be called through a common interface, PGM_MTP. Several IAP calls are available for use by an application program to permit selective erasing and programming of flash sectors, pages, security bits, configuration bytes, and device ID. These functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FF03H. The boot ROM occupies the program memory space at the top of the address space from FF00H to FFEFH, thereby not conflicting with the user program memory space.

In addition, IAP operations can be accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the P89LPC933/934/935/936 *User manual*.

8.28.8 ISP

ISP is performed without removing the microcontroller from the system. The ISP facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89LPC933/934/935/936 through the serial port. This firmware is provided by Philips and embedded within each P89LPC933/934/935/936 device. The Philips ISP facility has made ISP in an embedded application possible with a minimum of additional expense in components and circuit board area. The ISP function uses five pins (V_{DD}, V_{SS}, TXD, RXD, and $\overline{RST}$). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature.

8.28.9 Power-on reset code execution

The P89LPC933/934/935/936 contains two special flash elements: the boot vector and the boot status bit. Following reset, the P89LPC933/934/935/936 examines the contents of the boot status bit. If the boot status bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the boot status bit is set to a value other than zero, the contents of the boot vector are used as the high byte of the execution address and the low byte is set to 00H.

Table 9 shows the factory default boot vector settings for these devices.

Remark: These settings are different than the original P89LPC932. Tools designed to support the P89LPC933/934/935/936 should be used to program this device, such as Flash Magic version 1.98, or later.

A factory-provided boot loader is preprogrammed into the address space indicated and uses the indicated boot loader entry point to perform ISP functions. This code can be erased by the user.

Remark: Users who wish to use this loader should take precautions to avoid erasing the sector that contains this boot loader. Instead, the page erase function can be used to erase the pages located in this sector which are not used by the boot loader.

A custom boot loader can be written with the boot vector set to the custom boot loader, if desired.

Table 9. Default boot vector values and ISP entry points

Device	Default boot vector	Default boot loader entry point	Default boot loader code range	Boot sector range
P89LPC933	0FH	0F00H	0E00H to 0FFFH	0C00H to 0FFFH
P89LPC934	1FH	1F00H	1E00H to 1FFFH	1C00H to 1FFFH
P89LPC935	1FH	1F00H	1E00H to 1FFFH	1C00H to 1FFFH
P89LPC936	3FH	3F00H	3E00H to 3FFFH	3C00H to 3FFFH

8.28.10 Hardware activation of the boot loader

The boot loader can also be executed by forcing the device into ISP mode during a power-on sequence (see the P89LPC933/934/935/936 *User manual* for specific information). This has the same effect as having a non-zero status byte. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting for the boot vector is changed, it will no longer point to the factory preprogrammed ISP boot loader code. After programming the flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

8.29 User configuration bytes

Some user-configurable features of the P89LPC933/934/935/936 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1. Please see the P89LPC933/934/935/936 *User manual* for additional details.

8.30 User sector security bytes

There are eight User Sector Security Bytes on the P89LPC933/934/935/936 device. Each byte corresponds to one sector. Please see the P89LPC933/934/935/936 *User manual* for additional details.

9. A/D converter

9.1 General description

The P89LPC935/936 have two 8-bit, 4-channel multiplexed successive approximation analog-to-digital converter modules sharing common control logic. The P89LPC933/934 have a single 8-bit, 4-channel multiplexed analog-to-digital converter and an additional DAC module. A block diagram of the A/D converter is shown in Figure 23. Each A/D consists of a 4-input multiplexer which feeds a sample-and-hold circuit providing an input signal to one of two comparator inputs. The control logic in combination with the SAR drives a digital-to-analog converter which provides the other input to the comparator. The output of the comparator is fed to the SAR.

9.2 Features and benefits

- Two (P89LPC935/936) 8-bit, 4-channel multiplexed input, successive approximation A/D converters with common control logic (one A/D on the P89LPC933/934).
- Four result registers for each A/D.
- Six operating modes:
  - Fixed channel, single conversion mode.
  - Fixed channel, continuous conversion mode.
  - Auto scan, single conversion mode.
  - Auto scan, continuous conversion mode.
  - Dual channel, continuous conversion mode.
  - Single step mode.
- Four conversion start modes:
  - Timer triggered start.

9.4.2 Fixed channel, continuous conversion mode

A single input channel can be selected for continuous conversion. The results of the conversions will be sequentially placed in the four result registers. An interrupt, if enabled, will be generated after every four conversions. Additional conversion results will again cycle through the four result registers, overwriting the previous results. Continuous conversions continue until terminated by the user.

9.4.3 Auto scan, single conversion mode

Any combination of the four input channels can be selected for conversion. A single conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. If only a single channel is selected this is equivalent to single channel, single conversion mode.

9.4.4 Auto scan, continuous conversion mode

Any combination of the four input channels can be selected for conversion. A conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. The process will repeat starting with the first selected channel. Additional conversion results will again cycle through the four result registers, overwriting the previous results. Continuous conversions continue until terminated by the user.

9.4.5 Dual channel, continuous conversion mode

This is a variation of the auto scan continuous conversion mode where conversion occurs on two user-selectable inputs. The result of the conversion of the first channel is placed in result register, ADxDAT0. The result of the conversion of the second channel is placed in result register, ADxDAT1. The first channel is again converted and its result stored in ADxDAT2. The second channel is again converted and its result placed in ADxDAT3. An interrupt is generated, if enabled, after every set of four conversions (two conversions per channel).

9.4.6 Single step mode

This special mode allows ‘single-stepping’ in an auto scan conversion mode. Any combination of the four input channels can be selected for conversion. After each channel is converted, an interrupt is generated, if enabled, and the A/D waits for the next start condition. May be used with any of the start modes.

9.5 Conversion start modes

9.5.1 Timer triggered start

An A/D conversion is started by the overflow of Timer 0. Once a conversion has started, additional Timer 0 triggers are ignored until the conversion has completed. The Timer triggered start mode is available in all A/D operating modes.

9.5.2 Start immediately

Programming this mode immediately starts a conversion. This start mode is available in all A/D operating modes.

9.5.3 Edge triggered

An A/D conversion is started by rising or falling edge of P1.4. Once a conversion has started, additional edge triggers are ignored until the conversion has completed. The edge triggered start mode is available in all A/D operating modes.

9.5.4 Dual start immediately (P89LPC935/936)

Programming this mode starts a synchronized conversion of both A/D converters. This start mode is available in all A/D operating modes. Both A/D converters must be in the same operating mode. In the continuous conversion modes, both A/D converters must select an identical number of channels. Any trigger of either A/D will start a simultaneous conversion of both A/Ds.

9.6 Boundary limits interrupt

Each of the A/D converters has both a high and low boundary limit register. After the four MSBs have been converted, these four bits are compared with the four MSBs of the boundary high and low registers. If the four MSBs of the conversion are outside the limit an interrupt will be generated, if enabled. If the conversion result is within the limits, the boundary limits will again be compared after all 8 bits have been converted. An interrupt will be generated, if enabled, if the result is outside the boundary limits. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

9.7 DAC output to a port pin with high output impedance

Each A/D converter’s DAC block can be output to a port pin. In this mode, the ADxDAT3 register is used to hold the value fed to the DAC. After a value has been written to the DAC (written to ADxDAT3), the DAC output will appear on the channel 3 pin.

9.8 Clock divider

The A/D converter requires that its internal clock source be in the range of 500 kHz to 3.3 MHz to maintain accuracy. A programmable clock divider that divides the clock from 1 to 8 is provided for this purpose.

9.9 Power-down and Idle mode

In Idle mode the A/C converter, if enabled, will continue to function and can cause the device to exit Idle mode when the conversion is completed if the A/D interrupt is enabled. In Power-down mode or Total Power-down mode, the A/D does not function. If the A/D is enabled, it will consume power. Power can be reduced by disabling the A/D.

11. Static characteristics

Table 11. Static characteristics

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(oper)}$	operating supply current	V_{DD} = 3.6 V; f_{osc} = 12 MHz	[2]	-	11	18	mA
		V_{DD} = 3.6 V; f_{osc} = 18 MHz	[2]	-	14	23	mA
$I_{DD(idle)}$	Idle mode supply current	V_{DD} = 3.6 V; f_{osc} = 12 MHz	[2]	-	3.25	5	mA
		V_{DD} = 3.6 V; f_{osc} = 18 MHz	[2]	-	5	7	mA
$I_{DD(pd)}$	Power-down mode supply current	V_{DD} = 3.6 V; voltage comparators powered down	[2]	-	55	80	μA
$I_{DD(tpd)}$	total Power-down mode supply current	all devices except P89LPC933HDH; V_{DD} = 3.6 V	[3]	-	1	5	μA
		P89LPC933HDH only; V_{DD} = 3.6 V	[3]	-	-	25	μA
$(dV/dt)_r$	rise rate	of V_{DD}		-	-	2	mV/μs
$(dV/dt)_f$	fall rate	of V_{DD}		-	-	50	mV/μs
V_{POR}	power-on reset voltage			-	-	0.5	V
V_{DDR}	data retention supply voltage			1.5	-	-	V
$V_{th(HL)}$	HIGH-LOW threshold voltage	except SCL, SDA		$0.22V_{DD}$	$0.4V_{DD}$	-	V
V_{IL}	LOW-level input voltage	SCL, SDA only		−0.5	-	$0.3V_{DD}$	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	except SCL, SDA		-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{IH}	HIGH-level input voltage	SCL, SDA only		$0.7V_{DD}$	-	5.5	V
V_{hys}	hysteresis voltage	port 1		-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 20 mA; V_{DD} = 2.4 V to 3.6 V all ports, all modes except high-Z	[4]	-	0.6	1.0	V
		I_{OL} = 3.2 mA; V_{DD} = 2.4 V to 3.6 V all ports, all modes except high-Z		-	0.2	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = −20 μA; V_{DD} = 2.4 V to 3.6 V; all ports, quasi-bidirectional mode		V_{DD} − 0.3	V_{DD} − 0.2	-	V
		I_{OH} = −3.2 mA; V_{DD} = 2.4 V to 3.6 V; all ports, push-pull mode		V_{DD} − 0.7	V_{DD} − 0.4	-	V
		I_{OH} = −10 mA; V_{DD} = 3.6 V; all ports, push-pull mode		-	3.2	-	V
V_{xtal}	crystal voltage	on XTAL1, XTAL2 pins; with respect to V_{SS}		−0.5	-	+4.0	V
V_n	voltage on any other pin	except XTAL1, XTAL2, V_{DD}; with respect to V_{SS}	[5]	−0.5	-	+5.5	V
C_{iss}	input capacitance		[6]	-	-	15	pF

Table 12. Dynamic characteristics (12 MHz) *…continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
t_{SPILAG}	SPI enable lag time	see Figure 29, 30					
	slave		250	-	250	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 26, 28, 29, 30					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 26, 28, 29, 30					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 26, 28, 29, 30					
	master or slave		100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 26, 28, 29, 30					
	master or slave		100	-	100	-	ns
t_{SPIA}	SPI access time	see Figure 29, 30					
	slave		0	120	0	120	ns
t_{SPIDIS}	SPI disable time	see Figure 29, 30					
	slave		0	240	-	240	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 26, 28, 29, 30					
	slave		-	240	-	240	ns
	master		-	167	-	167	ns
t_{SPIOH}	SPI output data hold time	see Figure 26, 28, 29, 30	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 26, 28, 29, 30					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 26, 28, 29, 30					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over ambient temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

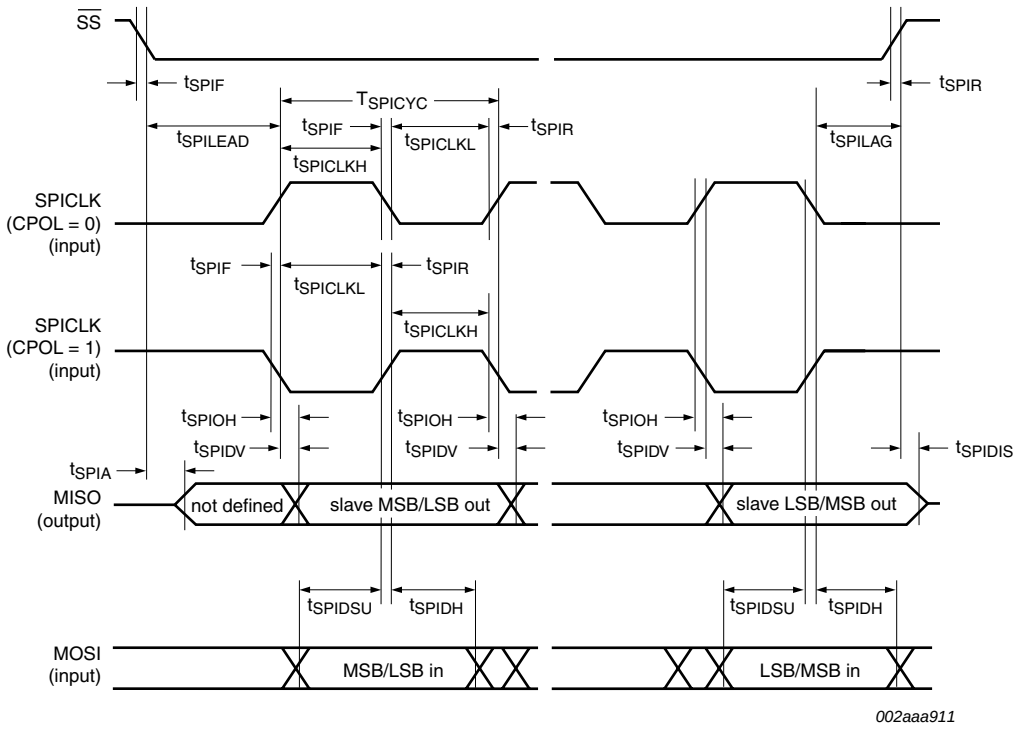


Fig 30. SPI slave timing (CPHA = 1)

12.2 ISP entry mode

Table 14. Dynamic characteristics, ISP entry mode

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VR}	$\overline{RST}$ delay from V_{DD} active time		50	-	-	µs
t_{RH}	$\overline{RST}$ HIGH time		1	-	32	µs
t_{RL}	$\overline{RST}$ LOW time		1	-	-	µs

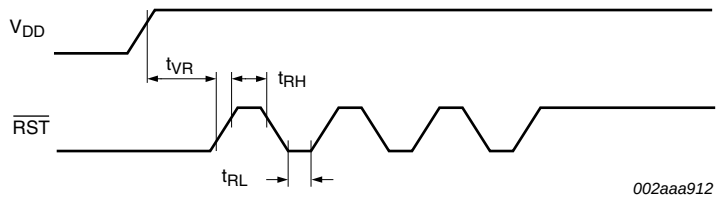


Fig 31. ISP entry timing

13.2 ADC electrical characteristics

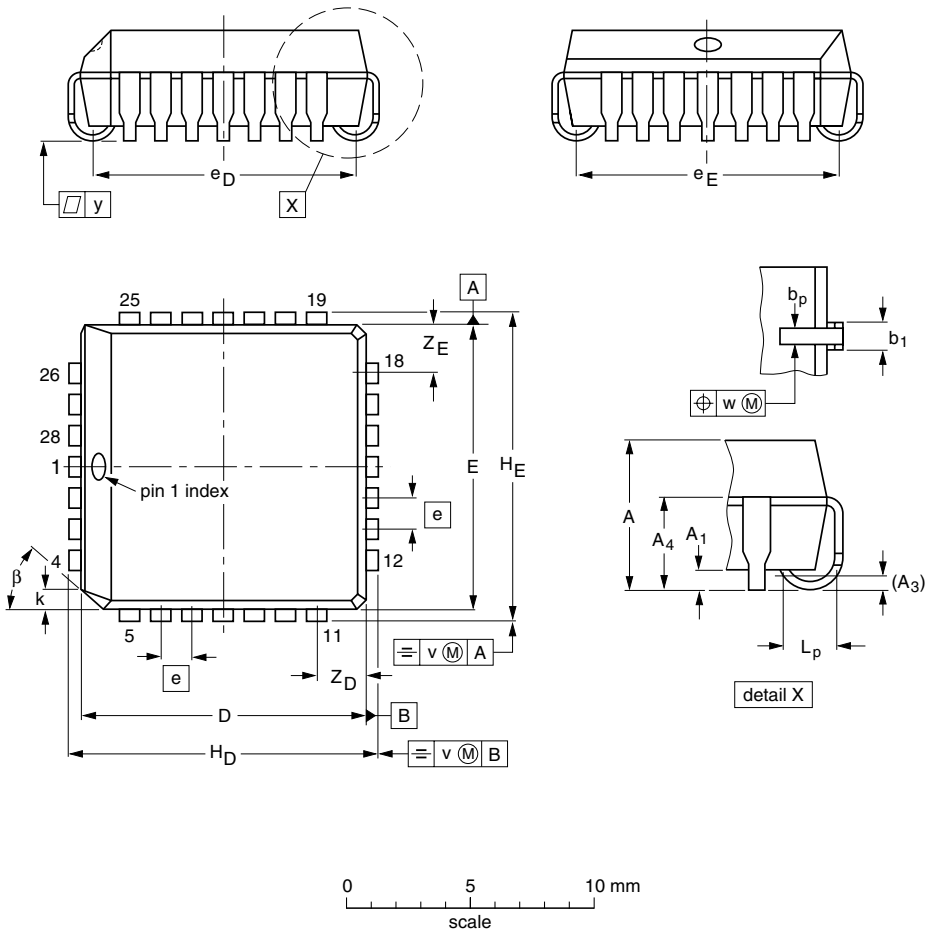
Table 16. ADC electrical characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.
All limits valid for an external source impedance of less than 10 kΩ.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		V_{SS} −0.2	-	V_{DD} +0.2	V
C_{iss}	input capacitance		-	-	15	pF
E_D	differential linearity error		-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		-	-	±1	LSB
E_O	offset error		-	-	±2	LSB
E_G	gain error		-	-	±1	%
$E_{u(tot)}$	total unadjusted error		-	-	±2	LSB
M_{CTC}	channel-to-channel matching		-	-	±1	LSB
$\alpha_{ct(port)}$	crosstalk between port inputs	0 kHz to 100 kHz	-	-	−60	dB
SR_{in}	input slew rate		-	-	100	V/ms
$T_{cy(ADC)}$	ADC clock cycle time		111	-	2000	ns
t_{ADC}	ADC conversion time	A/D enabled	-	-	$13T_{cy(ADC)}$	ns

14. Package outline

PLCC28: plastic leaded chip carrier; 28 leads **SOT261-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.43 0.39	0.43 0.39	0.495 0.485	0.495 0.485	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT261-2	112E08	MS-018	EDR-7319			~~99-12-27~~ 01-11-15

Fig 32. Package outline SOT261-2 (PLCC28)

16. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89LPC933_934_ 935_936 v.8	20110112	Product data sheet	-	P89LPC933_934_ 935_936 v.7
Modifications:	• Table 10 “Limiting values”: Changed V_n max to 5.5 V. • Table 11 “Static characteristics”: Added V_{POR}. • Table 16 “ADC electrical characteristics”: Corrected V_{IA} max. • Section 8.16 “Reset”: Added sentence “When this pin functions as a reset input....”			
P89LPC933_934_ 935_936 v.7	20081126	Product data sheet	-	P89LPC933_934_ 935_936 v.6
P89LPC933_934_ 935_936 v.6	20050620	Product data sheet	-	P89LPC933_934_ 935_936 v.5
P89LPC933_934_ 935_936 v.5	20041103	Product data sheet	-	P89LPC933_934_ 935 v.4
P89LPC933_934_ 935 v.4	20040209	Objective data	-	P89LPC933_934_ 935 v.3