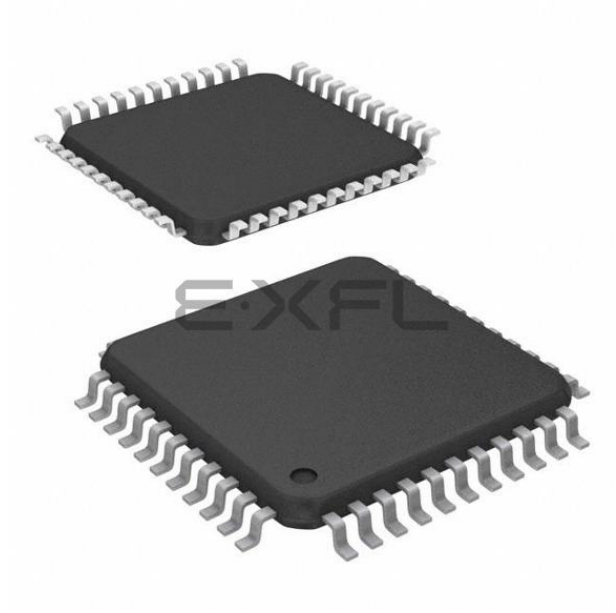
Analog Devices Inc./Maxim Integrated - DS80C320-ECG Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds80c320-ecg

DETAILED DESCRIPTION

The DS80C320/DS80C323 are fast 80C31/80C32-compatible microcontrollers. Wasted clock and memory cycles have been removed using a redesigned processor core. As a result, every 8051 instruction is executed between 1.5 and 3 times faster than the original for the same crystal speed. Typical applications see a speed improvement of 2.5 times using the same code and same crystal. The DS80C320 offers a maximum crystal rate of 33MHz, resulting in apparent execution speeds of 82.5MHz (approximately 2.5X).

The DS80C320/DS80C323 are pin compatible with all three packages of the standard 80C32 and offer the same timer/counters, serial port, and I/O ports. In short, the devices are extremely familiar to 8051 users, but provide the speed of a 16-bit processor.

The DS80C320 provides several extras in addition to greater speed. These include a second full hardware serial port, seven additional interrupts, programmable watchdog timer, power-fail interrupt and reset. The device also provides dual data pointers (DPTRs) to speed block data memory moves. It can also adjust the speed of off-chip data memory access to between two and nine machine cycles for flexibility in selecting memory and peripherals.

The DS80C320 operating voltage ranges from 4.25V to 5.5V, making it ideal as a high-performance upgrade to existing 5V systems. For applications in which power consumption is critical, the DS80C323 offers the same feature set as the DS80C320, but with 2.7V to 5.5V operation.

Designers must have two documents to fully use all the features of this device: this data sheet and the *High-Speed Microcontroller User's Guide*, available on our website at www.maxim-ic.com/microcontrollers. Data sheets contain pin descriptions, feature overviews, and electrical specifications, whereas our user's guides contain detailed information about device features and operation.

ORDERING INFORMATION

PART	Pb-FREE/RoHS-COMPLIANT	TEMP RANGE	MAX CLOCK SPEED (MHz)	PIN-PACKAGE
DS80C320-MCG	**DS80C320**-MCG+	0°C to +70°C	25	40 Plastic DIP
DS80C320-QCG	DS80C320-QCG+	0°C to +70°C	25	44 PLCC
DS80C320-ECG	DS80C320-ECG+	0°C to +70°C	25	44 TQFP
DS80C320-MNG	DS80C320-MNG+	-40°C to +85°C	25	40 Plastic DIP
DS80C320-QNG	DS80C320-QNG+	-40°C to +85°C	25	44 PLCC
DS80C320-ENG	DS80C320-ENG+	-40°C to +85°C	25	44 TQFP
DS80C320-MCL	DS80C320-MCL+	0°C to +70°C	33	40 Plastic DIP
DS80C320-QCL	DS80C320-QCL+	0°C to +70°C	33	44 PLCC
DS80C320-ECL	DS80C320-ECL+	0°C to +70°C	33	44 TQFP
DS80C320-MNL	DS80C320-MNL+	-40°C to +85°C	33	40 Plastic DIP
DS80C320-QNL	DS80C320-QNL+	-40°C to +85°C	33	44 PLCC
DS80C320-ENL	DS80C320-ENL+	-40°C to +85°C	33	44 TQFP
DS80C323-MCD	**DS80C323**-MCD+	0°C to +70°C	18	40 Plastic DIP
DS80C323-QCD	DS80C323-QCD+	0°C to +70°C	18	44 PLCC
DS80C323-ECD	DS80C323-ECD+	0°C to +70°C	18	44 TQFP
DS80C323-QND	DS80C323-QND+	-40°C to +85°C	18	44 PLCC
DS80C323-END	DS80C323-END+	-40°C to +85°C	18	44 TQFP

+ Denotes a lead(Pb)-free/RoHS-compliant device.

80C32 COMPATIBILITY

The DS80C320/DS80C323 are CMOS 80C32-compatible microcontrollers designed for high performance. In most cases, the devices will drop into an existing 80C32 design to significantly improve the operation. Every effort has been made to keep the devices familiar to 8032 users, yet they have many new features. In general, software written for existing 80C32-based systems will work on the DS80C320 and DS80C323. The exception is critical timing, because the high-speed microcontroller performs its instructions much faster than the original. It may be necessary to use memories with faster access times if the same crystal frequency is used.

Application Note 57: DS80C320 Memory Interface Timing is a useful tool to help the embedded system designer select the proper memories for her or his application.

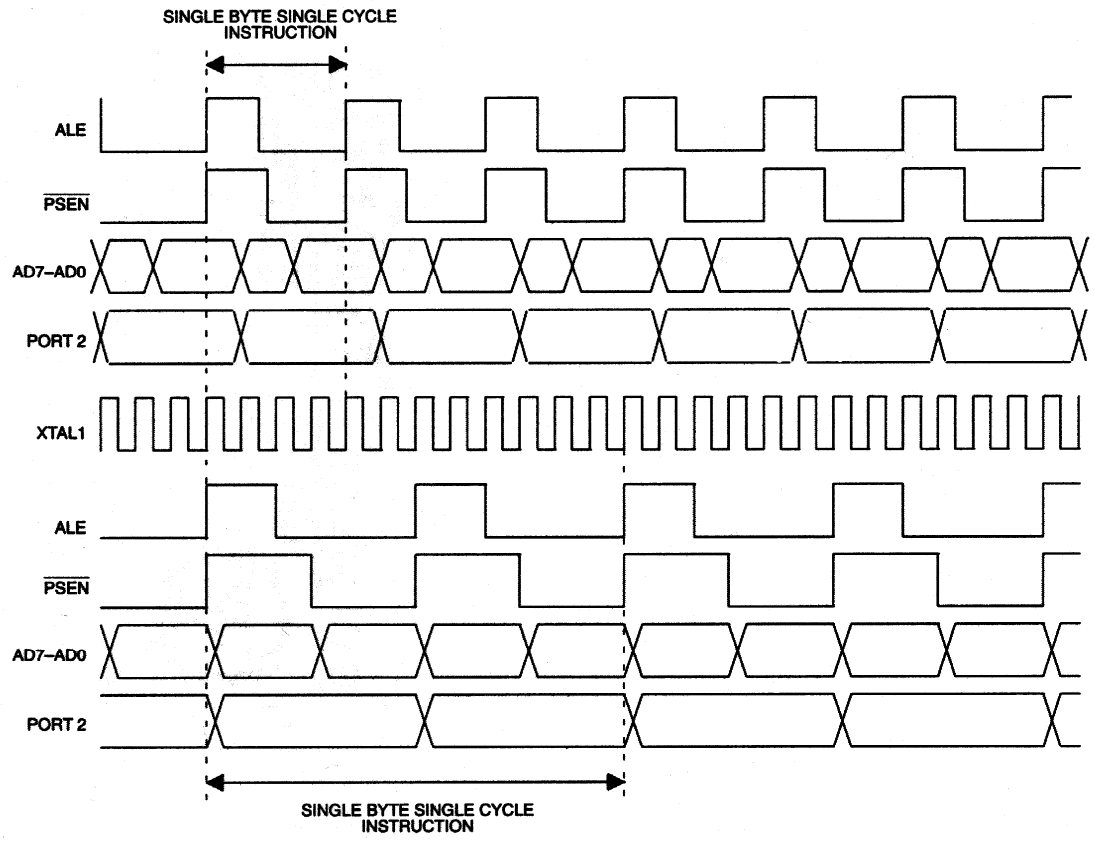
The DS80C320/DS80C323 run the standard 8051 instruction set and is pin compatible with an 80C32 in any of three standard packages. They also provide the same timer/counter resources, full-duplex serial port, 256 bytes of scratchpad RAM, and I/O ports as the standard 80C32. Timers will default to a 12 clock-per-cycle operation to keep timing compatible with original 8051 systems. However, they can be programmed to run at the new 4 clocks per cycle if desired.

New hardware features are accessed using special-function registers that do not overlap with standard 80C32 locations. A summary of these SFRs is provided below.

The DS80C320/DS80C323 address memory in an identical fashion to the standard 80C32. Electrical timing appears different due to the high-speed nature of the product. However, the signals are essentially the same. Detailed timing diagrams are provided in the *Electrical Specifications* section.

This data sheet assumes the user is familiar with the basic features of the standard 80C32. In addition to these standard features, the DS80C320/DS80C323 include many new functions. This data sheet provides only a summary and overview. Detailed descriptions are available in the *High-Speed Microcontroller User's Guide*.

Figure 2. Comparative Timing of the DS80C320/DS80C323 and 80C32



HIGH-SPEED OPERATION

The DS80C320/DS80C323 are built around a high-speed, 80C32-compatible core. Higher speed comes not just from increasing the clock frequency but also from a newer, more efficient design.

In this updated core, dummy memory cycles have been eliminated. In a conventional 80C32, machine cycles are generated by dividing the clock frequency by 12. In the DS80C320/DS80C323, the same machine cycle is performed in 4 clocks. Thus the fastest instruction, one machine cycle, is executed three times faster for the same crystal frequency. Note that these are identical instructions. Figure 2 shows a comparison of the timing differences. The majority of instructions will see the full 3-to-1 speed improvement. Some instructions will get between 1.5X and 2.4X improvement. Note that all instructions are faster than the original 80C51. Table 1 shows a summary of the instruction set, including the speed.

The numerical average of all op codes is approximately a 2.5-to-1 speed improvement. Individual programs are affected differently, depending on the actual instructions used. Speed-sensitive applications would make the most use of instructions that are three times faster. However, the sheer number of 3-to-1 improved op codes makes dramatic speed improvements likely for any code. The Dual Data Pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory.

INSTRUCTION SET SUMMARY

All instructions in the DS80C320/DS80C323 perform the same functions as their 80C32 counterparts. Their effect on bits, flags, and other status functions is identical. However, the timing of each instruction is different. This applies both in absolute and relative number of clocks.

For absolute timing of real-time events, the timing of software loops will need to be calculated using the Table 1. However, counter/timers default to run at the older 12 clocks per increment. Therefore, while software runs at higher speed, timer-based events need no modification to operate as before. Timers can be set to run at 4 clocks per increment cycle to take advantage of higher speed operation.

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture, the “MOVX A, @DPTR” instruction and the “MOV direct, direct” instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS80C320/DS80C323, the MOVX instruction can be done in two machine cycles or eight oscillator cycles, but the “MOV direct, direct” uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times from each other. This is because in most cases, the DS80C320/DS80C323 use one cycle for each byte. The user concerned with precise program timing should examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just four clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV.

Table 1. Instruction Set Summary

SYMBOL	FUNCTION
A	Accumulator
Rn	Register R7 to R0
direct	Internal Register Address
@Ri	Internal Register pointed to by R0 or R1 (except MOVX)
rel	Two's Complement Offset Byte

SYMBOL	FUNCTION
bit	direct bit-address
#data	8-bit constant
#data 16	16-bit constant
addr 16	16-bit destination address
addr 11	11-bit destination address

INSTRUCTION	BYTE	OSCILLATOR CYCLES	INSTRUCTION	BYTE	OSCILLATOR CYCLES
ARITHMATIC INSTRUCTIONS					
ADD A, Rn	1	4	INC A	1	4
ADD A, direct	2	8	INC Rn	1	4
ADD A, @Ri	1	4	INC direct	2	8
ADD A, #data	2	8	INC @Ri	1	4
ADDC A, Rn	1	4	INC DPTR	1	12
ADDC A, direct	2	8	DEC A	1	4
ADDC A, @Ri	1	4	DEC Rn	1	4
ADDC A, #data	2	8	DEC direct	2	8
SUBB A, Rn	1	4	DEC @Ri	1	4
SUBB A, direct	2	8	MUL AB	1	20
SUBB A, @Ri	1	4	DIV AB	1	20
SUBB A, #data	2	8	DA A	1	4
LOGICAL INSTRUCTIONS					
ANL A, Rn	1	4	XRL A, Rn	1	4
ANL A, direct	2	8	XRL A, direct	2	8
ANL A, @Ri	1	4	XRL A, @Ri	1	4
ANL A, #data	2	8	XRL A, #data	2	8
ANL direct, A	2	8	XRL direct, A	2	8
ANL direct, #data	3	12	XRL direct, #data	3	12
ORL A, Rn	1	4	CLR A	1	4
ORL A, direct	2	8	CPL A	1	4
ORL A, @Ri	1	4	RL A	1	4
ORL A, #data	2	8	RLC A	1	4
ORL direct, A	2	8	RR A	1	4
ORL direct, #data	3	12	RRC A	1	4

STRETCH MEMORY CYCLE

The DS80C320/DS80C323 allow the application software to adjust the speed of data memory access. The microcontroller is capable of performing the MOVX in as little as two instruction cycles. However, this value can be stretched as needed so that both fast memory and slow memory or peripherals can be accessed with no glue logic. Even in high-speed systems, it may not be necessary or desirable to perform data memory access at full speed. In addition, there are a variety of memory-mapped peripherals such as LCD displays or UARTs that are not fast.

The Stretch MOVX is controlled by the Clock Control Register at SFR location 8Eh as described below. This allows the user to select a stretch value between 0 and 7. A Stretch of 0 will result in a two-machine cycle MOVX. A Stretch of 7 will result in a MOVX of nine machine cycles. Software can dynamically change this value depending on the particular memory or peripheral.

On reset, the Stretch value will default to 1, resulting in a three-cycle MOVX. Therefore, RAM access will not be performed at full speed. This is a convenience to existing designs that may not have fast RAM in place. When maximum speed is desired, the software should select a Stretch value of 0. When using very slow RAM or peripherals, a larger stretch value can be selected. Note that this affects data memory only and the only way to slow program memory (ROM) access is to use a slower crystal.

Using a Stretch value between 1 and 7 causes the microcontroller to stretch the read/write strobe and all related timing. This results in a wider read/write strobe allowing more time for memory/peripherals to respond. The timing of the variable speed MOVX is shown in the *Electrical Specifications* section. Note that full speed access is not the reset default case. Table 2 shows the resulting strobe widths for each Stretch value. The memory stretch is implemented using the Clock Control special-function register at SFR location 8Eh. The stretch value is selected using bits CKCON.2–0. In the table, these bits are referred to as M2 through M0. The first stretch (default) allows the use of common 120ns or 150ns RAMs without dramatically lengthening the memory access.

Table 2. Data Memory Cycle Stretch Values

CKCON.2–0			MEMORY CYCLES	$\overline{RD}$ or $\overline{WR}$ STROBE WIDTH IN CLOCKS	STROBE WIDTH TIME AT 25MHz (ns)
MD2	MD1	MD0			
0	0	0	2	2	80
0	0	1	3 (default)	4	160
0	1	0	4	8	320
0	1	1	5	12	480
1	0	0	6	16	640
1	0	1	7	20	800
1	1	0	8	24	960
1	1	1	9	28	1120

DUAL DATA POINTER

Data memory block moves can be accelerated using the Dual Data Pointer (DPTR). The standard 8032 DPTR is a 16-bit value that is used to address off-chip data RAM or peripherals. In the DS80C320/DS80C323, the standard 16-bit data pointer is called DPTR0 and is located at SFR addresses 82h and 83h. These are the standard locations. The new DPTR is located at SFR 84h and 85h and is called DPTR1. The DPTR Select bit (DPS) chooses the active pointer and is located at the LSB of the SFR location 86h. No other bits in register 86h have any effect and are set to 0. The user switches between data pointers by toggling the LSB of register 86h. The increment (INC) instruction is the fastest way to accomplish this. All DPTR-related instructions use the currently selected DPTR for any activity. Therefore only one instruction is required to switch from a source to a destination address. Using the Dual-Data Pointer saves code from needing to save source and destination addresses when doing a block move. Once loaded, the software simply switches between DPTR and 1. The relevant register locations are as follows.

DPL	82h	Low byte original DPTR
DPH	83h	High byte original DPTR
DPL1	84h	Low byte new DPTR
DPH1	85h	High byte new DPTR
DPS	86h	DPTR Select (LSB)

Sample code listed below illustrates the saving from using the dual DPTR. The example program was original code written for an 8051 and requires a total of 1869 DS80C320/DS80C323 machine cycles. This takes 299µs to execute at 25MHz. The new code using the Dual DPTR requires only 1097 machine cycles taking 175.5µs. The Dual DPTR saves 772 machine cycles or 123.5µs for a 64-byte block move. Since each pass through the loop saves 12 machine cycles when compared to the single DPTR approach, larger blocks gain more efficiency using this feature.

64-Byte Block Move without Dual Data Pointer

```
; SH and SL are high and low byte source address.
; DH and DL are high and low byte of destination address.
                                                                    # CYCLES
MOV     R5, #64d            ; NUMBER OF BYTES TO MOVE               2
MOV     DPTR, #SHSL         ; LOAD SOURCE ADDRESS                   3
MOV     R1, #SL             ; SAVE LOW BYTE OF SOURCE               2
MOV     R2, #SH             ; SAVE HIGH BYTE OF SOURCE              2
MOV     R3, #DL             ; SAVE LOW BYTE OF DESTINATION          2
MOV     R4, #DH             ; SAVE HIGH BYTE OF DESTINATION         2

MOVE:
; THIS LOOP IS PERFORMED THE NUMBER OF TIMES LOADED INTO R5, IN THIS EXAMPLE 64

MOVX    A, @DPTR            ; READ SOURCE DATA BYTE                 2
MOV     R1, DPL             ; SAVE NEW SOURCE POINTER               2
MOV     R2, DPH             ;                                       2
MOV     DPL, R3             ; LOAD NEW DESTINATION                  2
MOV     DPH, R4             ;                                       2
MOVX    @DPTR, A            ; WRITE DATA TO DESTINATION             2
INC     DPTR                ; NEXT DESTINATION ADDRESS              3
MOV     R3, DPL             ; SAVE NEW DESTINATION POINTER          2
MOV     R4, DPH             ;                                       2
MOV     DPL, R1             ; GET NEW SOURCE POINTER                2
MOV     DPH, R2             ;                                       2
INC     DPTR                ; NEXT SOURCE ADDRESS                   3
DJNZ    R5, MOVE            ; FINISHED WITH TABLE?                  3
```

POWER MANAGEMENT

The DS80C320/DS80C323 provide the standard Idle and power-down (Stop) modes that are available on the standard 80C32. However, the device has enhancements that make these modes more useful, and allow more power saving.

The Idle mode is invoked by setting the LSB of the Power Control register (PCON to 87h). Idle will leave internal clocks, serial port and timer running. No memory access will be performed so power is dramatically reduced. Since clocks are running, the Idle power consumption is related to crystal frequency. It should be approximately one-half the operational power. The CPU can exit the Idle state with any interrupt or a reset.

The power-down or Stop mode is invoked by setting the PCON.1 bit. Stop mode is a lower power state than Idle since it turns off all internal clocking. The I_{CC} of a standard Stop mode is approximately 1 µA but is specified in the *Electrical Specifications* section. The CPU will exit Stop mode from an external interrupt or a reset condition.

Note that internally generated interrupts (timer, serial port, watchdog) are not useful in Idle or Stop since they require clocking activity.

IDLE MODE ENHANCEMENTS

A simple enhancement to Idle mode makes it substantially more useful. The innovation involves not the Idle mode itself, but the watchdog timer. As mentioned above, the Watchdog Timer provides an optional interrupt capability. This interrupt can provide a periodic interval timer to bring the DS80C320/DS80C323 out of Idle mode. This can be useful even if the Watchdog is not normally used. By enabling the Watchdog Timer and its interrupt prior to invoking Idle, a user can periodically come out of Idle perform an operation, then return to Idle until the next operation. This will lower the overall power consumption. When using the Watchdog Interrupt to cancel the Idle state, make sure to restart the Watchdog Timer or it will cause a reset.

STOP MODE ENHANCEMENTS

The DS80C320/DS80C323 provide two enhancements to the Stop mode. As documented above, the device provides a bandgap reference to determine Power-fail Interrupt and Reset thresholds. The default state is that the bandgap reference is off when Stop mode is invoked. This allows the extremely low power state mentioned above. A user can optionally choose to have the bandgap enabled during Stop mode. This means that PFI and power-fail reset will be activated and are valid means for leaving Stop mode.

In Stop mode with the bandgap on, I_{CC} will be approximately 50µA compared with 1µA with the bandgap off. If a user does not require a Power-fail Reset or Interrupt while in Stop mode, the bandgap can remain turned off. Note that only the most power sensitive applications should turn off the bandgap, as this results in an uncontrolled power-down condition.

The control of the bandgap reference is located in the Extended Interrupt Flag register (EXIF to 91h). Setting BGS (EXIF.0) to a 1 will leave the bandgap reference enabled during Stop mode. The default or reset condition is with the bit at a logic 0. This results in the bandgap being turned off during Stop mode. Note that this bit has no control of the reference during full power or Idle modes. Be aware that the DS80C320 and DS80C323 require that the reset watchdog timer bit (RWT;WDCON.0) be set

Figure 4. Ring Oscillator Startup

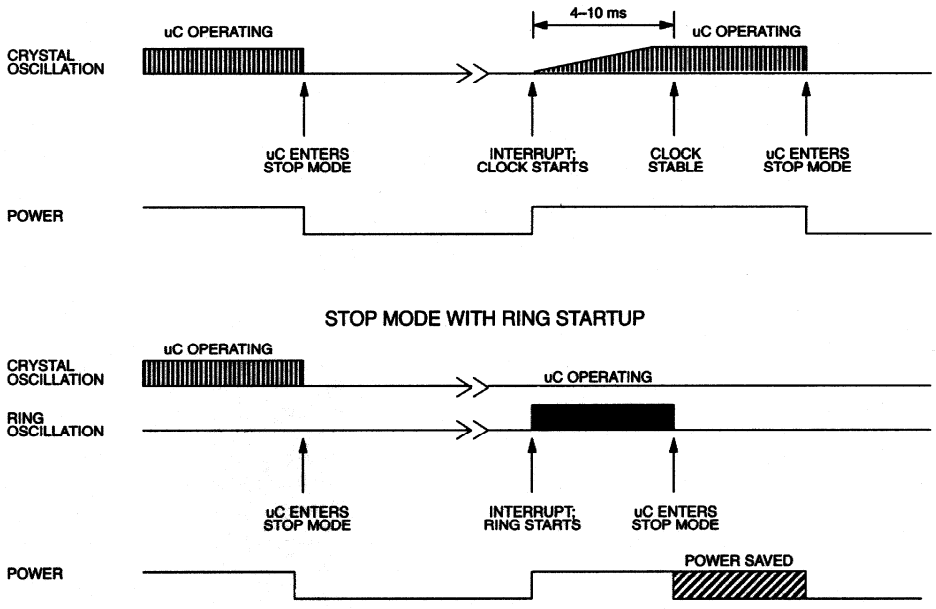


DIAGRAM ASSUMES THAT THE OPERATION FOLLOWING STOP REQUIRES LESS THAN 18ms COMPLETE.

TIMED ACCESS PROTECTION

Selected SFR bits are critical to operation, making it desirable to protect against an accidental write operation. The Timed Access procedure prevents an errant CPU from accidentally altering a bit that would cause difficulty. The Timed Access procedure requires that the write of a protected bit be preceded by the following instructions:

```
MOV     0C7h, #0AAh
MOV     0C7h, #55h
```

By writing an AAh followed by a 55h to the Timed Access register (location C7h), the hardware opens a three-cycle window that allows software to modify one of the protected bits. If the instruction that seeks to modify the protected bit is not immediately proceeded by these instructions, the write will not take effect. The protected bits are:

EXIF.0	BGS Bandgap Select
WDCON.6	POR Power-on Reset flag
WDCON.1	EWT Enable Watchdog
WDCON.0	RWT Reset Watchdog
WDCON.3	WDIF Watchdog Interrupt Flag

SPECIAL-FUNCTION REGISTERS

Most special features of the DS80C320/DS80C323 or 80C32 are controlled by bits in the SFRs, allowing the devices to add many features but use the same instruction set. When writing software to use a new feature, the SFR must be defined to an assembler or compiler using an equate statement. This is the only change needed to access the new function. The DS80C320/DS80C323 duplicate the SFRs that are contained in the standard 80C32. Table 5 shows the register addresses and bit locations. Many are standard 80C32 registers. The *High-Speed Microcontroller User's Guide* describes all SFRs.

Table 5. Special-Function Register Locations

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**SEL**	86h
PCON	SMOD_0	**SMOD0**	—	—	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	**WD1**	**WD0**	**T2M**	**T1M**	**T0M**	**MD2**	**MD1**	**MD0**	8Eh
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
EXIF	**IE5**	**IE4**	**IE3**	**IE2**	—	**RGMD**	**RGSL**	**BGS**	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
P2	P2.0	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	A8h
SADDR0									A9h
SADDR1									AAh
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
IP	—	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
SCON1	**SM0/FE_0**	**SM1_0**	**SM2_0**	**REN_0**	**TB8_0**	**RB8_0**	**TI_0**	**RI_0**	C0h
SBUF1									C1h
STATUS	PIP	HIP	LIP	1	1	1	1	1	C5h
TA									C7h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	C8h
T2MOD	—	—	—	—	—	—	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	FL	P	D0h
WDCON	**SMOD_1**	**POR**	**EPFI**	**PFI**	**WDIF**	**WTRF**	**EWT**	**RWT**	D8h
ACC									E0h
EIE	—	—	—	**EWDI**	**EX5**	**EX4**	**EX3**	**EX2**	E8h
B									F0h
EIP	—	—	—	**PWDI**	**PX5**	**PX4**	**PX3**	**PX2**	F8h

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground……..-0.3V to +6.0V
Operating Temperature Range……-40°C to +85°C
Storage Temperature Range……..-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS—DS80C320

(V_{CC} = 4.5V to 5.5V, T_A = -40°C to +85°C.)

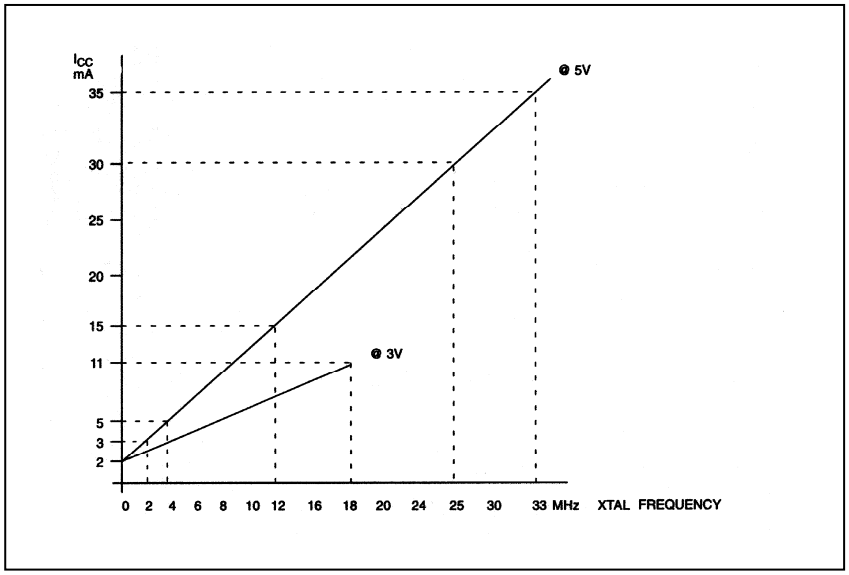
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Power-Fail Warning Voltage	V_{PFW}	4.25	4.38	4.55	V	1
Minimum Operating Voltage	V_{RST}	4.0	4.1	4.25	V	1, 12
Supply Current Active Mode at 25MHz	I_{CC}		30	45	mA	2
Supply Current Idle Mode at 25MHz	I_{IDLE}		15	25	mA	3
Supply Current Active Mode at 33MHz	I_{CC}		35		mA	2
Supply Current Idle Mode at 33MHz	I_{IDLE}		20		mA	3
Supply Current Stop Mode, Bandgap Reference Disabled	I_{STOP}		0.01	1	µA	4
Supply Current Stop Mode, Bandgap Reference Enabled	I_{SPBG}		50	80	µA	4, 10
Input Low Level	V_{IL}	-0.3		+0.8	V	1
Input High Level (Except XTAL1 and RST)	V_{IH1}	2.0		V_{CC} + 0.3	V	1
Input High Level XTAL1 and RST	V_{IH2}	3.5		V_{CC} + 0.3	V	1
Output-Low Voltage Ports 1, 3 at I_{OL} = 1.6mA	V_{OL1}			0.45	V	1
Output-Low Voltage Ports 0, 2, ALE, $\overline{PSEN}$ at I_{OL} = 3.2mA	V_{OL2}			0.45	V	1, 5
Output-High Voltage Ports 1, 3, ALE, $\overline{PSEN}$ at I_{OH} = -50µA	V_{OH1}	2.4			V	1, 6
Output High Voltage Ports 1, 3 at I_{OH} = -1.5mA	V_{OH2}	2.4			V	1, 7
Output-High Voltage Ports 0, 2, ALE, $\overline{PSEN}$ at I_{OH} = -8mA	V_{OH3}	2.4			V	1, 5
Input Low Current Ports 1, 3 at 0.45V	I_{IL}			-55	µA	11
Transition Current from 1 to 0 Ports 1, 3 at 2V	I_{TL}			-650	µA	8
Input Leakage Port 0, Bus Mode	I_L	-300		+300	µA	9
RST Pulldown Resistance	R_{RST}	50		170	kΩ	

NOTES FOR DS80C320 DC ELECTRICAL CHARACTERISTICS

All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested.

1. All voltages are referenced to ground.
2. Active current is measured with a 25MHz clock source driving XTAL1, V_{CC} = RST = 5.5V, all other pins disconnected.
3. Idle mode current is measured with a 25MHz clock source driving XTAL1, V_{CC} = 5.5V, RST at ground, all other pins disconnected.
4. Stop mode current measured with XTAL1 and RST grounded, V_{CC} = 5.5V, all other pins disconnected.
5. When addressing external memory. This specification only applies to the first clock cycle following transition.
6. RST = V_{CC}. This condition mimics operation of pins in I/O mode.
7. During a 0-to-1 transition, a one-shot drives the ports hard for two clock cycles. This measurement reflects port in transition mode.
8. Ports 1 and 3 source transition current when being pulled down externally. It reaches its maximum at approximately 2V.
9. $0.45<V_{IN}<V_{CC}$. Not a high-impedance input. This port is a weak address holding latch because Port 0 is dedicated as an address bus on the DS80C320. Peak current occurs near the input transition point of the latch, approximately 2V.
10. Over the industrial temperature range, this specification has a maximum value of 200µA.
11. This is the current required from an external circuit to hold a logic low level on an I/O pin while the corresponding port latch bit is set to 1. This is only the current required to *hold* the low level; transitions from 1 to 0 on an I/O pin will also have to overcome the transition current.
12. Device operating range is 4.5V to 5.5V; however, device is tested to 4.0V to ensure proper operation at minimum V_{RST}.

TYPICAL I_{CC} vs. FREQUENCY



MOVX CHARACTERISTICS—DS80C320

PARAMETER	SYMBOL	VARIABLE CLOCK		UNITS	STRETCH
		MIN	MAX		
$\overline{RD}$ Pulse Width	t_{RLRH}	$2t_{CLCL}$-11		ns	t_{MCS}=0
		t_{MCS}-11			t_{MCS}>0
$\overline{WR}$ Pulse Width	t_{WLWH}	$2t_{CLCL}$-11		ns	t_{MCS}=0
		t_{MCS}-11			t_{MCS}>0
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2t_{CLCL}$-25	ns	t_{MCS}=0
			t_{MCS}-25		t_{MCS}>0
Data Hold After Read	t_{RHDX}	0		ns	
Data Float After Read	t_{RHDZ}		t_{CLCL}-5	ns	t_{MCS}=0
			$2t_{CLCL}$-5		t_{MCS}>0
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL}$-27	ns	t_{MCS}=0
			$1.5t_{CLCL}$-28+t_{MCS}		t_{MCS}>0
Port 0 Address to Valid Data In	t_{AVDV1}		$3t_{CLCL}$-27	ns	t_{MCS}=0
			$2t_{CLCL}$-31+t_{MCS}		t_{MCS}>0
Port 2 Address to Valid Data In	t_{AVDV2}		$3.5t_{CLCL}$-32	ns	t_{MCS}=0
			$2.5t_{CLCL}$-34+t_{MCS}		t_{MCS}>0
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL}$-8	$0.5t_{CLCL}$+6	ns	t_{MCS}=0
		$1.5t_{CLCL}$-7	$1.5t_{CLCL}$+8		t_{MCS}>0
Port 0 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	t_{CLCL}-11		ns	t_{MCS}=0
		$2t_{CLCL}$-10			t_{MCS}>0
Port 2 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL}$-9		ns	t_{MCS}=0
		$2.5t_{CLCL}$-13			t_{MCS}>0
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-9		ns	t_{MCS}=0
		t_{CLCL}-10			t_{MCS}>0
Data Hold After Write	t_{WHQX}	t_{CLCL}-12		ns	t_{MCS}=0
		$2t_{CLCL}$-7			t_{MCS}>0
$\overline{RD}$ Low to Address Float	t_{RLAZ}		(Note 5)	ns	
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{WHLH}	0	10	ns	t_{MCS}=0
		t_{CLCL}-5	t_{CLCL}+11		t_{MCS}>0

Note: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.

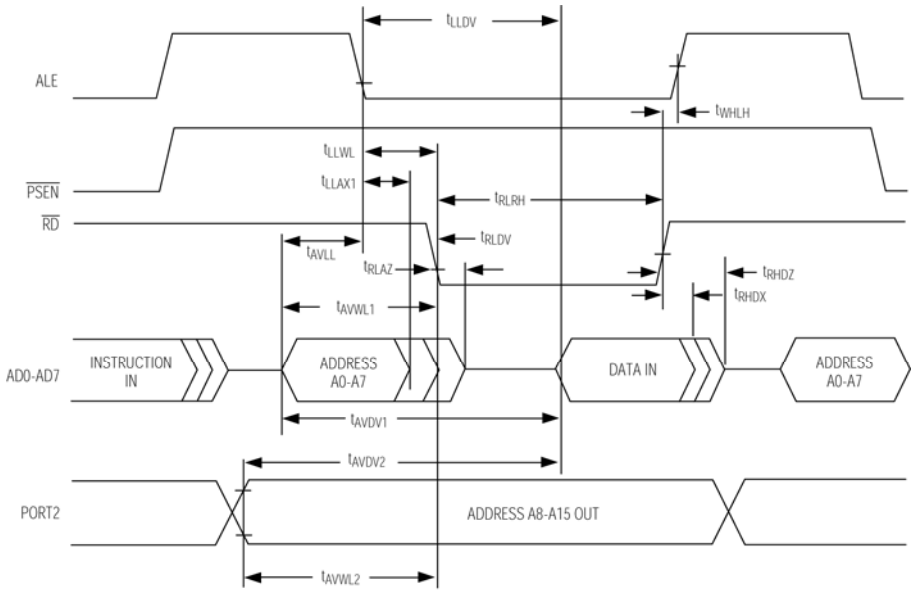
M2	M1	M0	MOVX CYCLES	t_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles (default)	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

NOTES FOR DS80C323 DC ELECTRICAL CHARACTERISTICS (continued)

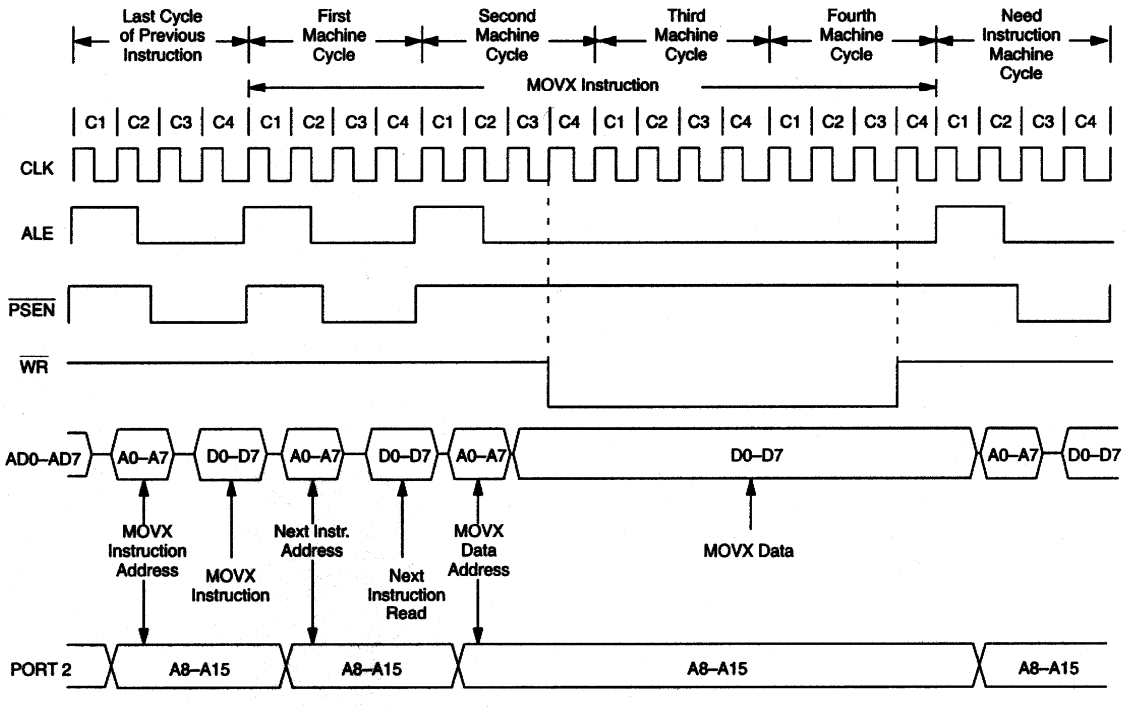
All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested. Device operating range is 2.7V to 5.5V. DC electrical specifications are for operation 2.7V to 3.3V.

6. RST = V_{CC}. This condition mimics operation of pins in I/O mode.
7. During a 0-to-1 transition, a one-shot drives the ports hard for two clock cycles. This measurement reflects port in transition mode.
8. Ports 1, 2, and 3 source transition current when being pulled down externally. It reaches its maximum at approximately 2V.
9. V_{IN} between ground and V_{CC} - 0.3V. Not a high-impedance input. This port is a weak address latch because Port 0 is dedicated as an address bus on the DS80C323. Peak current occurs near the input transition point of the latch, approximately 2V.
10. Over the industrial temperature range, this specification has a maximum value of 200µA.
11. This is the current from an external circuit to hold a logic low level on an I/O pin while the corresponding port latch bit is set to 1. This is only the current required to *hold* the low level; transitions from 1 to 0 on an I/O pin will also have to overcome the transition current.
12. Device operating range is 2.7V to 5.5V, however device is tested to 2.5V to ensure proper operation at minimum V_{RST}.

DATA MEMORY READ CYCLE

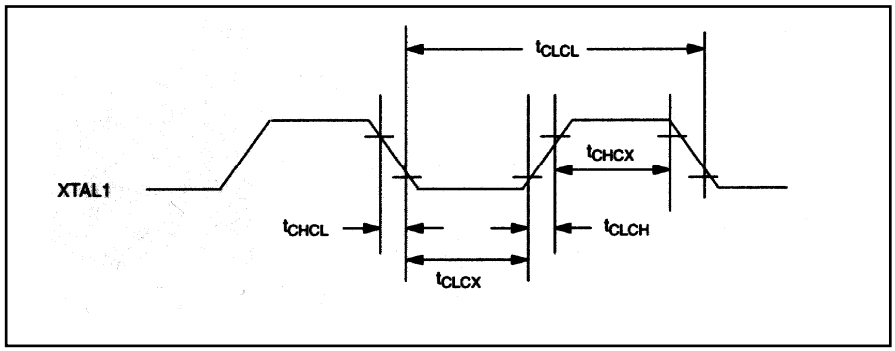


DATA MEMORY WRITE WITH STRETCH = 2

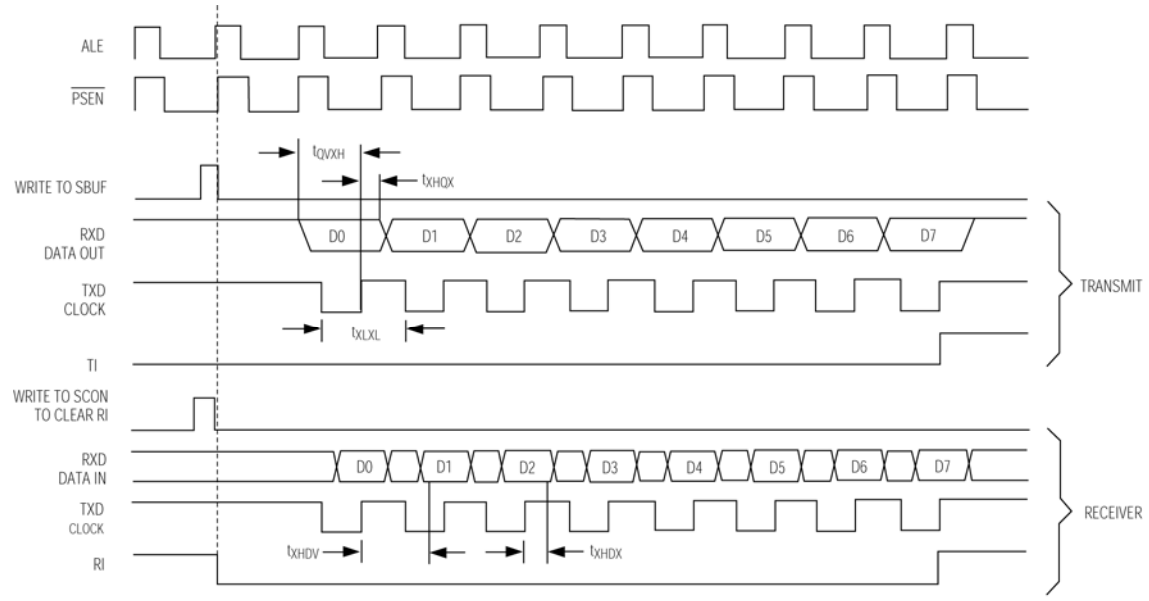


4-CYCLE DATA MEMORY WRITE
STRETCH VALUE = 2

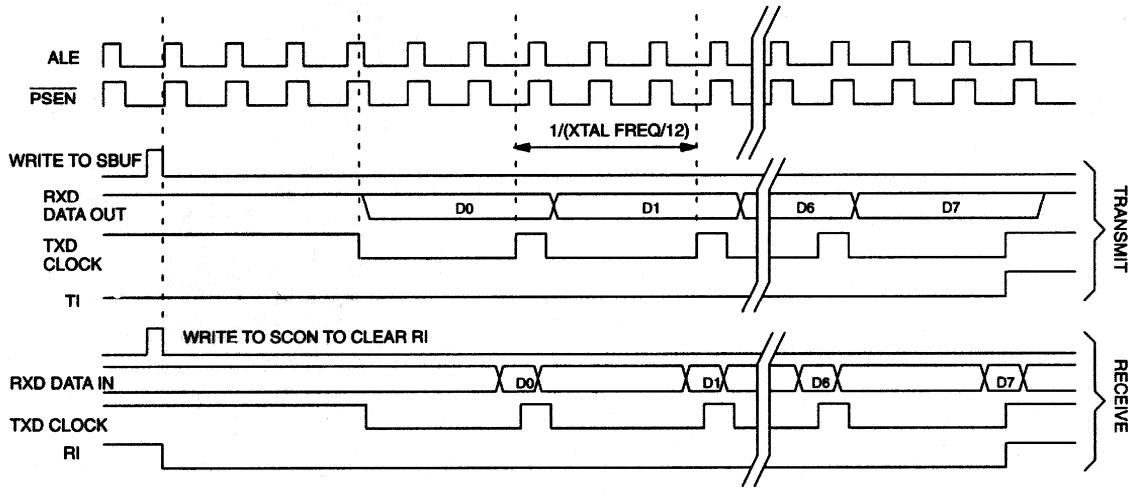
EXTERNAL CLOCK DRIVE



SERIAL PORT MODE 0 TIMING

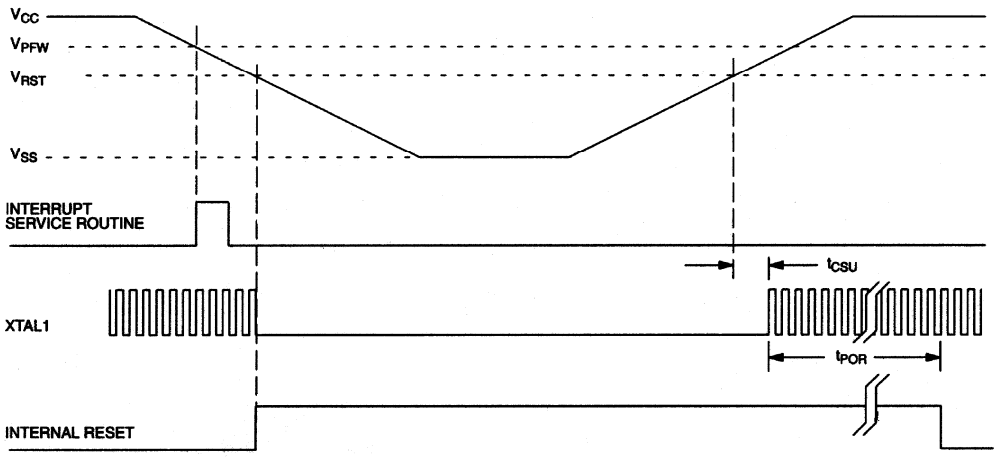


SERIAL PORT 0 (SYNCHRONOUS MODE)
HIGH SPEED OPERATION SM2 = 1 ≥ TXD CLOCK = XTAL/4



SERIAL PORT 0 (SYNCHRONOUS MODE)
SM2 = 0 ≥ TXD CLOCK = XTAL/12

POWER-CYCLE TIMING



PACKAGE INFORMATION

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
44 TQFP	C44+2	**21-0293**
44 MQFP	M44+10	**21-0269**
44 MQFP	M44+5	**21-0826**
40 PDIP	P40+1	**21-0044**
44 PLCC	Q44+1	**21-0049**

DATA SHEET REVISION SUMMARY (continued)

The following represent the key differences between the 05/22/96 and the 10/21/97 version of the DS80C320 data sheet. Please review this summary carefully.

DS80C320

1. Added note to clarify I_{IL} specification.
2. Added note to clarify AC timing conditions.
3. Corrected erroneous t_{QVXL} label on figure "Serial Port Mode 0 Timing" to read t_{QVXH}.
4. Added note to prevent accidental corruption of Watchdog Timer count while changing counter length.

DS80C323

1. Added note to clarify I_{IL} specification.
2. Remove port 2 from V_{OH1} specification, add port 3.
3. I_{OH} for V_{OH3} specification changed from -3mA to -2mA.
4. Added note to clarify AC timing conditions.

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