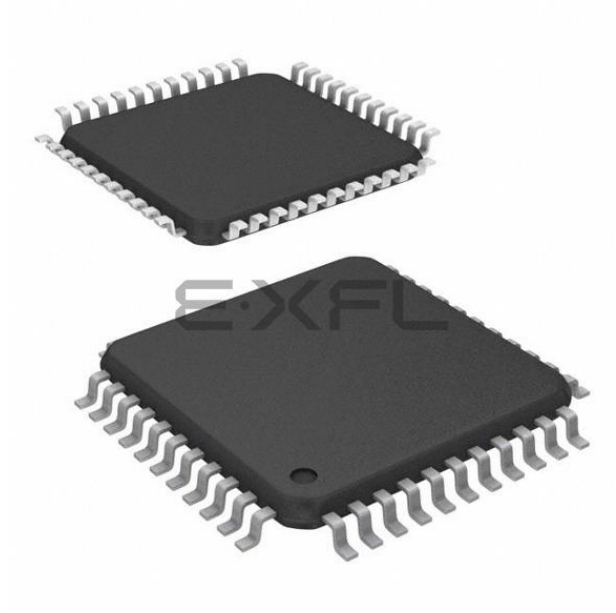
Analog Devices Inc./Maxim Integrated - DS80C320-ECL+ Datasheet



Welcome to E-XFL.COM

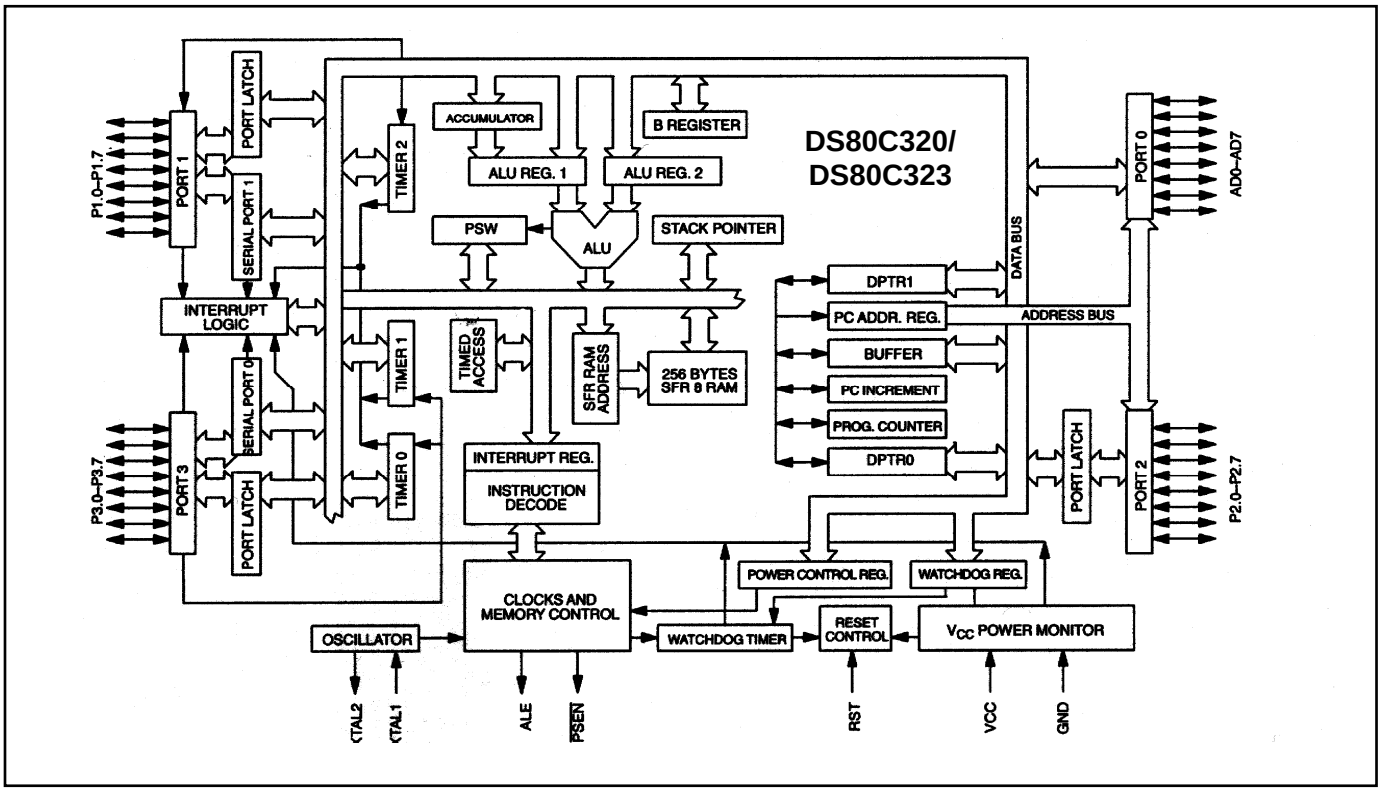
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds80c320-ecl

Figure 1. Block Diagram



PIN DESCRIPTION

PIN			NAME	FUNCTION
DIP	PLCC	TQFP		
40	44	38	V_{CC}	**+5V (+3V for DS80C323)**
20	22, 23	16, 17	GND	**Digital Circuit Ground**
9	10	4	RST	**Reset Input.** The RST input pin contains a Schmitt voltage input to recognize external active-high reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wired OR external reset sources. An RC is ***not*** required for power-up, as the device provides this function internally.
18	20	14	XTAL2	**Crystal Oscillator Pins.** XTAL1 and XTAL2 provide support for parallel-resonant, AT-cut crystals. XTAL1 acts also as an input in the event that an external clock source is used in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
19	21	15	XTAL1	
29	32	26	$\overline{\text{PSEN}}$	**Program Store-Enable Output, Active Low.** This signal is commonly connected to external ROM memory as a chip enable. $\overline{\text{PSEN}}$ provides an active-low pulse width of 2.25 XTAL1 cycles with a period of four XTAL1 cycles. $\overline{\text{PSEN}}$ is driven high when data memory (RAM) is being accessed through the bus and during a reset condition.

80C32 COMPATIBILITY

The DS80C320/DS80C323 are CMOS 80C32-compatible microcontrollers designed for high performance. In most cases, the devices will drop into an existing 80C32 design to significantly improve the operation. Every effort has been made to keep the devices familiar to 8032 users, yet they have many new features. In general, software written for existing 80C32-based systems will work on the DS80C320 and DS80C323. The exception is critical timing, because the high-speed microcontroller performs its instructions much faster than the original. It may be necessary to use memories with faster access times if the same crystal frequency is used.

Application Note 57: DS80C320 Memory Interface Timing is a useful tool to help the embedded system designer select the proper memories for her or his application.

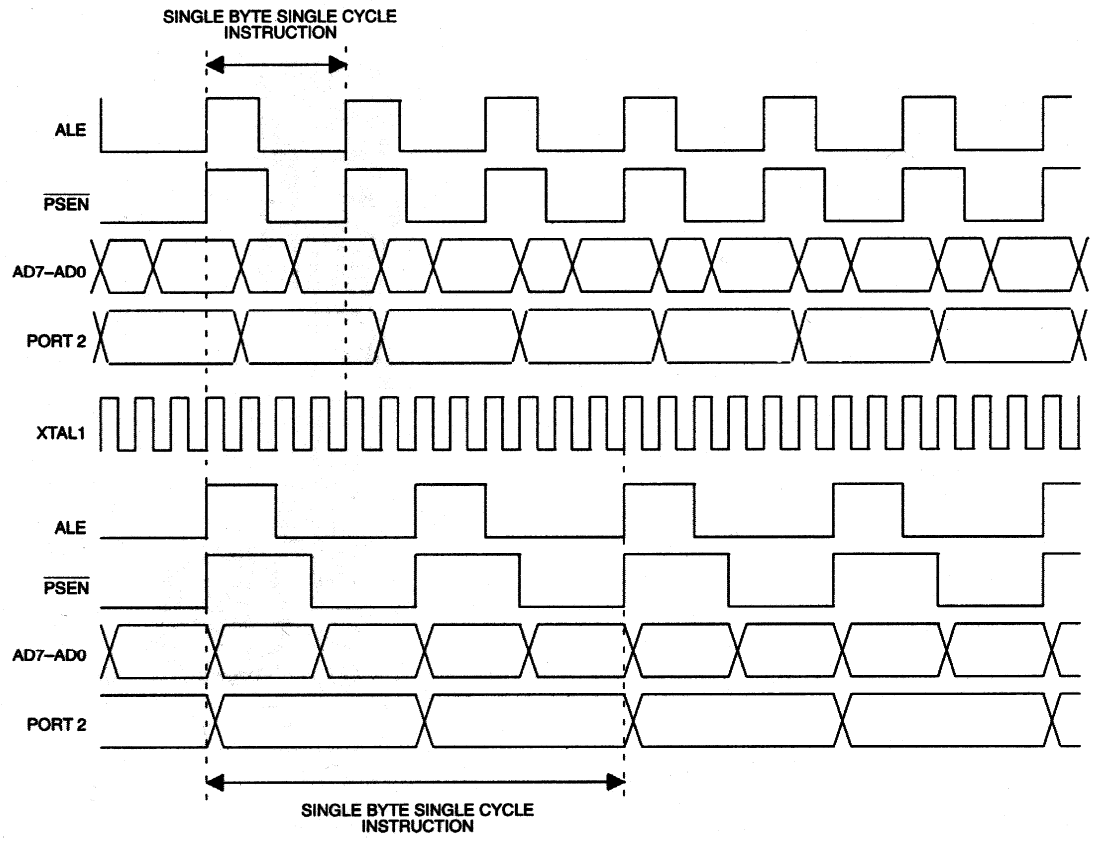
The DS80C320/DS80C323 run the standard 8051 instruction set and is pin compatible with an 80C32 in any of three standard packages. They also provide the same timer/counter resources, full-duplex serial port, 256 bytes of scratchpad RAM, and I/O ports as the standard 80C32. Timers will default to a 12 clock-per-cycle operation to keep timing compatible with original 8051 systems. However, they can be programmed to run at the new 4 clocks per cycle if desired.

New hardware features are accessed using special-function registers that do not overlap with standard 80C32 locations. A summary of these SFRs is provided below.

The DS80C320/DS80C323 address memory in an identical fashion to the standard 80C32. Electrical timing appears different due to the high-speed nature of the product. However, the signals are essentially the same. Detailed timing diagrams are provided in the *Electrical Specifications* section.

This data sheet assumes the user is familiar with the basic features of the standard 80C32. In addition to these standard features, the DS80C320/DS80C323 include many new functions. This data sheet provides only a summary and overview. Detailed descriptions are available in the *High-Speed Microcontroller User's Guide*.

Figure 2. Comparative Timing of the DS80C320/DS80C323 and 80C32



HIGH-SPEED OPERATION

The DS80C320/DS80C323 are built around a high-speed, 80C32-compatible core. Higher speed comes not just from increasing the clock frequency but also from a newer, more efficient design.

In this updated core, dummy memory cycles have been eliminated. In a conventional 80C32, machine cycles are generated by dividing the clock frequency by 12. In the DS80C320/DS80C323, the same machine cycle is performed in 4 clocks. Thus the fastest instruction, one machine cycle, is executed three times faster for the same crystal frequency. Note that these are identical instructions. Figure 2 shows a comparison of the timing differences. The majority of instructions will see the full 3-to-1 speed improvement. Some instructions will get between 1.5X and 2.4X improvement. Note that all instructions are faster than the original 80C51. Table 1 shows a summary of the instruction set, including the speed.

The numerical average of all op codes is approximately a 2.5-to-1 speed improvement. Individual programs are affected differently, depending on the actual instructions used. Speed-sensitive applications would make the most use of instructions that are three times faster. However, the sheer number of 3-to-1 improved op codes makes dramatic speed improvements likely for any code. The Dual Data Pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory.

Table 1. Instruction Set Summary

SYMBOL	FUNCTION
A	Accumulator
Rn	Register R7 to R0
direct	Internal Register Address
@Ri	Internal Register pointed to by R0 or R1 (except MOVX)
rel	Two's Complement Offset Byte

SYMBOL	FUNCTION
bit	direct bit-address
#data	8-bit constant
#data 16	16-bit constant
addr 16	16-bit destination address
addr 11	11-bit destination address

INSTRUCTION	BYTE	OSCILLATOR CYCLES	INSTRUCTION	BYTE	OSCILLATOR CYCLES
ARITHMATIC INSTRUCTIONS					
ADD A, Rn	1	4	INC A	1	4
ADD A, direct	2	8	INC Rn	1	4
ADD A, @Ri	1	4	INC direct	2	8
ADD A, #data	2	8	INC @Ri	1	4
ADDC A, Rn	1	4	INC DPTR	1	12
ADDC A, direct	2	8	DEC A	1	4
ADDC A, @Ri	1	4	DEC Rn	1	4
ADDC A, #data	2	8	DEC direct	2	8
SUBB A, Rn	1	4	DEC @Ri	1	4
SUBB A, direct	2	8	MUL AB	1	20
SUBB A, @Ri	1	4	DIV AB	1	20
SUBB A, #data	2	8	DA A	1	4
LOGICAL INSTRUCTIONS					
ANL A, Rn	1	4	XRL A, Rn	1	4
ANL A, direct	2	8	XRL A, direct	2	8
ANL A, @Ri	1	4	XRL A, @Ri	1	4
ANL A, #data	2	8	XRL A, #data	2	8
ANL direct, A	2	8	XRL direct, A	2	8
ANL direct, #data	3	12	XRL direct, #data	3	12
ORL A, Rn	1	4	CLR A	1	4
ORL A, direct	2	8	CPL A	1	4
ORL A, @Ri	1	4	RL A	1	4
ORL A, #data	2	8	RLC A	1	4
ORL direct, A	2	8	RR A	1	4
ORL direct, #data	3	12	RRC A	1	4

Table 1 shows the speed for each class of instruction. Note that many of the instructions have multiple op codes. There are 255 op codes for 111 instructions. Of the 255 op codes, 159 are three times faster than the original 80C32. While a system that emphasizes those instructions will see the most improvement, the large total number that receive a 3 to 1 improvement assure a dramatic speed increase for any system. The speed improvement summary is provided below.

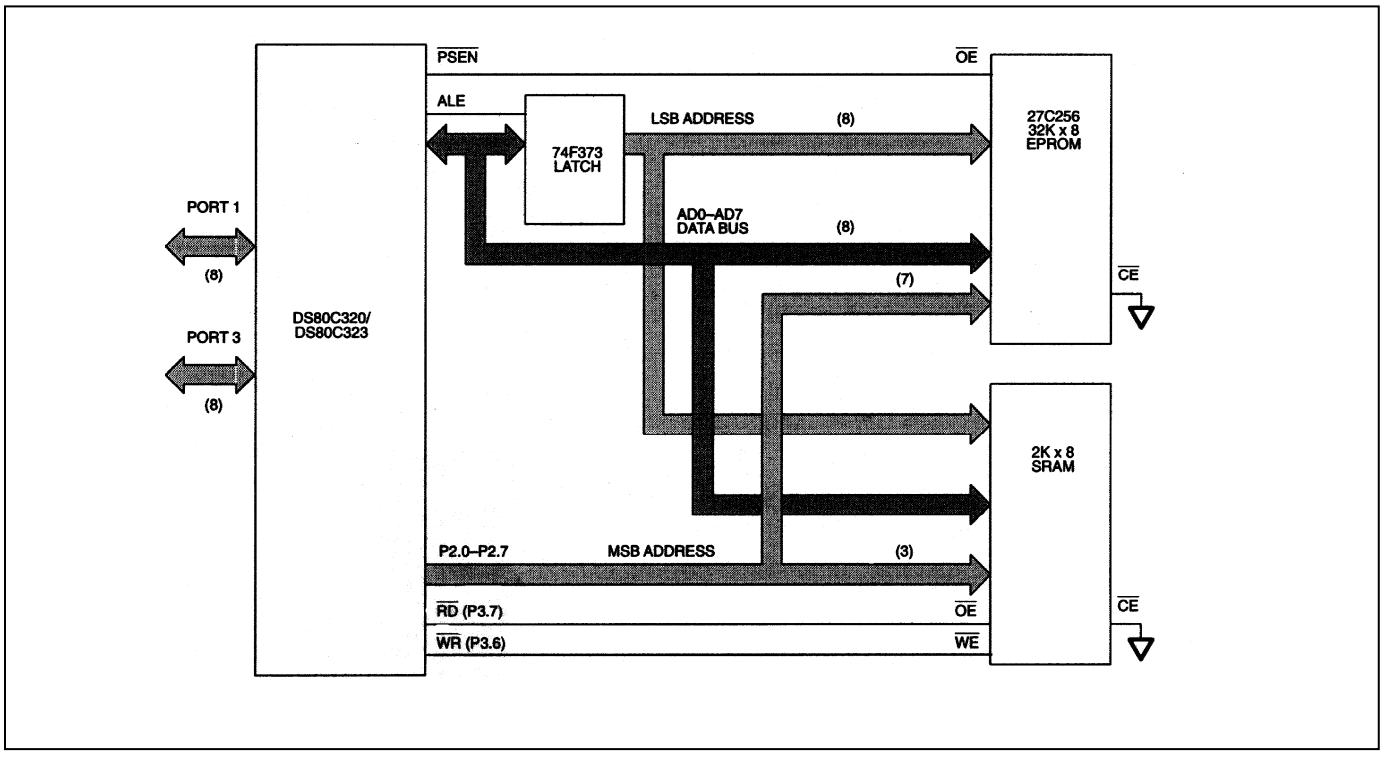
SPEED ADVANTAGE SUMMARY

#OP CODES	SPEED IMPROVEMENT
159	3.0 x
51	1.5 x
43	2.0 x
2	2.4 x
255	Average: 2.5

MEMORY ACCESS

The DS80C320/DS80C323 do not contain on-chip ROM and 256 bytes of scratchpad RAM. Off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. Figure 3 shows a typical memory connection. Timing diagrams are provided in the *Electrical Specifications* section. Program memory (ROM) is accessed at a fixed rate determined by the crystal frequency and the actual instructions. As previously mentioned, an instruction cycle requires 4 clocks. Data memory (RAM) is accessed according to a variable-speed MOVX instruction as described below.

Figure 3. Typical Memory Connection



STRETCH MEMORY CYCLE

The DS80C320/DS80C323 allow the application software to adjust the speed of data memory access. The microcontroller is capable of performing the MOVX in as little as two instruction cycles. However, this value can be stretched as needed so that both fast memory and slow memory or peripherals can be accessed with no glue logic. Even in high-speed systems, it may not be necessary or desirable to perform data memory access at full speed. In addition, there are a variety of memory-mapped peripherals such as LCD displays or UARTs that are not fast.

The Stretch MOVX is controlled by the Clock Control Register at SFR location 8Eh as described below. This allows the user to select a stretch value between 0 and 7. A Stretch of 0 will result in a two-machine cycle MOVX. A Stretch of 7 will result in a MOVX of nine machine cycles. Software can dynamically change this value depending on the particular memory or peripheral.

On reset, the Stretch value will default to 1, resulting in a three-cycle MOVX. Therefore, RAM access will not be performed at full speed. This is a convenience to existing designs that may not have fast RAM in place. When maximum speed is desired, the software should select a Stretch value of 0. When using very slow RAM or peripherals, a larger stretch value can be selected. Note that this affects data memory only and the only way to slow program memory (ROM) access is to use a slower crystal.

Using a Stretch value between 1 and 7 causes the microcontroller to stretch the read/write strobe and all related timing. This results in a wider read/write strobe allowing more time for memory/peripherals to respond. The timing of the variable speed MOVX is shown in the *Electrical Specifications* section. Note that full speed access is not the reset default case. Table 2 shows the resulting strobe widths for each Stretch value. The memory stretch is implemented using the Clock Control special-function register at SFR location 8Eh. The stretch value is selected using bits CKCON.2–0. In the table, these bits are referred to as M2 through M0. The first stretch (default) allows the use of common 120ns or 150ns RAMs without dramatically lengthening the memory access.

Table 2. Data Memory Cycle Stretch Values

CKCON.2–0			MEMORY CYCLES	$\overline{RD}$ or $\overline{WR}$ STROBE WIDTH IN CLOCKS	STROBE WIDTH TIME AT 25MHz (ns)
MD2	MD1	MD0			
0	0	0	2	2	80
0	0	1	3 (default)	4	160
0	1	0	4	8	320
0	1	1	5	12	480
1	0	0	6	16	640
1	0	1	7	20	800
1	1	0	8	24	960
1	1	1	9	28	1120

Figure 4. Ring Oscillator Startup

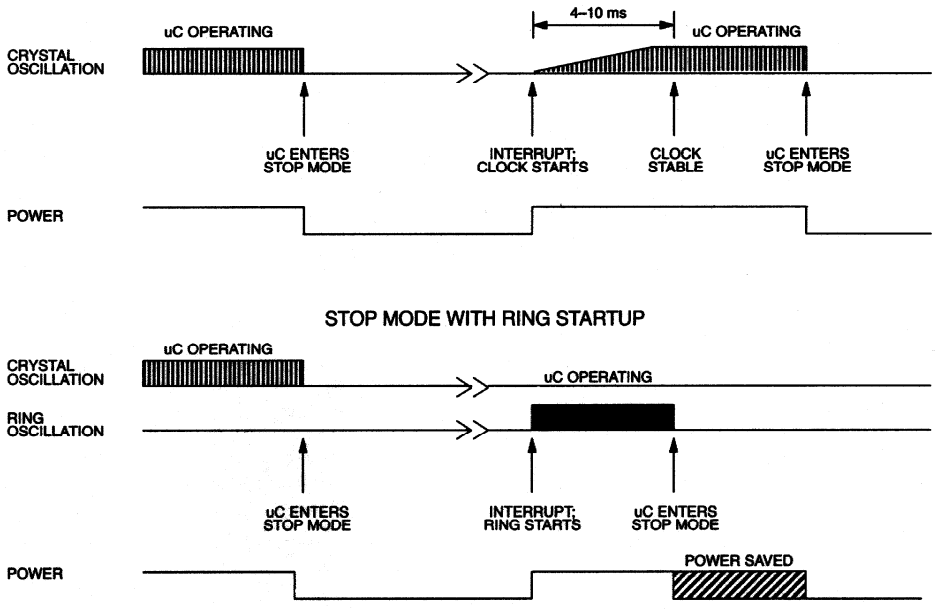


DIAGRAM ASSUMES THAT THE OPERATION FOLLOWING STOP REQUIRES LESS THAN 18ms COMPLETE.

TIMED ACCESS PROTECTION

Selected SFR bits are critical to operation, making it desirable to protect against an accidental write operation. The Timed Access procedure prevents an errant CPU from accidentally altering a bit that would cause difficulty. The Timed Access procedure requires that the write of a protected bit be preceded by the following instructions:

```
MOV     0C7h, #0AAh
MOV     0C7h, #55h
```

By writing an AAh followed by a 55h to the Timed Access register (location C7h), the hardware opens a three-cycle window that allows software to modify one of the protected bits. If the instruction that seeks to modify the protected bit is not immediately proceeded by these instructions, the write will not take effect. The protected bits are:

EXIF.0	BGS Bandgap Select
WDCON.6	POR Power-on Reset flag
WDCON.1	EWT Enable Watchdog
WDCON.0	RWT Reset Watchdog
WDCON.3	WDIF Watchdog Interrupt Flag

SPECIAL-FUNCTION REGISTERS

Most special features of the DS80C320/DS80C323 or 80C32 are controlled by bits in the SFRs, allowing the devices to add many features but use the same instruction set. When writing software to use a new feature, the SFR must be defined to an assembler or compiler using an equate statement. This is the only change needed to access the new function. The DS80C320/DS80C323 duplicate the SFRs that are contained in the standard 80C32. Table 5 shows the register addresses and bit locations. Many are standard 80C32 registers. The *High-Speed Microcontroller User's Guide* describes all SFRs.

Table 5. Special-Function Register Locations

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**SEL**	86h
PCON	SMOD_0	**SMOD0**	—	—	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	**WD1**	**WD0**	**T2M**	**T1M**	**T0M**	**MD2**	**MD1**	**MD0**	8Eh
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
EXIF	**IE5**	**IE4**	**IE3**	**IE2**	—	**RGMD**	**RGSL**	**BGS**	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
P2	P2.0	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	A8h
SADDR0									A9h
SADDR1									AAh
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
IP	—	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
SCON1	**SM0/FE_0**	**SM1_0**	**SM2_0**	**REN_0**	**TB8_0**	**RB8_0**	**TI_0**	**RI_0**	C0h
SBUF1									C1h
STATUS	PIP	HIP	LIP	1	1	1	1	1	C5h
TA									C7h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	C8h
T2MOD	—	—	—	—	—	—	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	FL	P	D0h
WDCON	**SMOD_1**	**POR**	**EPFI**	**PFI**	**WDIF**	**WTRF**	**EWT**	**RWT**	D8h
ACC									E0h
EIE	—	—	—	**EWDI**	**EX5**	**EX4**	**EX3**	**EX2**	E8h
B									F0h
EIP	—	—	—	**PWDI**	**PX5**	**PX4**	**PX3**	**PX2**	F8h

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground……..-0.3V to +6.0V
Operating Temperature Range……-40°C to +85°C
Storage Temperature Range……..-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS—DS80C320

(V_{CC} = 4.5V to 5.5V, T_A = -40°C to +85°C.)

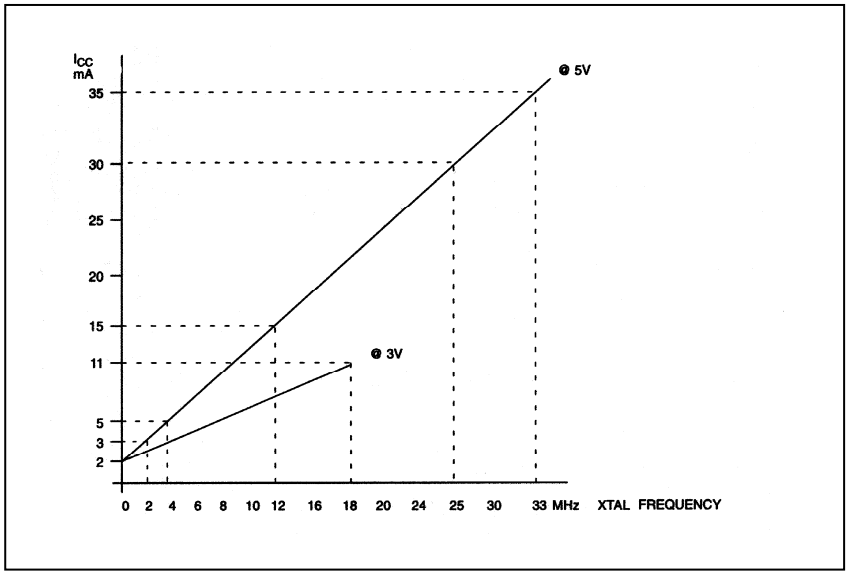
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Power-Fail Warning Voltage	V_{PFW}	4.25	4.38	4.55	V	1
Minimum Operating Voltage	V_{RST}	4.0	4.1	4.25	V	1, 12
Supply Current Active Mode at 25MHz	I_{CC}		30	45	mA	2
Supply Current Idle Mode at 25MHz	I_{IDLE}		15	25	mA	3
Supply Current Active Mode at 33MHz	I_{CC}		35		mA	2
Supply Current Idle Mode at 33MHz	I_{IDLE}		20		mA	3
Supply Current Stop Mode, Bandgap Reference Disabled	I_{STOP}		0.01	1	µA	4
Supply Current Stop Mode, Bandgap Reference Enabled	I_{SPBG}		50	80	µA	4, 10
Input Low Level	V_{IL}	-0.3		+0.8	V	1
Input High Level (Except XTAL1 and RST)	V_{IH1}	2.0		V_{CC} + 0.3	V	1
Input High Level XTAL1 and RST	V_{IH2}	3.5		V_{CC} + 0.3	V	1
Output-Low Voltage Ports 1, 3 at I_{OL} = 1.6mA	V_{OL1}			0.45	V	1
Output-Low Voltage Ports 0, 2, ALE, $\overline{PSEN}$ at I_{OL} = 3.2mA	V_{OL2}			0.45	V	1, 5
Output-High Voltage Ports 1, 3, ALE, $\overline{PSEN}$ at I_{OH} = -50µA	V_{OH1}	2.4			V	1, 6
Output High Voltage Ports 1, 3 at I_{OH} = -1.5mA	V_{OH2}	2.4			V	1, 7
Output-High Voltage Ports 0, 2, ALE, $\overline{PSEN}$ at I_{OH} = -8mA	V_{OH3}	2.4			V	1, 5
Input Low Current Ports 1, 3 at 0.45V	I_{IL}			-55	µA	11
Transition Current from 1 to 0 Ports 1, 3 at 2V	I_{TL}			-650	µA	8
Input Leakage Port 0, Bus Mode	I_L	-300		+300	µA	9
RST Pulldown Resistance	R_{RST}	50		170	kΩ	

NOTES FOR DS80C320 DC ELECTRICAL CHARACTERISTICS

All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested.

1. All voltages are referenced to ground.
2. Active current is measured with a 25MHz clock source driving XTAL1, V_{CC} = RST = 5.5V, all other pins disconnected.
3. Idle mode current is measured with a 25MHz clock source driving XTAL1, V_{CC} = 5.5V, RST at ground, all other pins disconnected.
4. Stop mode current measured with XTAL1 and RST grounded, V_{CC} = 5.5V, all other pins disconnected.
5. When addressing external memory. This specification only applies to the first clock cycle following transition.
6. RST = V_{CC}. This condition mimics operation of pins in I/O mode.
7. During a 0-to-1 transition, a one-shot drives the ports hard for two clock cycles. This measurement reflects port in transition mode.
8. Ports 1 and 3 source transition current when being pulled down externally. It reaches its maximum at approximately 2V.
9. $0.45<V_{IN}<V_{CC}$. Not a high-impedance input. This port is a weak address holding latch because Port 0 is dedicated as an address bus on the DS80C320. Peak current occurs near the input transition point of the latch, approximately 2V.
10. Over the industrial temperature range, this specification has a maximum value of 200µA.
11. This is the current required from an external circuit to hold a logic low level on an I/O pin while the corresponding port latch bit is set to 1. This is only the current required to *hold* the low level; transitions from 1 to 0 on an I/O pin will also have to overcome the transition current.
12. Device operating range is 4.5V to 5.5V; however, device is tested to 4.0V to ensure proper operation at minimum V_{RST}.

TYPICAL I_{CC} vs. FREQUENCY



DC ELECTRICAL CHARACTERISTICS—DS80C323

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Voltage	V_{CC}	2.7	3.0	5.5	V	1
Power-Fail Warning Voltage	V_{PFW}	2.6	2.7	2.8	V	1
Minimum Operating Voltage	V_{RST}	2.5	2.6	2.7	V	1, 12
Supply Current Active Mode at 18MHz	I_{CC}		10		mA	2
Supply Current Idle Mode at 18MHz	I_{IDLE}		6		mA	3
Supply Current Stop Mode, Bandgap Reference Disabled	I_{STOP}		0.1		µA	2
Supply Current Stop Mode, Bandgap Reference Enabled	I_{SPBG}		40		µA	4, 10
Input Low Level	V_{IL}	-0.3		+0.2 x V_{CC}	V	1
Input High Level (Except XTAL1 and RST)	V_{IH1}	0.7 x V_{CC}		V_{CC}+0.3	V	1
Input High Level XTAL1 and RST	V_{IH2}	0.7 x V_{CC} +0.25V		V_{CC}+0.3	V	1
Output Low Voltage Ports 1, 3 at I_{OL} = 1.6mA	V_{OL1}			0.4	V	1
Output Low Voltage Ports 0, 2, $\overline{PSEN}$ /ALE at I_{OL} = 3.2mA	V_{OL2}			0.4	V	1, 5
Output High Voltage Ports 1, 3, $\overline{PSEN}$ /ALE at I_{OH} = -15µA	V_{OH1}	V_{DD} -0.4V			V	1, 6
Output High Voltage Ports 1, 3 at I_{OH} = -1.5mA	V_{OH2}	V_{DD} -0.4V			V	1, 7
Output High Voltage Ports 0, 2, $\overline{PSEN}$ /ALE at I_{OH} = -2mA	V_{OH3}	V_{DD} -0.4V			V	1, 5
Input Low Current Ports 1, 3 at 0.45V	I_{IL}			-30	µA	11
Transition Current from 1 ≥ 0, Ports 1, 3 at 2V	I_{TL}			-400	µA	8
Input Leakage Port 0, Bus Mode	I_L	-300		+300	µA	9
RST Pulldown Resistance	R_{RST}	50		170	kΩ	

NOTES FOR DS80C323 DC ELECTRICAL CHARACTERISTICS

All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested. Device operating range is 2.7V to 5.5V. DC electrical specifications are for operation 2.7V to 3.3V.

1. All voltages are referenced to ground.
2. Active mode current is measured with an 18MHz clock source driving XTAL1, V_{CC} = RST = 3.3V, all other pins disconnected.
3. Idle mode current is measured with an 18MHz clock source driving XTAL1, V_{CC} = 3.3V, all other pins disconnected.
4. Stop mode current measured with XTAL1 and RST grounded, V_{CC} = 3.3V, all other pins disconnected.
5. When addressing external memory. This specification only applies to the first clock cycle following the transition.

NOTES FOR DS80C323 DC ELECTRICAL CHARACTERISTICS (continued)

All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested. Device operating range is 2.7V to 5.5V. DC electrical specifications are for operation 2.7V to 3.3V.

6. RST = V_{CC}. This condition mimics operation of pins in I/O mode.
7. During a 0-to-1 transition, a one-shot drives the ports hard for two clock cycles. This measurement reflects port in transition mode.
8. Ports 1, 2, and 3 source transition current when being pulled down externally. It reaches its maximum at approximately 2V.
9. V_{IN} between ground and V_{CC} - 0.3V. Not a high-impedance input. This port is a weak address latch because Port 0 is dedicated as an address bus on the DS80C323. Peak current occurs near the input transition point of the latch, approximately 2V.
10. Over the industrial temperature range, this specification has a maximum value of 200µA.
11. This is the current from an external circuit to hold a logic low level on an I/O pin while the corresponding port latch bit is set to 1. This is only the current required to *hold* the low level; transitions from 1 to 0 on an I/O pin will also have to overcome the transition current.
12. Device operating range is 2.7V to 5.5V, however device is tested to 2.5V to ensure proper operation at minimum V_{RST}.

MOVX CHARACTERISTICS—DS80C323

PARAMETER	SYMBOL	VARIABLE CLOCK		UNITS	STRETCH
		MIN	MAX		
$\overline{RD}$ Pulse Width	t_{RLRH}	$2t_{CLCL}$-11		ns	t_{MCS}=0
		t_{MCS}-11			t_{MCS}>0
$\overline{WR}$ Pulse Width	t_{WLWH}	$2t_{CLCL}$-11		ns	t_{MCS}=0
		t_{MCS}-11			t_{MCS}>0
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2t_{CLCL}$-32	ns	t_{MCS}=0
			t_{MCS}-36		t_{MCS}>0
Data Hold After Read	t_{RHDX}	0		ns	
Data Float After Read	t_{RHDZ}		t_{CLCL}-5	ns	t_{MCS}=0
			$2t_{CLCL}$-7		t_{MCS}>0
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL}$-43	ns	t_{MCS}=0
			$1.5t_{CLCL}$-45+t_{MCS}		t_{MCS}>0
Port 0 Address to Valid Data In	t_{AVDV1}		$3t_{CLCL}$-40	ns	t_{MCS}=0
			$2t_{CLCL}$-42+t_{MCS}		t_{MCS}>0
Port 2 Address to Valid Data In	t_{AVDV2}		$3.5t_{CLCL}$-58	ns	t_{MCS}=0
			$2.5t_{CLCL}$-59+t_{MCS}		t_{MCS}>0
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL}$-18	$0.5t_{CLCL}$+7	ns	t_{MCS}=0
		$1.5t_{CLCL}$-11	$1.5t_{CLCL}$+8		t_{MCS}>0
Port 0 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	t_{CLCL}-10		ns	t_{MCS}=0
		$2t_{CLCL}$-10			t_{MCS}>0
Port 2 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL}$-27		ns	t_{MCS}=0
		$2.5t_{CLCL}$-25			t_{MCS}>0
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-14		ns	t_{MCS}=0
		t_{CLCL}-13			t_{MCS}>0
Data Hold After Write	t_{WHQX}	t_{CLCL}-15		ns	t_{MCS}=0
		$2t_{CLCL}$-13			t_{MCS}>0
$\overline{RD}$ Low to Address Float	t_{RLAZ}		(Note 5)	ns	
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{WHLH}	-1	14	ns	t_{MCS}=0
		t_{CLCL}-5	t_{CLCL}+16		t_{MCS}>0

Note: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.

M2	M1	M0	MOVX CYCLES	t_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles (default)	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Clock High Time	t_{CHCX}	10			ns
Clock Low Time	t_{CLCX}	10			ns
Clock Rise Time	t_{CLCH}			5	ns
Clock Fall Time	t_{CHCL}			5	ns

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

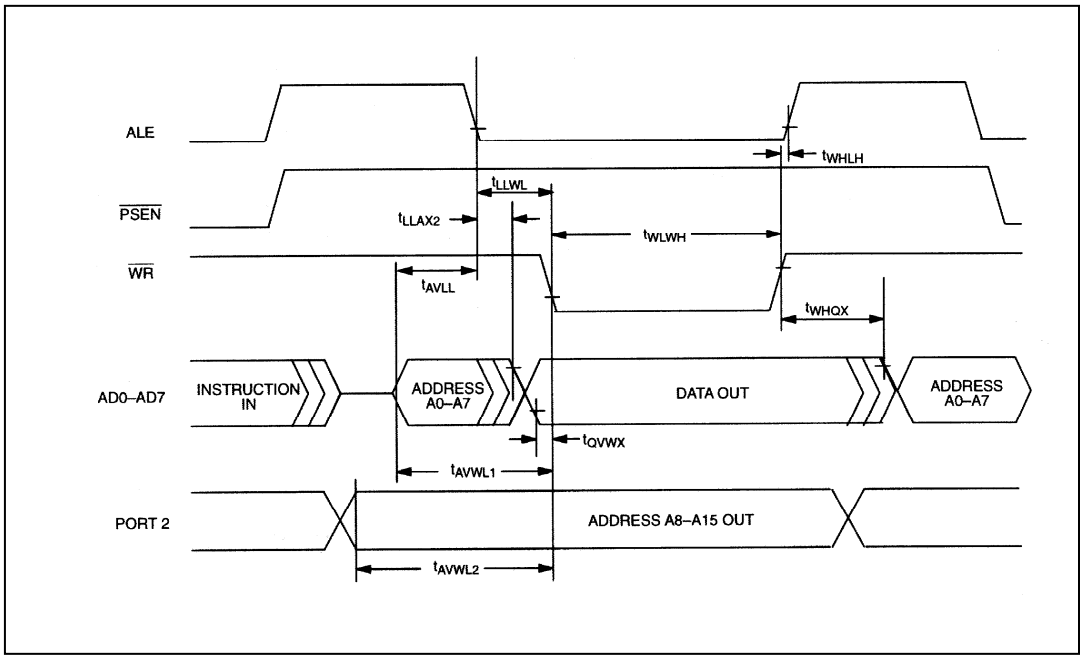
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Port Clock Cycle Time	t_{XLXL}	SM2 = 0; 12 clocks per cycle		$12t_{CLCL}$		ns
		SM2 = 1; 4 clocks per cycle		$4t_{CLCL}$		
Output Data Setup to Clock Rising Edge	t_{QVXH}	SM2 = 0 12 clocks per cycle		$10t_{CLCL}$		ns
		SM2 = 1; 4 clocks per cycle		$3t_{CLCL}$		
Output Data Hold from Clock Rising	t_{XHQX}	SM2 = 0 12 clocks per cycle		$2t_{CLCL}$		ns
		SM2 = 1; 4 clocks per cycle		t_{CLCL}		
Input Data Hold After Clock Rising	t_{XHDX}	SM2 = 0; 12 clocks per cycle		t_{CLCL}		ns
		SM2 = 1; 4 clocks per cycle		t_{CLCL}		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0; 12 clocks per cycle		$11t_{CLCL}$		ns
		SM2 = 1 4 clocks per cycle		$2t_{CLCL}$		

EXPLANATION OF AC SYMBOLS

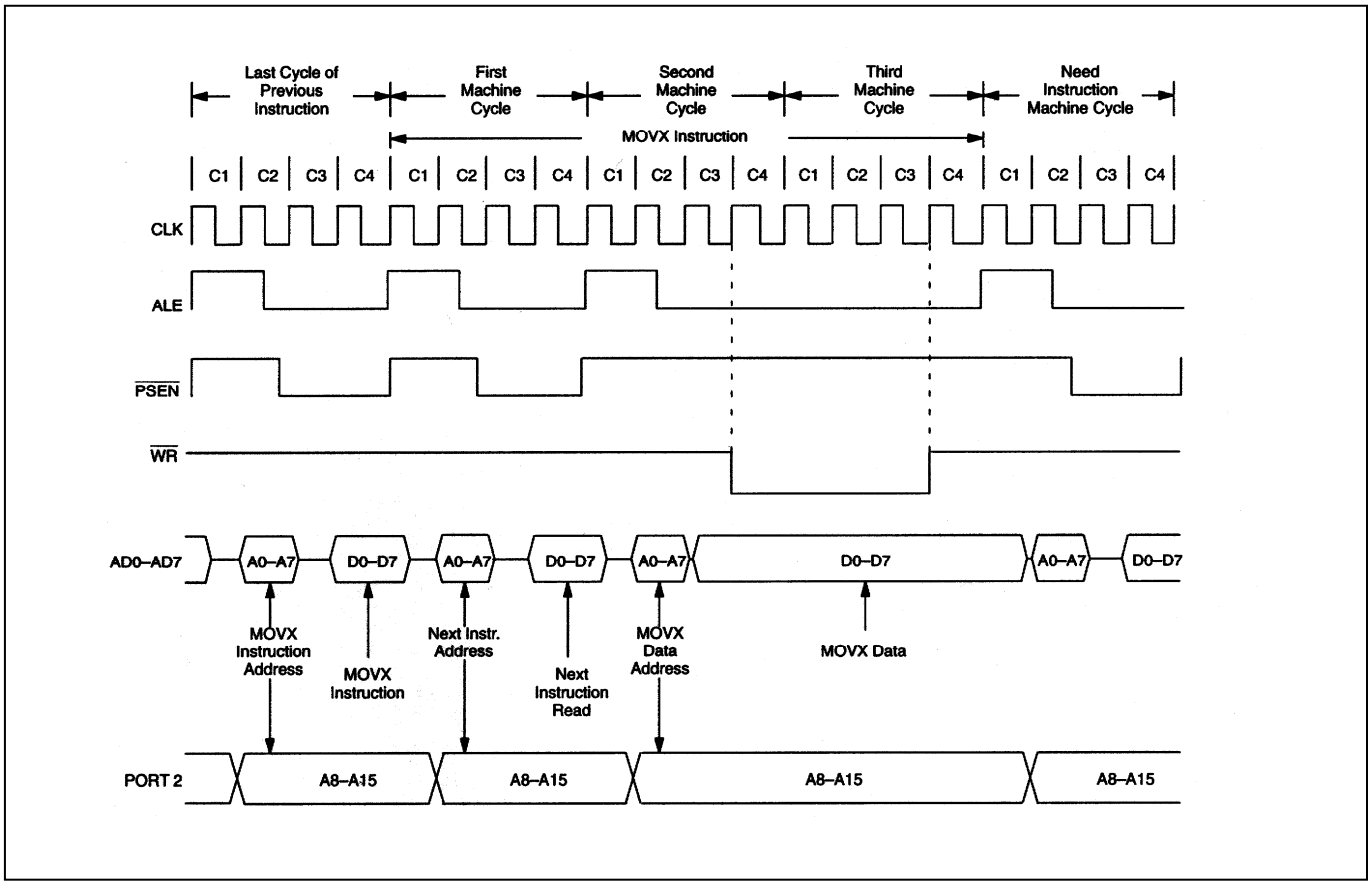
In an effort to remain compatible with the original 8051 family, this device specifies the same parameter as such devices, using the same symbols. For completeness, the following is an explanation of the symbols.

t	Time
A	Address
C	Clock
D	Input data
H	Logic level high
L	Logic level low
I	Instruction
P	$\overline{\text{PSEN}}$
Q	Output data
R	$\overline{\text{RD}}$ signal
V	Valid
W	$\overline{\text{WR}}$ signal
X	No longer a valid logic level
Z	Tri-state

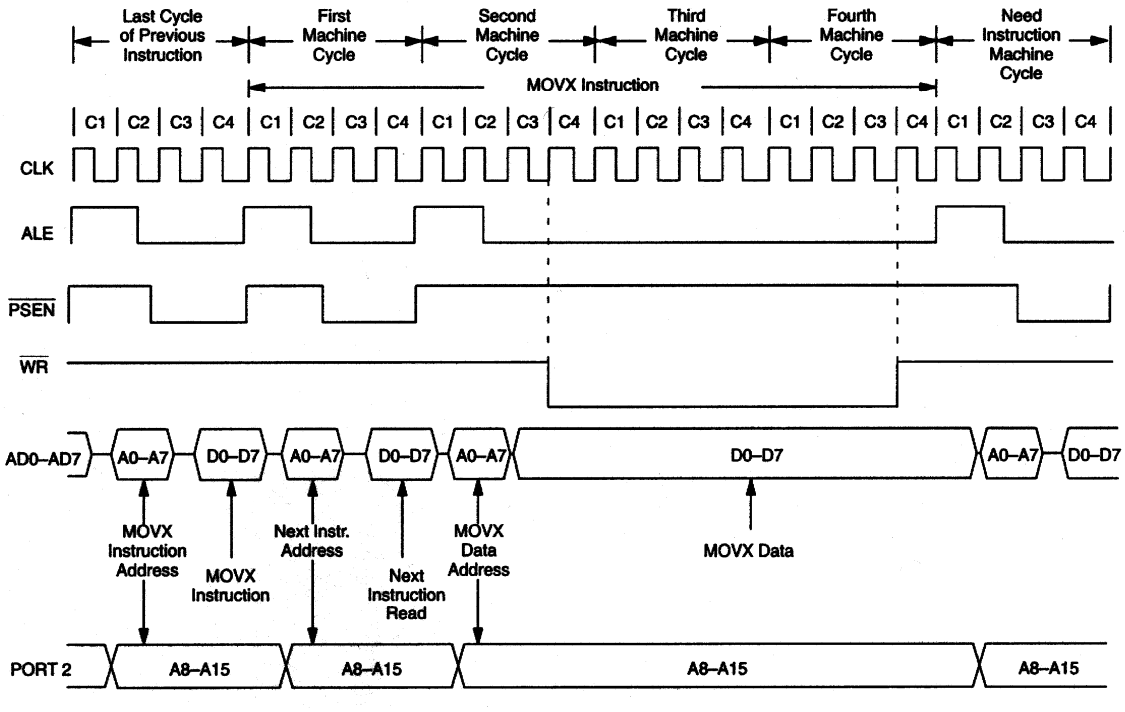
DATA MEMORY WRITE CYCLE



DATA MEMORY WRITE WITH STRETCH = 1

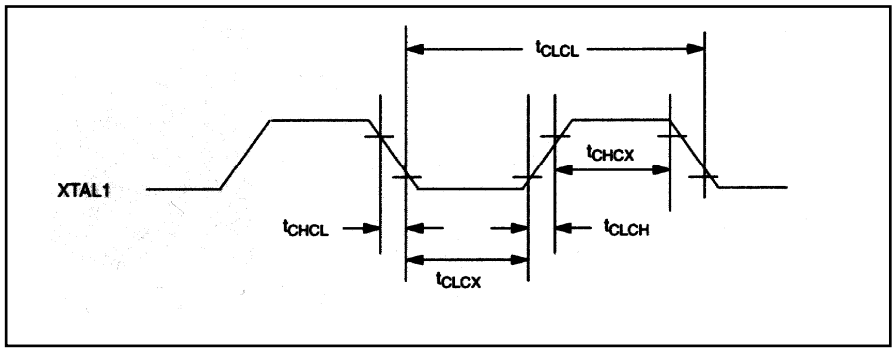


DATA MEMORY WRITE WITH STRETCH = 2

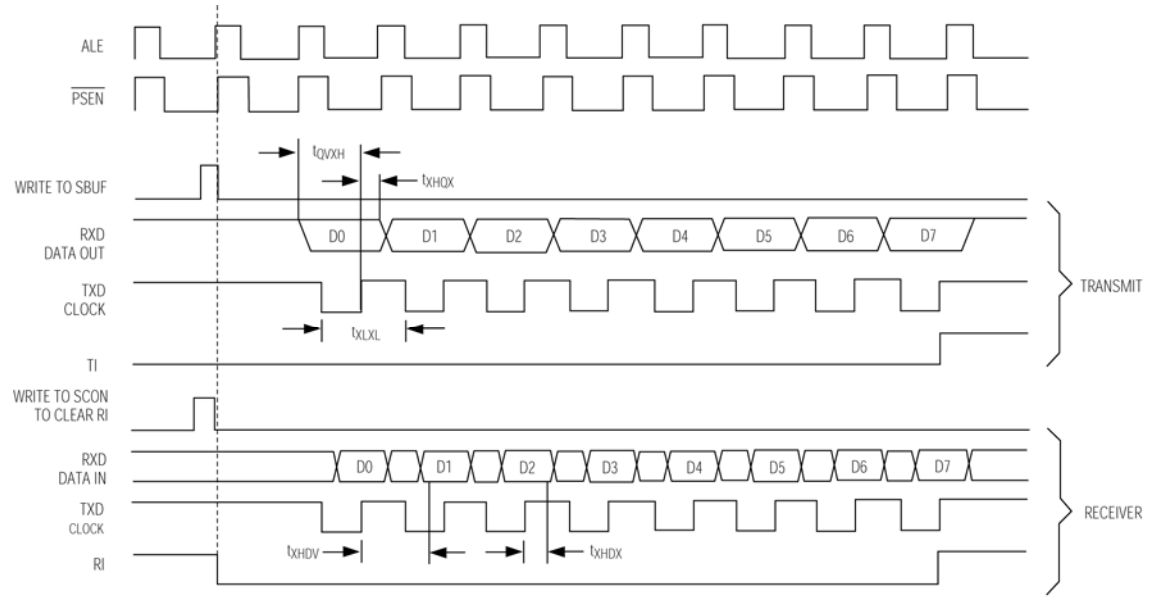


4-CYCLE DATA MEMORY WRITE
STRETCH VALUE = 2

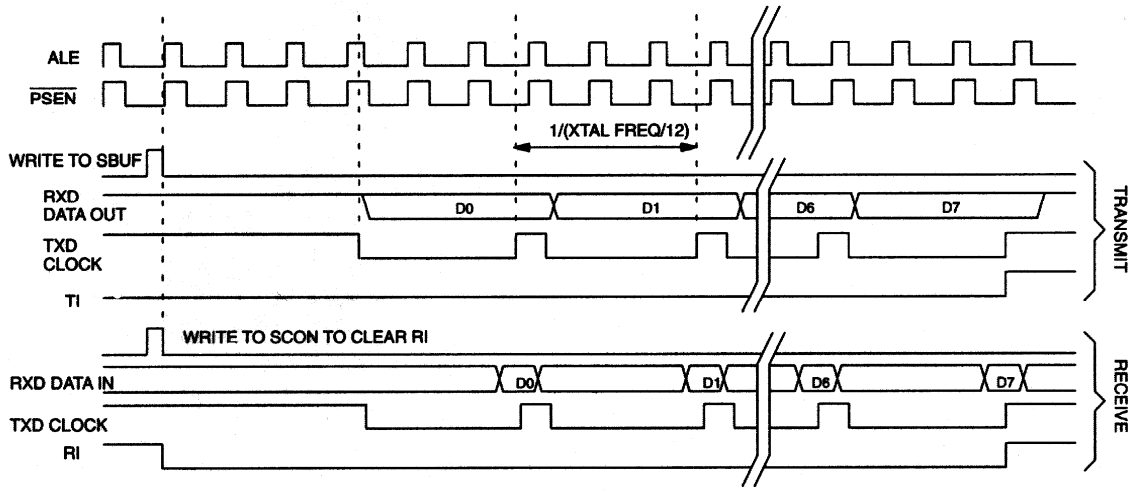
EXTERNAL CLOCK DRIVE



SERIAL PORT MODE 0 TIMING

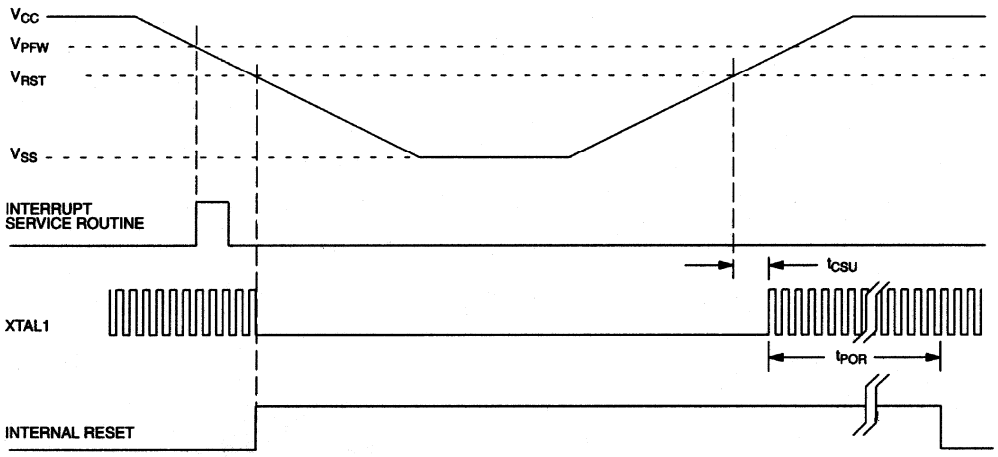


SERIAL PORT 0 (SYNCHRONOUS MODE)
HIGH SPEED OPERATION SM2 = 1 ≥ TXD CLOCK = XTAL/4



SERIAL PORT 0 (SYNCHRONOUS MODE)
SM2 = 0 ≥ TXD CLOCK = XTAL/12

POWER-CYCLE TIMING



PACKAGE INFORMATION

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
44 TQFP	C44+2	**21-0293**
44 MQFP	M44+10	**21-0269**
44 MQFP	M44+5	**21-0826**
40 PDIP	P40+1	**21-0044**
44 PLCC	Q44+1	**21-0049**

DATA SHEET REVISION SUMMARY (continued)

The following represent the key differences between the 05/22/96 and the 10/21/97 version of the DS80C320 data sheet. Please review this summary carefully.

DS80C320

1. Added note to clarify I_{IL} specification.
2. Added note to clarify AC timing conditions.
3. Corrected erroneous t_{QVXL} label on figure "Serial Port Mode 0 Timing" to read t_{QVXH}.
4. Added note to prevent accidental corruption of Watchdog Timer count while changing counter length.

DS80C323

1. Added note to clarify I_{IL} specification.
2. Remove port 2 from V_{OH1} specification, add port 3.
3. I_{OH} for V_{OH3} specification changed from -3mA to -2mA.
4. Added note to clarify AC timing conditions.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600