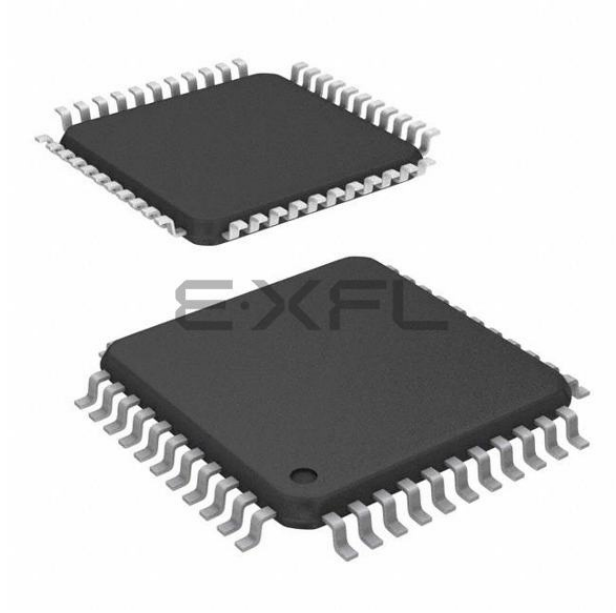
Analog Devices Inc./Maxim Integrated - DS80C320-ENG+ Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds80c320-eng

DETAILED DESCRIPTION

The DS80C320/DS80C323 are fast 80C31/80C32-compatible microcontrollers. Wasted clock and memory cycles have been removed using a redesigned processor core. As a result, every 8051 instruction is executed between 1.5 and 3 times faster than the original for the same crystal speed. Typical applications see a speed improvement of 2.5 times using the same code and same crystal. The DS80C320 offers a maximum crystal rate of 33MHz, resulting in apparent execution speeds of 82.5MHz (approximately 2.5X).

The DS80C320/DS80C323 are pin compatible with all three packages of the standard 80C32 and offer the same timer/counters, serial port, and I/O ports. In short, the devices are extremely familiar to 8051 users, but provide the speed of a 16-bit processor.

The DS80C320 provides several extras in addition to greater speed. These include a second full hardware serial port, seven additional interrupts, programmable watchdog timer, power-fail interrupt and reset. The device also provides dual data pointers (DPTRs) to speed block data memory moves. It can also adjust the speed of off-chip data memory access to between two and nine machine cycles for flexibility in selecting memory and peripherals.

The DS80C320 operating voltage ranges from 4.25V to 5.5V, making it ideal as a high-performance upgrade to existing 5V systems. For applications in which power consumption is critical, the DS80C323 offers the same feature set as the DS80C320, but with 2.7V to 5.5V operation.

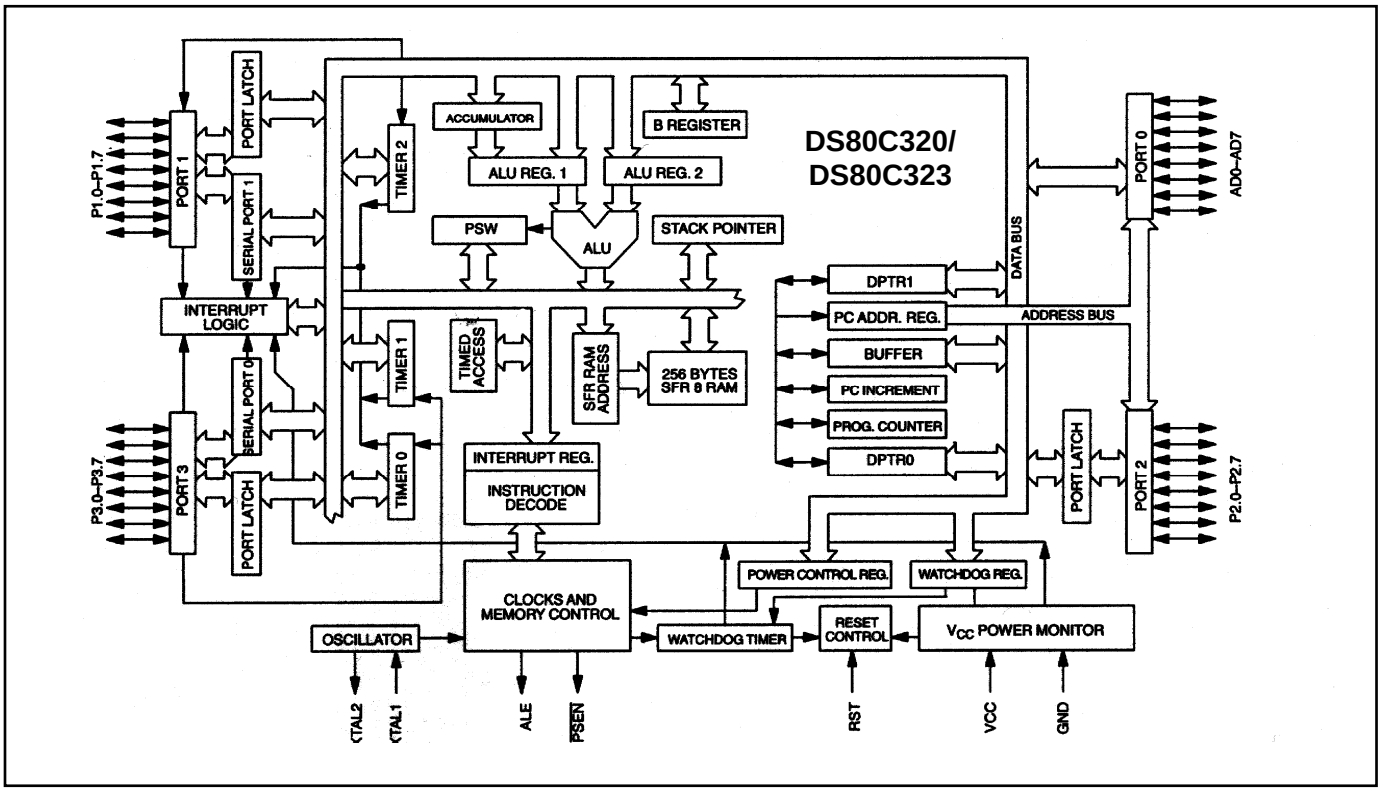
Designers must have two documents to fully use all the features of this device: this data sheet and the *High-Speed Microcontroller User's Guide*, available on our website at www.maxim-ic.com/microcontrollers. Data sheets contain pin descriptions, feature overviews, and electrical specifications, whereas our user's guides contain detailed information about device features and operation.

ORDERING INFORMATION

PART	Pb-FREE/RoHS-COMPLIANT	TEMP RANGE	MAX CLOCK SPEED (MHz)	PIN-PACKAGE
DS80C320-MCG	**DS80C320**-MCG+	0°C to +70°C	25	40 Plastic DIP
DS80C320-QCG	DS80C320-QCG+	0°C to +70°C	25	44 PLCC
DS80C320-ECG	DS80C320-ECG+	0°C to +70°C	25	44 TQFP
DS80C320-MNG	DS80C320-MNG+	-40°C to +85°C	25	40 Plastic DIP
DS80C320-QNG	DS80C320-QNG+	-40°C to +85°C	25	44 PLCC
DS80C320-ENG	DS80C320-ENG+	-40°C to +85°C	25	44 TQFP
DS80C320-MCL	DS80C320-MCL+	0°C to +70°C	33	40 Plastic DIP
DS80C320-QCL	DS80C320-QCL+	0°C to +70°C	33	44 PLCC
DS80C320-ECL	DS80C320-ECL+	0°C to +70°C	33	44 TQFP
DS80C320-MNL	DS80C320-MNL+	-40°C to +85°C	33	40 Plastic DIP
DS80C320-QNL	DS80C320-QNL+	-40°C to +85°C	33	44 PLCC
DS80C320-ENL	DS80C320-ENL+	-40°C to +85°C	33	44 TQFP
DS80C323-MCD	**DS80C323**-MCD+	0°C to +70°C	18	40 Plastic DIP
DS80C323-QCD	DS80C323-QCD+	0°C to +70°C	18	44 PLCC
DS80C323-ECD	DS80C323-ECD+	0°C to +70°C	18	44 TQFP
DS80C323-QND	DS80C323-QND+	-40°C to +85°C	18	44 PLCC
DS80C323-END	DS80C323-END+	-40°C to +85°C	18	44 TQFP

+ Denotes a lead(Pb)-free/RoHS-compliant device.

Figure 1. Block Diagram



PIN DESCRIPTION

PIN			NAME	FUNCTION
DIP	PLCC	TQFP		
40	44	38	V_{CC}	**+5V (+3V for DS80C323)**
20	22, 23	16, 17	GND	**Digital Circuit Ground**
9	10	4	RST	**Reset Input.** The RST input pin contains a Schmitt voltage input to recognize external active-high reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wired OR external reset sources. An RC is ***not*** required for power-up, as the device provides this function internally.
18	20	14	XTAL2	**Crystal Oscillator Pins.** XTAL1 and XTAL2 provide support for parallel-resonant, AT-cut crystals. XTAL1 acts also as an input in the event that an external clock source is used in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
19	21	15	XTAL1	
29	32	26	$\overline{\text{PSEN}}$	**Program Store-Enable Output, Active Low.** This signal is commonly connected to external ROM memory as a chip enable. $\overline{\text{PSEN}}$ provides an active-low pulse width of 2.25 XTAL1 cycles with a period of four XTAL1 cycles. $\overline{\text{PSEN}}$ is driven high when data memory (RAM) is being accessed through the bus and during a reset condition.

PIN DESCRIPTION (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>TQFP</th></tr>
<tr><td>30</td><td>33</td><td>27</td><td>ALE</td><td>Address Latch-Enable Output. This pin functions as a clock to latch the external address LSB from the multiplexed address/data bus. This signal is commonly connected to the latch enable of an external 373 family transparent latch. ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. ALE is forced high when the device is in a reset condition.</td></tr>
<tr><td>39</td><td>43</td><td>37</td><td>AD0</td><td rowspan="8">Port 0, Input/Output. Port 0 is the multiplexed address/data bus. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls, the port transitions to a bidirectional data bus. This bus is used to read external ROM and read/write external RAM memory or peripherals. The Port 0 has no true port latch and cannot be written directly by software. The reset condition of Port 0 is high. No pullup resistors are needed.</td></tr>
<tr><td>38</td><td>42</td><td>36</td><td>AD1</td></tr>
<tr><td>37</td><td>41</td><td>35</td><td>AD2</td></tr>
<tr><td>36</td><td>40</td><td>34</td><td>AD3</td></tr>
<tr><td>35</td><td>39</td><td>33</td><td>AD4</td></tr>
<tr><td>34</td><td>38</td><td>32</td><td>AD5</td></tr>
<tr><td>33</td><td>37</td><td>31</td><td>AD6</td></tr>
<tr><td>32</td><td>36</td><td>30</td><td>AD7</td></tr>
<tr><td>1–8</td><td>2–9</td><td>40–44, 1–3</td><td>P1.0–P1.7</td><td>Port 1, I/O. Port 1 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for Timer 2 I/O, new External Interrupts, and new Serial Port 1. The reset condition of Port 1 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the device will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port once again becomes the output high (and input) state. The alternate modes of Port 1 are outlined as follows:
<table>
<tr><th colspan="3">PIN</th><th rowspan="2">PORT</th><th rowspan="2">ALTERNATE</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>TQFP</th></tr>
<tr><td>1</td><td>2</td><td>40</td><td>P1.0</td><td>T2</td><td>External I/O for Timer/Counter 2</td></tr>
<tr><td>2</td><td>3</td><td>41</td><td>P1.1</td><td>T2EX</td><td>Timer/Counter 2 Capture/Reload Trigger</td></tr>
<tr><td>3</td><td>4</td><td>42</td><td>P1.2</td><td>RXD1</td><td>Serial Port 1 Input</td></tr>
<tr><td>4</td><td>5</td><td>43</td><td>P1.3</td><td>TXD1</td><td>Serial Port 1 Output</td></tr>
<tr><td>5</td><td>6</td><td>44</td><td>P1.4</td><td>INT2</td><td>External Interrupt 2 (Positive-Edge Detect)</td></tr>
<tr><td>6</td><td>7</td><td>1</td><td>P1.5</td><td>$\overline{\text{INT3}}$</td><td>External Interrupt 3 (Negative-Edge Detect)</td></tr>
<tr><td>7</td><td>8</td><td>2</td><td>P1.6</td><td>INT4</td><td>External Interrupt 4 (Positive-Edge Detect)</td></tr>
<tr><td>8</td><td>9</td><td>3</td><td>P1.7</td><td>$\overline{\text{INT5}}$</td><td>External Interrupt 5 (Negative-Edge Detect)</td></tr>
</table>
</td></tr>
</table>

80C32 COMPATIBILITY

The DS80C320/DS80C323 are CMOS 80C32-compatible microcontrollers designed for high performance. In most cases, the devices will drop into an existing 80C32 design to significantly improve the operation. Every effort has been made to keep the devices familiar to 8032 users, yet they have many new features. In general, software written for existing 80C32-based systems will work on the DS80C320 and DS80C323. The exception is critical timing, because the high-speed microcontroller performs its instructions much faster than the original. It may be necessary to use memories with faster access times if the same crystal frequency is used.

Application Note 57: DS80C320 Memory Interface Timing is a useful tool to help the embedded system designer select the proper memories for her or his application.

The DS80C320/DS80C323 run the standard 8051 instruction set and is pin compatible with an 80C32 in any of three standard packages. They also provide the same timer/counter resources, full-duplex serial port, 256 bytes of scratchpad RAM, and I/O ports as the standard 80C32. Timers will default to a 12 clock-per-cycle operation to keep timing compatible with original 8051 systems. However, they can be programmed to run at the new 4 clocks per cycle if desired.

New hardware features are accessed using special-function registers that do not overlap with standard 80C32 locations. A summary of these SFRs is provided below.

The DS80C320/DS80C323 address memory in an identical fashion to the standard 80C32. Electrical timing appears different due to the high-speed nature of the product. However, the signals are essentially the same. Detailed timing diagrams are provided in the *Electrical Specifications* section.

This data sheet assumes the user is familiar with the basic features of the standard 80C32. In addition to these standard features, the DS80C320/DS80C323 include many new functions. This data sheet provides only a summary and overview. Detailed descriptions are available in the *High-Speed Microcontroller User's Guide*.

INSTRUCTION SET SUMMARY

All instructions in the DS80C320/DS80C323 perform the same functions as their 80C32 counterparts. Their effect on bits, flags, and other status functions is identical. However, the timing of each instruction is different. This applies both in absolute and relative number of clocks.

For absolute timing of real-time events, the timing of software loops will need to be calculated using the Table 1. However, counter/timers default to run at the older 12 clocks per increment. Therefore, while software runs at higher speed, timer-based events need no modification to operate as before. Timers can be set to run at 4 clocks per increment cycle to take advantage of higher speed operation.

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture, the “MOVX A, @DPTR” instruction and the “MOV direct, direct” instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS80C320/DS80C323, the MOVX instruction can be done in two machine cycles or eight oscillator cycles, but the “MOV direct, direct” uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times from each other. This is because in most cases, the DS80C320/DS80C323 use one cycle for each byte. The user concerned with precise program timing should examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just four clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV.

immediately preceding the setting of the Stop bit to guarantee a correct power-on delay when exiting Stop mode.

The second feature allows an additional power saving option. This is the ability to start instantly when exiting Stop mode. It is accomplished using an internal ring oscillator that can be used when exiting Stop mode in response to an interrupt. The benefit of the ring oscillator is as follows.

Using Stop mode turns off the crystal oscillator and all internal clocks to save power. This requires that the oscillator be restarted when exiting Stop mode. Actual start-up time is crystal dependent, but is normally at least 4ms. A common recommendation is 10ms. In an application that will wakeup, perform a short operation, then return to sleep, the crystal startup can be longer than the real transaction. However, the ring oscillator will start instantly. The user can perform a simple operation and return to sleep before the crystal has even stabilized. If the ring is used to start and the processor remains running, hardware will automatically switch to the crystal once a power-on reset interval (65,536 clocks) has expired. This value is used to guarantee stability even though power is not being cycled.

If the user returns to Stop mode prior to switching of crystal, then all clocks will be turned off again. The ring oscillator runs at approximately 3MHz (1.5MHz at 3V) but will not be a precision value. No real-time precision operations (including serial communication) should be conducted during this ring period. Figure 4 shows how the operation would compare when using the ring, and when starting up normally. The default state is to come out of Stop mode without using the ring oscillator.

This function is controlled using the RGSL - Ring Select bit at EXIF.1 (EXIF to 91h). When EXIF.1 is set, the ring oscillator will be used to come out of Stop mode quickly. As mentioned above, the processor will automatically switch from the ring (if enabled) to the crystal after a delay of 65,536 crystal clocks. For a 3.57MHz crystal, this is approximately 18ms. The processor sets a flag called RGMD - Ring Mode to tell software that the ring is being used. This bit at EXIF.2 will be logic 1 when the ring is in use. No serial communication or precision timing should be attempted while this bit is set, since the operating frequency is not precise.

SPECIAL-FUNCTION REGISTERS

Most special features of the DS80C320/DS80C323 or 80C32 are controlled by bits in the SFRs, allowing the devices to add many features but use the same instruction set. When writing software to use a new feature, the SFR must be defined to an assembler or compiler using an equate statement. This is the only change needed to access the new function. The DS80C320/DS80C323 duplicate the SFRs that are contained in the standard 80C32. Table 5 shows the register addresses and bit locations. Many are standard 80C32 registers. The *High-Speed Microcontroller User's Guide* describes all SFRs.

Table 5. Special-Function Register Locations

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**SEL**	86h
PCON	SMOD_0	**SMOD0**	—	—	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	**WD1**	**WD0**	**T2M**	**T1M**	**T0M**	**MD2**	**MD1**	**MD0**	8Eh
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
EXIF	**IE5**	**IE4**	**IE3**	**IE2**	—	**RGMD**	**RGSL**	**BGS**	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
P2	P2.0	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	A8h
SADDR0									A9h
SADDR1									AAh
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
IP	—	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
SCON1	**SM0/FE_0**	**SM1_0**	**SM2_0**	**REN_0**	**TB8_0**	**RB8_0**	**TI_0**	**RI_0**	C0h
SBUF1									C1h
STATUS	PIP	HIP	LIP	1	1	1	1	1	C5h
TA									C7h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	C8h
T2MOD	—	—	—	—	—	—	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	FL	P	D0h
WDCON	**SMOD_1**	**POR**	**EPFI**	**PFI**	**WDIF**	**WTRF**	**EWT**	**RWT**	D8h
ACC									E0h
EIE	—	—	—	**EWDI**	**EX5**	**EX4**	**EX3**	**EX2**	E8h
B									F0h
EIP	—	—	—	**PWDI**	**PX5**	**PX4**	**PX3**	**PX2**	F8h

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground……..-0.3V to +6.0V
Operating Temperature Range……-40°C to +85°C
Storage Temperature Range……..-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS—DS80C320

(V_{CC} = 4.5V to 5.5V, T_A = -40°C to +85°C.)

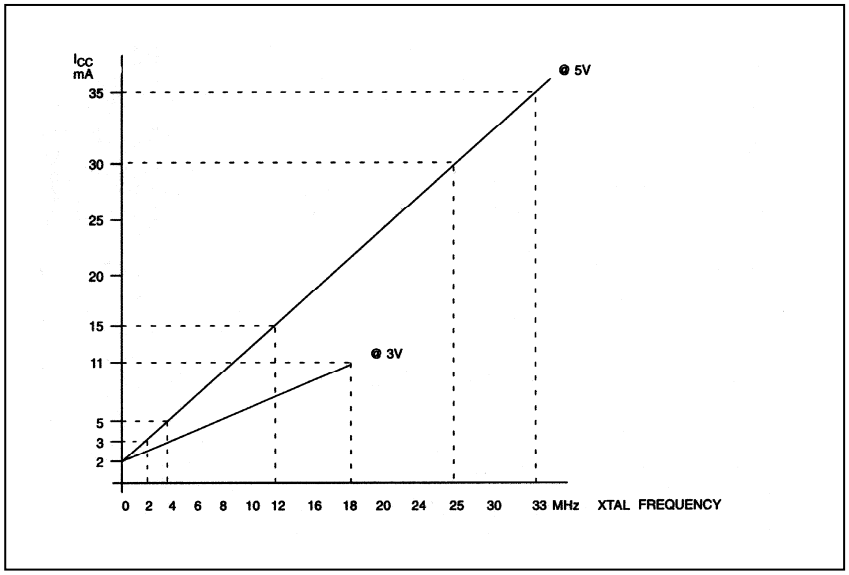
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Power-Fail Warning Voltage	V_{PFW}	4.25	4.38	4.55	V	1
Minimum Operating Voltage	V_{RST}	4.0	4.1	4.25	V	1, 12
Supply Current Active Mode at 25MHz	I_{CC}		30	45	mA	2
Supply Current Idle Mode at 25MHz	I_{IDLE}		15	25	mA	3
Supply Current Active Mode at 33MHz	I_{CC}		35		mA	2
Supply Current Idle Mode at 33MHz	I_{IDLE}		20		mA	3
Supply Current Stop Mode, Bandgap Reference Disabled	I_{STOP}		0.01	1	µA	4
Supply Current Stop Mode, Bandgap Reference Enabled	I_{SPBG}		50	80	µA	4, 10
Input Low Level	V_{IL}	-0.3		+0.8	V	1
Input High Level (Except XTAL1 and RST)	V_{IH1}	2.0		V_{CC} + 0.3	V	1
Input High Level XTAL1 and RST	V_{IH2}	3.5		V_{CC} + 0.3	V	1
Output-Low Voltage Ports 1, 3 at I_{OL} = 1.6mA	V_{OL1}			0.45	V	1
Output-Low Voltage Ports 0, 2, ALE, $\overline{PSEN}$ at I_{OL} = 3.2mA	V_{OL2}			0.45	V	1, 5
Output-High Voltage Ports 1, 3, ALE, $\overline{PSEN}$ at I_{OH} = -50µA	V_{OH1}	2.4			V	1, 6
Output High Voltage Ports 1, 3 at I_{OH} = -1.5mA	V_{OH2}	2.4			V	1, 7
Output-High Voltage Ports 0, 2, ALE, $\overline{PSEN}$ at I_{OH} = -8mA	V_{OH3}	2.4			V	1, 5
Input Low Current Ports 1, 3 at 0.45V	I_{IL}			-55	µA	11
Transition Current from 1 to 0 Ports 1, 3 at 2V	I_{TL}			-650	µA	8
Input Leakage Port 0, Bus Mode	I_L	-300		+300	µA	9
RST Pulldown Resistance	R_{RST}	50		170	kΩ	

NOTES FOR DS80C320 DC ELECTRICAL CHARACTERISTICS

All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested.

1. All voltages are referenced to ground.
2. Active current is measured with a 25MHz clock source driving XTAL1, V_{CC} = RST = 5.5V, all other pins disconnected.
3. Idle mode current is measured with a 25MHz clock source driving XTAL1, V_{CC} = 5.5V, RST at ground, all other pins disconnected.
4. Stop mode current measured with XTAL1 and RST grounded, V_{CC} = 5.5V, all other pins disconnected.
5. When addressing external memory. This specification only applies to the first clock cycle following transition.
6. RST = V_{CC}. This condition mimics operation of pins in I/O mode.
7. During a 0-to-1 transition, a one-shot drives the ports hard for two clock cycles. This measurement reflects port in transition mode.
8. Ports 1 and 3 source transition current when being pulled down externally. It reaches its maximum at approximately 2V.
9. $0.45<V_{IN}<V_{CC}$. Not a high-impedance input. This port is a weak address holding latch because Port 0 is dedicated as an address bus on the DS80C320. Peak current occurs near the input transition point of the latch, approximately 2V.
10. Over the industrial temperature range, this specification has a maximum value of 200µA.
11. This is the current required from an external circuit to hold a logic low level on an I/O pin while the corresponding port latch bit is set to 1. This is only the current required to *hold* the low level; transitions from 1 to 0 on an I/O pin will also have to overcome the transition current.
12. Device operating range is 4.5V to 5.5V; however, device is tested to 4.0V to ensure proper operation at minimum V_{RST}.

TYPICAL I_{CC} vs. FREQUENCY



AC CHARACTERISTICS—DS80C320

PARAMETER		SYMBOL	33MHz		VARIABLE CLOCK		UNITS
			MIN	MAX	MIN	MAX	
Oscillator Frequency	External Oscillator	$1/t_{CLCL}$	0	33	0	33	MHz
	External Crystal		1	33	1	33	
ALE Pulse Width		t_{LHLL}	34		$1.5t_{CLCL}$-11		ns
Port 0 Address Valid to ALE Low		t_{AVLL}	4		$0.5t_{CLCL}$-11		ns
Address Hold After ALE Low		t_{LLAX1}	2	(Note 5)	$0.25t_{CLCL}$-5	(Note 5)	ns
Address Hold After ALE Low for MOVX $\overline{WR}$		t_{LLAX2}	6		$0.5t_{CLCL}$-9		ns
ALE Low to Valid Instruction In		t_{LLIV}		49		$2.5t_{CLCL}$-27	ns
ALE Low to $\overline{PSEN}$ Low		t_{LLPL}	0.5		$0.25t_{CLCL}$-7		ns
$\overline{PSEN}$ Pulse Width		t_{PLPH}	61		$2.25t_{CLCL}$-7		ns
$\overline{PSEN}$ Low to Valid Instruction In		t_{PLIV}		48		$2.25t_{CLCL}$-21	ns
Input Instruction Hold After $\overline{PSEN}$		t_{PXIX}	0		0		ns
Input Instruction Float After $\overline{PSEN}$		t_{PXIZ}		25		t_{CLCL}-5	ns
Port 0 Address to Valid Instruction In		t_{AVIV1}		64		$3t_{CLCL}$-27	ns
Port 2 Address to Valid Instruction In		t_{AVIV2}		73		$3.5t_{CLCL}$-33	ns
$\overline{PSEN}$ Low to Address Float		t_{PLAZ}		(Note 5)		(Note 5)	ns

NOTES FOR DS80C320 AC ELECTRICAL CHARACTERISTICS

All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested. AC electrical characteristics assume 50% duty cycle for the oscillator, oscillator frequency > 16MHz, and are not 100% tested, but are guaranteed by design.

1. All signals rated over operating temperature at 33MHz.
2. All signals characterized with load capacitance of 80pF except Port 0, ALE, $\overline{PSEN}$, $\overline{RD}$ and $\overline{WR}$ at 100pF. Note that loading should be approximately equal for valid timing.
3. Interfacing to memory devices with float times (turn off times) over 30ns may cause contention. This will not damage the parts but will cause an increase in operating current.
4. Specifications assume a 50% duty cycle for the oscillator. Port 2 timing will change with the duty cycle variations.
5. Address is held in a weak latch until over driven by external memory.

MOVX CHARACTERISTICS—DS80C320

PARAMETER	SYMBOL	VARIABLE CLOCK		UNITS	STRETCH
		MIN	MAX		
$\overline{RD}$ Pulse Width	t_{RLRH}	$2t_{CLCL}$-11		ns	t_{MCS}=0
		t_{MCS}-11			t_{MCS}>0
$\overline{WR}$ Pulse Width	t_{WLWH}	$2t_{CLCL}$-11		ns	t_{MCS}=0
		t_{MCS}-11			t_{MCS}>0
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2t_{CLCL}$-25	ns	t_{MCS}=0
			t_{MCS}-25		t_{MCS}>0
Data Hold After Read	t_{RHDX}	0		ns	
Data Float After Read	t_{RHDZ}		t_{CLCL}-5	ns	t_{MCS}=0
			$2t_{CLCL}$-5		t_{MCS}>0
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL}$-27	ns	t_{MCS}=0
			$1.5t_{CLCL}$-28+t_{MCS}		t_{MCS}>0
Port 0 Address to Valid Data In	t_{AVDV1}		$3t_{CLCL}$-27	ns	t_{MCS}=0
			$2t_{CLCL}$-31+t_{MCS}		t_{MCS}>0
Port 2 Address to Valid Data In	t_{AVDV2}		$3.5t_{CLCL}$-32	ns	t_{MCS}=0
			$2.5t_{CLCL}$-34+t_{MCS}		t_{MCS}>0
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL}$-8	$0.5t_{CLCL}$+6	ns	t_{MCS}=0
		$1.5t_{CLCL}$-7	$1.5t_{CLCL}$+8		t_{MCS}>0
Port 0 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	t_{CLCL}-11		ns	t_{MCS}=0
		$2t_{CLCL}$-10			t_{MCS}>0
Port 2 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL}$-9		ns	t_{MCS}=0
		$2.5t_{CLCL}$-13			t_{MCS}>0
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-9		ns	t_{MCS}=0
		t_{CLCL}-10			t_{MCS}>0
Data Hold After Write	t_{WHQX}	t_{CLCL}-12		ns	t_{MCS}=0
		$2t_{CLCL}$-7			t_{MCS}>0
$\overline{RD}$ Low to Address Float	t_{RLAZ}		(Note 5)	ns	
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{WHLH}	0	10	ns	t_{MCS}=0
		t_{CLCL}-5	t_{CLCL}+11		t_{MCS}>0

Note: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.

M2	M1	M0	MOVX CYCLES	t_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles (default)	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

DC ELECTRICAL CHARACTERISTICS—DS80C323

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Voltage	V_{CC}	2.7	3.0	5.5	V	1
Power-Fail Warning Voltage	V_{PFW}	2.6	2.7	2.8	V	1
Minimum Operating Voltage	V_{RST}	2.5	2.6	2.7	V	1, 12
Supply Current Active Mode at 18MHz	I_{CC}		10		mA	2
Supply Current Idle Mode at 18MHz	I_{IDLE}		6		mA	3
Supply Current Stop Mode, Bandgap Reference Disabled	I_{STOP}		0.1		µA	2
Supply Current Stop Mode, Bandgap Reference Enabled	I_{SPBG}		40		µA	4, 10
Input Low Level	V_{IL}	-0.3		+0.2 x V_{CC}	V	1
Input High Level (Except XTAL1 and RST)	V_{IH1}	0.7 x V_{CC}		V_{CC}+0.3	V	1
Input High Level XTAL1 and RST	V_{IH2}	0.7 x V_{CC} +0.25V		V_{CC}+0.3	V	1
Output Low Voltage Ports 1, 3 at I_{OL} = 1.6mA	V_{OL1}			0.4	V	1
Output Low Voltage Ports 0, 2, $\overline{PSEN}$ /ALE at I_{OL} = 3.2mA	V_{OL2}			0.4	V	1, 5
Output High Voltage Ports 1, 3, $\overline{PSEN}$ /ALE at I_{OH} = -15µA	V_{OH1}	V_{DD} -0.4V			V	1, 6
Output High Voltage Ports 1, 3 at I_{OH} = -1.5mA	V_{OH2}	V_{DD} -0.4V			V	1, 7
Output High Voltage Ports 0, 2, $\overline{PSEN}$ /ALE at I_{OH} = -2mA	V_{OH3}	V_{DD} -0.4V			V	1, 5
Input Low Current Ports 1, 3 at 0.45V	I_{IL}			-30	µA	11
Transition Current from 1 ≥ 0, Ports 1, 3 at 2V	I_{TL}			-400	µA	8
Input Leakage Port 0, Bus Mode	I_L	-300		+300	µA	9
RST Pulldown Resistance	R_{RST}	50		170	kΩ	

NOTES FOR DS80C323 DC ELECTRICAL CHARACTERISTICS

All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested. Device operating range is 2.7V to 5.5V. DC electrical specifications are for operation 2.7V to 3.3V.

1. All voltages are referenced to ground.
2. Active mode current is measured with an 18MHz clock source driving XTAL1, V_{CC} = RST = 3.3V, all other pins disconnected.
3. Idle mode current is measured with an 18MHz clock source driving XTAL1, V_{CC} = 3.3V, all other pins disconnected.
4. Stop mode current measured with XTAL1 and RST grounded, V_{CC} = 3.3V, all other pins disconnected.
5. When addressing external memory. This specification only applies to the first clock cycle following the transition.

AC ELECTRICAL CHARACTERISTICS—DS80C323

PARAMETER		SYMBOL	18 MHz		VARIABLE CLOCK		UNITS
			MIN	MAX	MIN	MAX	
Oscillator Frequency	External Oscillator	$1/t_{CLCL}$	0	18	0	18	MHz
	External Crystal		1	18	1	18	
ALE Pulse Width		t_{LHLL}	68		$1.5t_{CLCL}$-15		ns
Port 0 Address Valid to ALE Low		t_{AVLL}	16		$0.5t_{CLCL}$-11		ns
Address Hold After ALE Low		t_{LLAX1}	6	(Note 5)	$0.25t_{CLCL}$-8	(Note 5)	ns
Address Hold After ALE Low for MOVX $\overline{WR}$		t_{LLAX2}	14		$0.5t_{CLCL}$-13		ns
ALE Low to Valid Instruction In		t_{LLIV}		93		$2.5t_{CLCL}$-46	ns
ALE Low to $\overline{PSEN}$ Low		t_{LLPL}	4		$0.25t_{CLCL}$-10		ns
$\overline{PSEN}$ Pulse Width		t_{PLPH}	118		$2.25t_{CLCL}$-7		ns
$\overline{PSEN}$ Low to Valid Instruction In		t_{PLIV}		87		$2.25t_{CLCL}$-38	ns
Input Instruction Hold After $\overline{PSEN}$		t_{PXIX}	0		0		ns
Input Instruction Float After $\overline{PSEN}$		t_{PXIZ}		51		t_{CLCL}-5	ns
Port 0 Address to Valid Instruction In		t_{AVIV1}		128		$3t_{CLCL}$-39	ns
Port 2 Address to Valid Instruction In		t_{AVIV2}		139		$3.5t_{CLCL}$-56	ns
$\overline{PSEN}$ Low to Address Float		t_{PLAZ}		(Note 5)		(Note 5)	ns

NOTES FOR DS80C323 AC ELECTRICAL CHARACTERISTICS

All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested. AC electrical characteristics assume 50% duty cycle for the oscillator, oscillator frequency > 16MHz, and are not 100% production tested, but are guaranteed by design.

1. All signals rated over operating temperature at 18MHz.
2. All signals characterized with load capacitance of 80pF except Port 0, ALE, $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}$ at 100pF. Note that loading should be approximately equal for valid timing.
3. Interfacing to memory devices with float times (turn off times) over 35ns may cause contention. This will not damage the parts, but will cause an increase in operating current.
4. Specifications assume a 50% duty cycle for the oscillator. Port 2 timing will change with the duty cycle variations.
5. Address is held in a weak latch until over-driven by external memory.

MOVX CHARACTERISTICS—DS80C323

PARAMETER	SYMBOL	VARIABLE CLOCK		UNITS	STRETCH
		MIN	MAX		
$\overline{RD}$ Pulse Width	t_{RLRH}	$2t_{CLCL}$-11		ns	t_{MCS}=0
		t_{MCS}-11			t_{MCS}>0
$\overline{WR}$ Pulse Width	t_{WLWH}	$2t_{CLCL}$-11		ns	t_{MCS}=0
		t_{MCS}-11			t_{MCS}>0
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2t_{CLCL}$-32	ns	t_{MCS}=0
			t_{MCS}-36		t_{MCS}>0
Data Hold After Read	t_{RHDX}	0		ns	
Data Float After Read	t_{RHDZ}		t_{CLCL}-5	ns	t_{MCS}=0
			$2t_{CLCL}$-7		t_{MCS}>0
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL}$-43	ns	t_{MCS}=0
			$1.5t_{CLCL}$-45+t_{MCS}		t_{MCS}>0
Port 0 Address to Valid Data In	t_{AVDV1}		$3t_{CLCL}$-40	ns	t_{MCS}=0
			$2t_{CLCL}$-42+t_{MCS}		t_{MCS}>0
Port 2 Address to Valid Data In	t_{AVDV2}		$3.5t_{CLCL}$-58	ns	t_{MCS}=0
			$2.5t_{CLCL}$-59+t_{MCS}		t_{MCS}>0
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL}$-18	$0.5t_{CLCL}$+7	ns	t_{MCS}=0
		$1.5t_{CLCL}$-11	$1.5t_{CLCL}$+8		t_{MCS}>0
Port 0 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	t_{CLCL}-10		ns	t_{MCS}=0
		$2t_{CLCL}$-10			t_{MCS}>0
Port 2 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL}$-27		ns	t_{MCS}=0
		$2.5t_{CLCL}$-25			t_{MCS}>0
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-14		ns	t_{MCS}=0
		t_{CLCL}-13			t_{MCS}>0
Data Hold After Write	t_{WHQX}	t_{CLCL}-15		ns	t_{MCS}=0
		$2t_{CLCL}$-13			t_{MCS}>0
$\overline{RD}$ Low to Address Float	t_{RLAZ}		(Note 5)	ns	
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{WHLH}	-1	14	ns	t_{MCS}=0
		t_{CLCL}-5	t_{CLCL}+16		t_{MCS}>0

Note: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.

M2	M1	M0	MOVX CYCLES	t_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles (default)	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Clock High Time	t_{CHCX}	10			ns
Clock Low Time	t_{CLCX}	10			ns
Clock Rise Time	t_{CLCH}			5	ns
Clock Fall Time	t_{CHCL}			5	ns

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Port Clock Cycle Time	t_{XLXL}	SM2 = 0; 12 clocks per cycle		$12t_{CLCL}$		ns
		SM2 = 1; 4 clocks per cycle		$4t_{CLCL}$		
Output Data Setup to Clock Rising Edge	t_{QVXH}	SM2 = 0 12 clocks per cycle		$10t_{CLCL}$		ns
		SM2 = 1; 4 clocks per cycle		$3t_{CLCL}$		
Output Data Hold from Clock Rising	t_{XHQX}	SM2 = 0 12 clocks per cycle		$2t_{CLCL}$		ns
		SM2 = 1; 4 clocks per cycle		t_{CLCL}		
Input Data Hold After Clock Rising	t_{XHDX}	SM2 = 0; 12 clocks per cycle		t_{CLCL}		ns
		SM2 = 1; 4 clocks per cycle		t_{CLCL}		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0; 12 clocks per cycle		$11t_{CLCL}$		ns
		SM2 = 1 4 clocks per cycle		$2t_{CLCL}$		

EXPLANATION OF AC SYMBOLS

In an effort to remain compatible with the original 8051 family, this device specifies the same parameter as such devices, using the same symbols. For completeness, the following is an explanation of the symbols.

t	Time
A	Address
C	Clock
D	Input data
H	Logic level high
L	Logic level low
I	Instruction
P	$\overline{\text{PSEN}}$
Q	Output data
R	$\overline{\text{RD}}$ signal
V	Valid
W	$\overline{\text{WR}}$ signal
X	No longer a valid logic level
Z	Tri-state

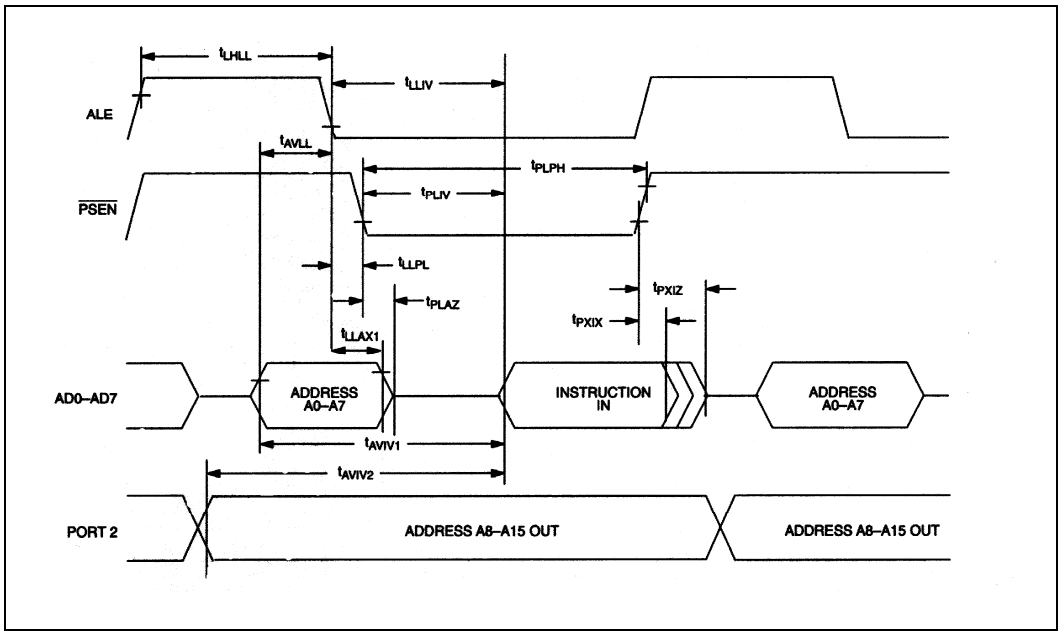
POWER-CYCLE TIMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Crystal Startup Time	t_{CSU}		1.8		ms	1
Power-On Reset Delay	t_{POR}			65,536	t_{CLCL}	2

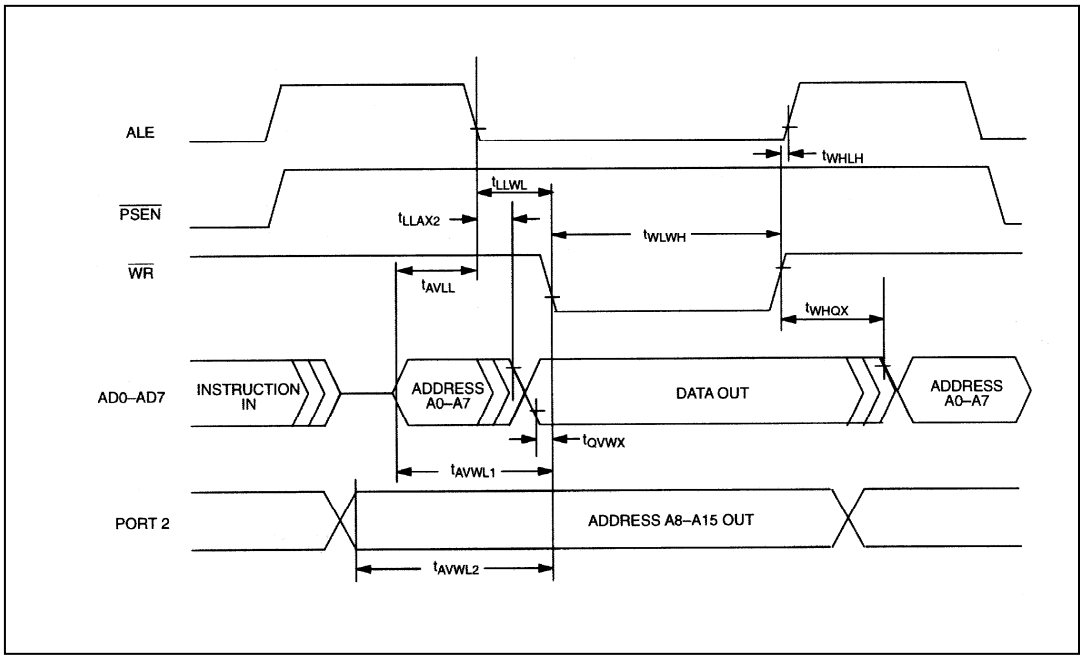
NOTES FOR POWER CYCLE TIMING CHARACTERISTICS

1. Startup time for crystals varies with load capacitance and manufacturer. Time shown is for an 11.0592MHz crystal manufactured by Fox crystal.
2. Reset delay is a synchronous counter of crystal oscillations after crystal startup. Counting begins when the level on the XTAL1 input meets the V_{IH2} criteria. At 25MHz, this time is 2.62ms.

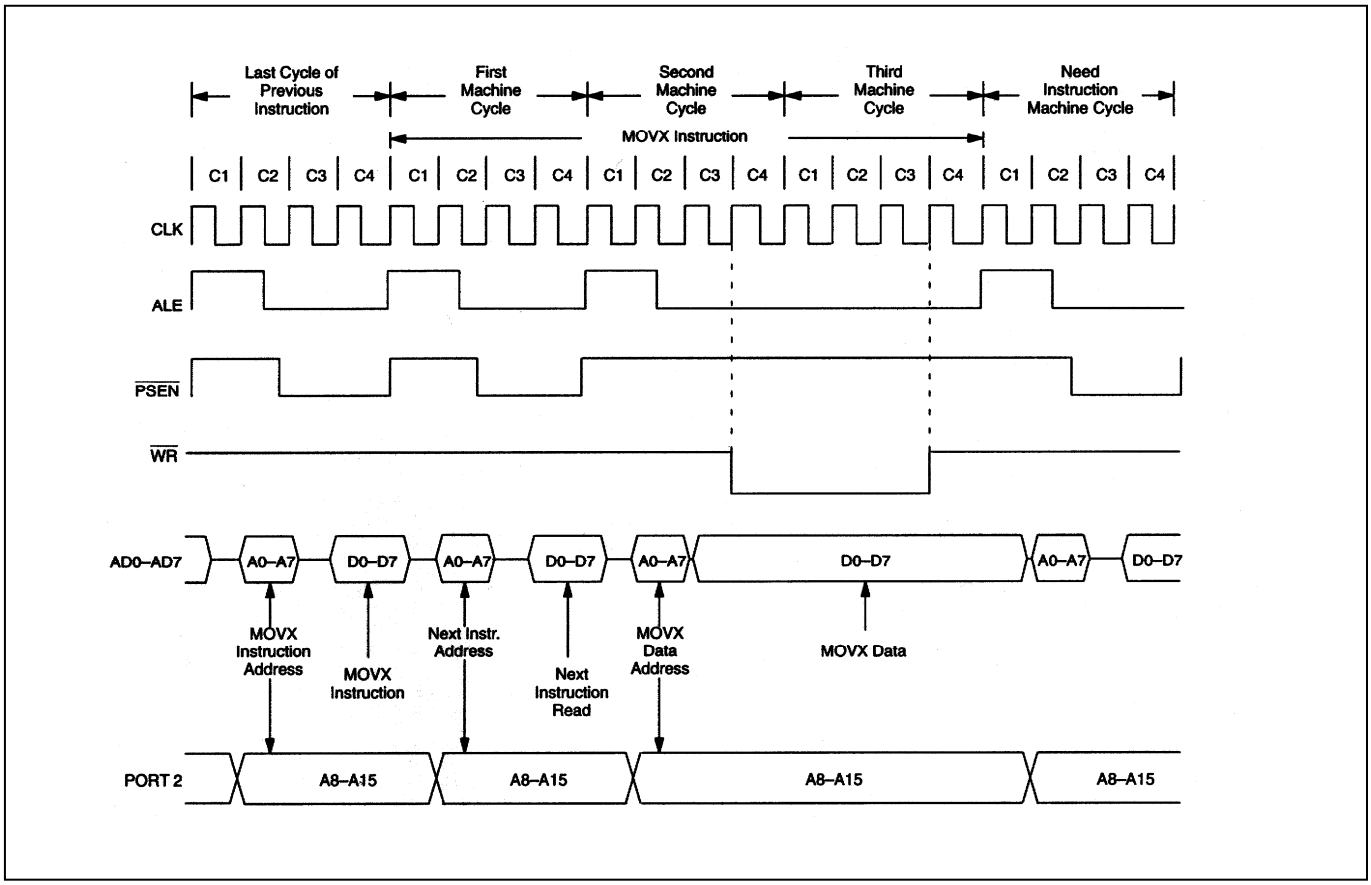
PROGRAM MEMORY READ CYCLE



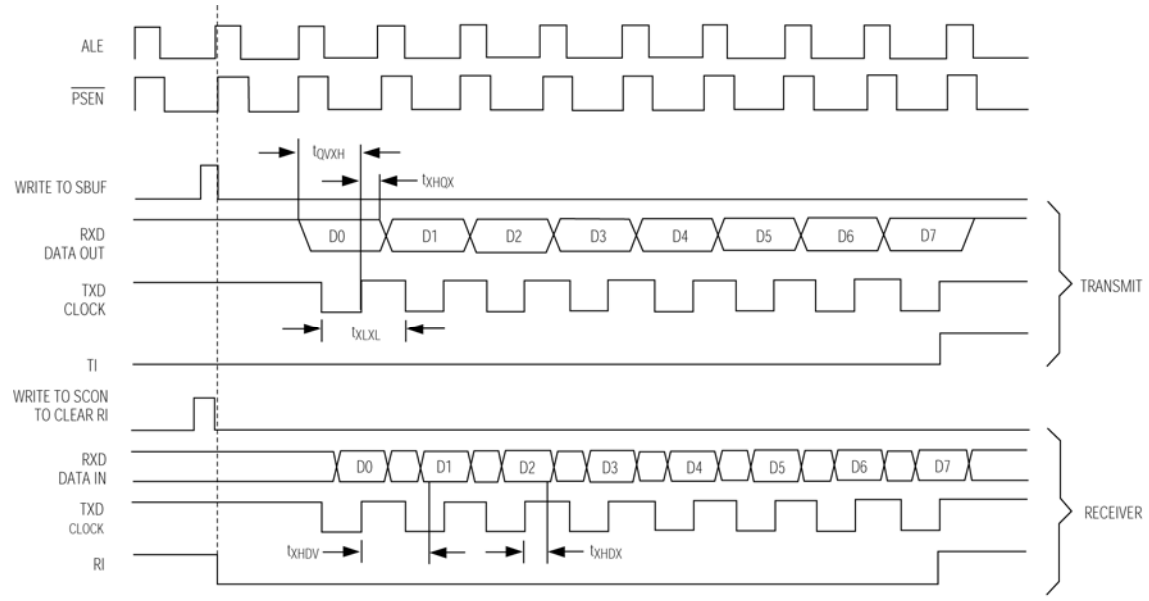
DATA MEMORY WRITE CYCLE



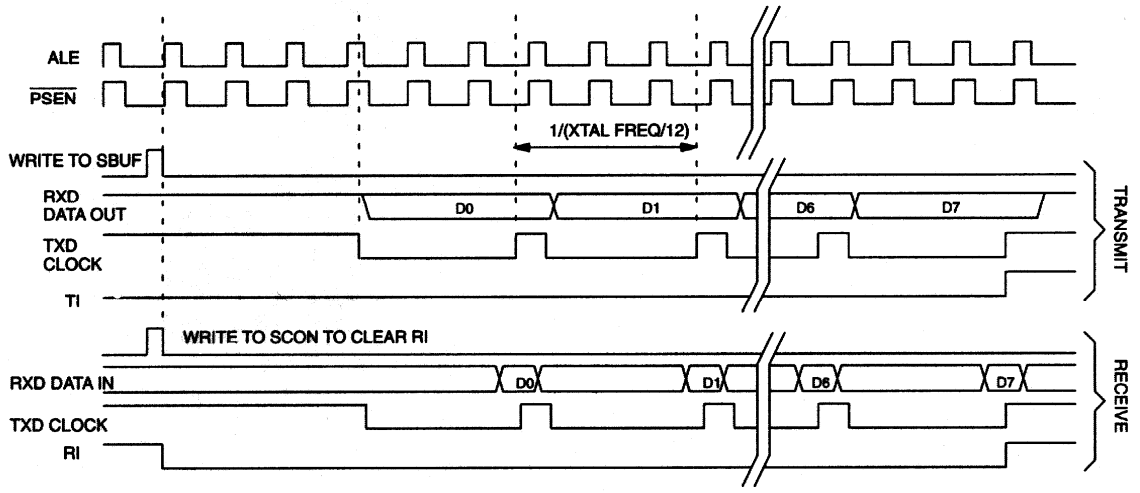
DATA MEMORY WRITE WITH STRETCH = 1



SERIAL PORT MODE 0 TIMING



SERIAL PORT 0 (SYNCHRONOUS MODE)
HIGH SPEED OPERATION SM2 = 1 ≥ TXD CLOCK = XTAL/4



SERIAL PORT 0 (SYNCHRONOUS MODE)
SM2 = 0 ≥ TXD CLOCK = XTAL/12

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
44 TQFP	C44+2	**21-0293**
44 MQFP	M44+10	**21-0269**
44 MQFP	M44+5	**21-0826**
40 PDIP	P40+1	**21-0044**
44 PLCC	Q44+1	**21-0049**

DATA SHEET REVISION SUMMARY

The following represent the key differences between the 101006 and 070505 version of the DS80C320/DS80C323 data sheet. Please review this summary carefully.

1. Deleted DS80C323-MND from Ordering Information table (page 2). Device was never manufactured.

The following represent the key differences between the 070505 and 051804 version of the DS80C320/DS80C323 data sheet. Please review this summary carefully.

2. Added Pb-free/RoHS-compliant part numbers to Ordering Information table.
3. Deleted the "A" from the IPC/JEDEC J-STD-020 specification in the Absolute Maximum Ratings.

The following represent the key differences between the 051804 and the 112299 version of the DS80C320/DS80C323 data sheet. Please review this summary carefully.

1. Removed "Preliminary" status as a result of final characterization.
2. Added industrial temperature DS80C323 devices to ordering information.
3. Updated soldering temperature specification to reflect JEDEC standards.
4. Updated the following DS80C323 AC timing parameters with final characterization data: t_{LHLL}, t_{LLAX1}, t_{LLAX2}, t_{LLAX2}, t_{LLIV}, t_{LLPL}, t_{PLIV}, t_{AVIV1}, t_{RLDV}, t_{RHDZ}, t_{LLDV}, t_{AVDV1}, t_{AVDV2}, t_{LLWL}, t_{AVWL1}, t_{AVWL2}, t_{QVWX}, t_{WHQX}, t_{WHLH}.
5. Updated the following DS80C320 AC timing parameters with final characterization data: t_{WHQX}, t_{LHLL}, t_{LLAX2}, tLLDV, t_{AVDV1}, t_{LLWL}, t_{AVWL1}, t_{AVWL2}.
6. Added note advising the need to reset watchdog timer before setting the Stop bit.
7. Added note clarifying drive strength of P0, P2, ALE, $\overline{PSEN}$.
8. Obsoleted DS80C320 25MHz AC timing tables; merged into 33MHz AC timing tables.
9. Corrected Serial Port Mode 0 Timing diagrams to show correct order of D6, D7.

The following represent the key differences between the 041896 and the 052799 version of the DS80C320 data sheet. Please review this summary carefully.

1. Corrected V_{CC} pin description to show DS80C323 operation at +3V.
2. Corrected Timed Access description to show three-cycle window.
3. Modified absolute Maximum Ratings for any pin relative to around, V_{CC} relative to ground.
4. Changed minimum oscillator frequency to 1MHz when using external crystal.
5. Clarified that t_{POR} begins when XTAL1 reaches V_{IH2}.

The following represent the key differences between the 103196 and the 041896 version of the DS80C320 data sheet. Please review this summary carefully.

1. Updated DS80C320 25MHz AC Characteristics.

The following represent the key differences between the 041895 and the 031096 version of the DS80C320 data sheet. Please review this summary carefully.

1. Remove Port 0, Port 2 from V_{OH1} specification (PCN B60802).
2. V_{OH1} test specification clarified (RST = V_{CC}).
3. Add t_{AVWL2} marking to External Memory Read Cycle figure.
4. Correct TQFP drawing to read 44-pin TQFP.
5. Rotate page 1 TQFP illustration to match assembly specifications.

The following represent the key differences between the 031096 and the 052296 version of the DS80C320 data sheet. Please review this summary carefully.

1. Added *Data Sheet Revision Summary* section.

The following represent the key differences between 05/23/96 and 05/22/96 version of the DS80C320 data sheet and between 05/23/96 and 03/27/95 version of the DS80C323 data sheet. Please review this summary carefully.

DS80C320:

1. Add DS80C323 Characteristics.
2. Change DS80C320 V_{PFW} specification from 4.5V to 4.55V (PCN E62802).
3. Update DS80C320 33MHz AC Characteristics.

DS80C323:

1. Delete Data Sheet. Contents moved to DS80C320/DS80C323.