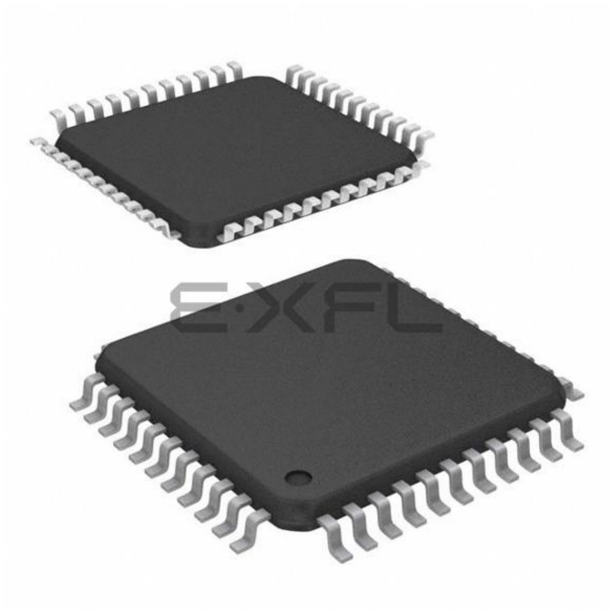


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

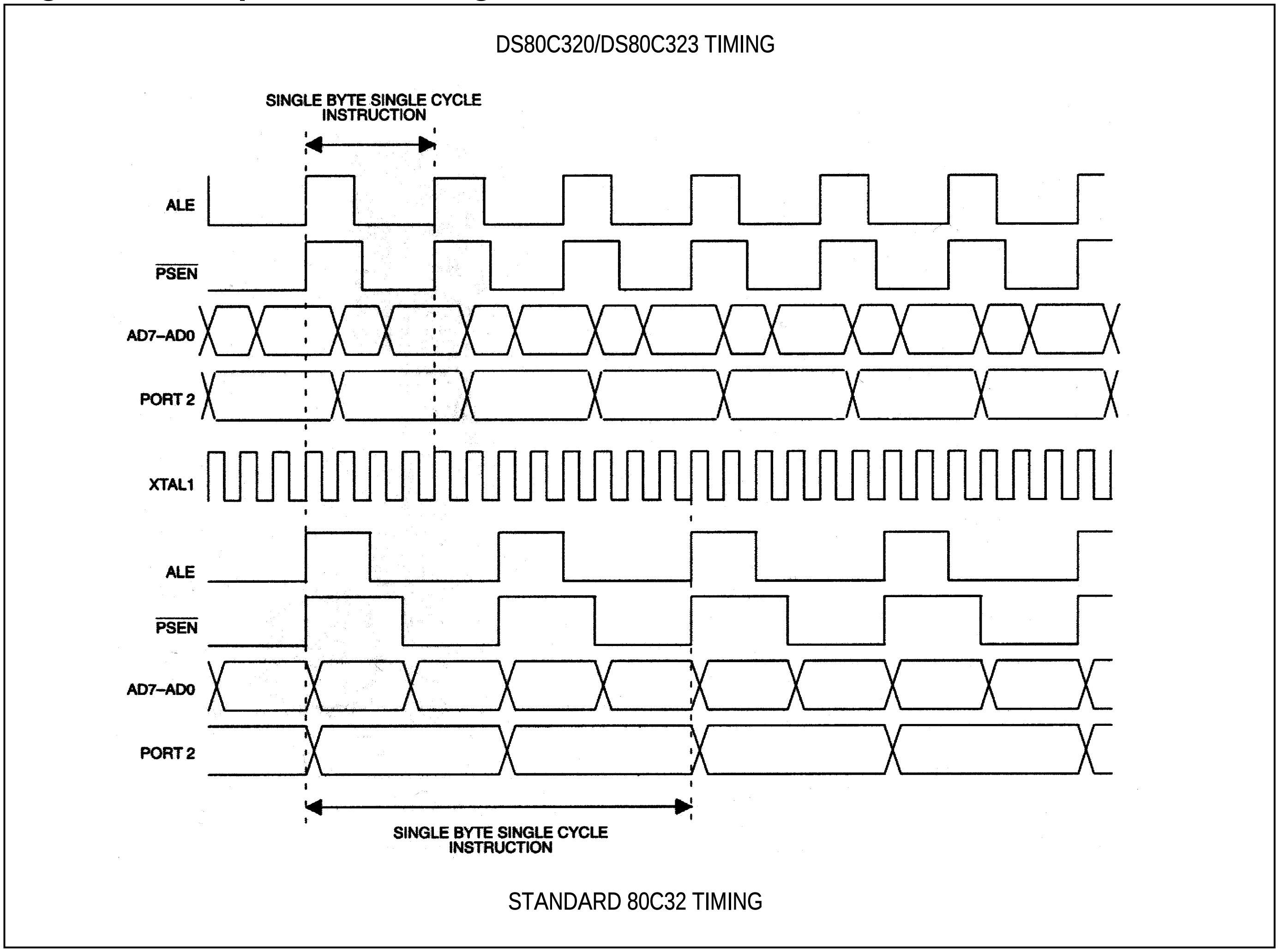
Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds80c320-enl

PIN DESCRIPTION (continued)

PIN			NAME	FUNCTION
DIP	PLCC	TQFP		
30	33	27	ALE	**Address Latch-Enable Output.** This pin functions as a clock to latch the external address LSB from the multiplexed address/data bus. This signal is commonly connected to the latch enable of an external 373 family transparent latch. ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. ALE is forced high when the device is in a reset condition.
39	43	37	AD0	**Port 0, Input/Output.** Port 0 is the multiplexed address/data bus. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls, the port transitions to a bidirectional data bus. This bus is used to read external ROM and read/write external RAM memory or peripherals. The Port 0 has no true port latch and cannot be written directly by software. The reset condition of Port 0 is high. No pullup resistors are needed.
38	42	36	AD1	
37	41	35	AD2	
36	40	34	AD3	
35	39	33	AD4	
34	38	32	AD5	
33	37	31	AD6	
32	36	30	AD7	
1–8	2–9	40–44, 1–3	P1.0–P1.7	**Port 1, I/O**. Port 1 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for Timer 2 I/O, new External Interrupts, and new Serial Port 1. The reset condition of Port 1 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the device will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port once again becomes the output high (and input) state. The alternate modes of Port 1 are outlined as follows:

PIN			PORT	ALTERNATE	FUNCTION
DIP	PLCC	TQFP			
1	2	40	P1.0	T2	External I/O for Timer/Counter 2
2	3	41	P1.1	T2EX	Timer/Counter 2 Capture/Reload Trigger
3	4	42	P1.2	RXD1	Serial Port 1 Input
4	5	43	P1.3	TXD1	Serial Port 1 Output
5	6	44	P1.4	INT2	External Interrupt 2 (Positive-Edge Detect)
6	7	1	P1.5	$\overline{\text{INT3}}$	External Interrupt 3 (Negative-Edge Detect)
7	8	2	P1.6	INT4	External Interrupt 4 (Positive-Edge Detect)
8	9	3	P1.7	$\overline{\text{INT5}}$	External Interrupt 5 (Negative-Edge Detect)

Figure 2. Comparative Timing of the DS80C320/DS80C323 and 80C32



HIGH-SPEED OPERATION

The DS80C320/DS80C323 are built around a high-speed, 80C32-compatible core. Higher speed comes not just from increasing the clock frequency but also from a newer, more efficient design.

In this updated core, dummy memory cycles have been eliminated. In a conventional 80C32, machine cycles are generated by dividing the clock frequency by 12. In the DS80C320/DS80C323, the same machine cycle is performed in 4 clocks. Thus the fastest instruction, one machine cycle, is executed three times faster for the same crystal frequency. Note that these are identical instructions. Figure 2 shows a comparison of the timing differences. The majority of instructions will see the full 3-to-1 speed improvement. Some instructions will get between 1.5X and 2.4X improvement. Note that all instructions are faster than the original 80C51. Table 1 shows a summary of the instruction set, including the speed.

The numerical average of all op codes is approximately a 2.5-to-1 speed improvement. Individual programs are affected differently, depending on the actual instructions used. Speed-sensitive applications would make the most use of instructions that are three times faster. However, the sheer number of 3-to-1 improved op codes makes dramatic speed improvements likely for any code. The Dual Data Pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory.

INSTRUCTION SET SUMMARY

All instructions in the DS80C320/DS80C323 perform the same functions as their 80C32 counterparts. Their effect on bits, flags, and other status functions is identical. However, the timing of each instruction is different. This applies both in absolute and relative number of clocks.

For absolute timing of real-time events, the timing of software loops will need to be calculated using the Table 1. However, counter/timers default to run at the older 12 clocks per increment. Therefore, while software runs at higher speed, timer-based events need no modification to operate as before. Timers can be set to run at 4 clocks per increment cycle to take advantage of higher speed operation.

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture, the “MOVX A, @DPTR” instruction and the “MOV direct, direct” instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS80C320/DS80C323, the MOVX instruction can be done in two machine cycles or eight oscillator cycles, but the “MOV direct, direct” uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times from each other. This is because in most cases, the DS80C320/DS80C323 use one cycle for each byte. The user concerned with precise program timing should examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just four clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV.

Table 1. Instruction Set Summary (continued)

INSTRUCTION	BYTE	OSCILLATOR CYCLES	INSTRUCTION	BYTE	OSCILLATOR CYCLES
DATA TRANSFER INSTRUCTIONS					
MOV A, Rn	1	4	MOVC A, @A+DPTR	1	12
MOV A, direct	2	8	MOVC A, @A+PC	1	12
MOV A, @Ri	1	4	MOVX A, @Ri	1	8–36*
MOV A, #data	2	8	MOVX A, @DPTR	1	8–36*
MOV Rn, A	1	4	MOVX @Ri, A	1	8–36*
MOV Rn, direct	2	8	MOVX @DPTR, A	1	8–36*
MOV Rn, #data	2	8	PUSH direct	2	8
MOV direct, A	2	8	POP direct	2	8
MOV direct, Rn	2	8	XCH A, Rn	1	4
MOV direct1, direct2	3	12	XCH A, direct	2	8
MOV direct, @Ri	2	8	XCH A, @Ri	1	4
MOV direct, #data	3	12	XCHD A, @Ri	1	4
MOV @Ri, A	1	4			
MOV @Ri, direct	2	8			
MOV @Ri, #data	2	8			
MOV DPTR, #data 16	3	12			
BIT MANIPULATION INSTRUCTIONS					
CLR C	1	4	ANL C, bit	2	8
CLR bit	2	8	ANL C, $\overline{\text{bit}}$	2	8
SETB C	1	4	ORL C, bit	2	8
SETB bit	2	8	ORL C, $\overline{\text{bit}}$	2	8
CPL C	1	4	MOV C, bit	2	8
CPL bit	2	8	MOV bit, C	2	8
PROGRAM BRANCHING INSTRUCTIONS					
ACALL addr 11	2	12	CJNE A, direct, rel	3	16
LCALL addr 16	3	16	CJNE A, #data, rel	3	16
RET	1	16	CJNE Rn, #data, rel	3	16
RETI	1	16	CJNE Ri, #data, rel	3	16
AJMP addr 11	2	12	NOP	1	4
LJMP addr 16	3	16	JC rel	2	12
SJMP rel	2	12	JNC rel	2	12
JMP @A+DPTR	1	12	JB bit, rel	3	16
JZ rel	2	12	JNB bit, rel	3	16
JNZ rel	2	12	JBC bit, rel	3	16
DJNZ Rn, rel	2	12			
DJNZ direct, rel	3	16			

**User selectable.*

STRETCH MEMORY CYCLE

The DS80C320/DS80C323 allow the application software to adjust the speed of data memory access. The microcontroller is capable of performing the MOVX in as little as two instruction cycles. However, this value can be stretched as needed so that both fast memory and slow memory or peripherals can be accessed with no glue logic. Even in high-speed systems, it may not be necessary or desirable to perform data memory access at full speed. In addition, there are a variety of memory-mapped peripherals such as LCD displays or UARTs that are not fast.

The Stretch MOVX is controlled by the Clock Control Register at SFR location 8Eh as described below. This allows the user to select a stretch value between 0 and 7. A Stretch of 0 will result in a two-machine cycle MOVX. A Stretch of 7 will result in a MOVX of nine machine cycles. Software can dynamically change this value depending on the particular memory or peripheral.

On reset, the Stretch value will default to 1, resulting in a three-cycle MOVX. Therefore, RAM access will not be performed at full speed. This is a convenience to existing designs that may not have fast RAM in place. When maximum speed is desired, the software should select a Stretch value of 0. When using very slow RAM or peripherals, a larger stretch value can be selected. Note that this affects data memory only and the only way to slow program memory (ROM) access is to use a slower crystal.

Using a Stretch value between 1 and 7 causes the microcontroller to stretch the read/write strobe and all related timing. This results in a wider read/write strobe allowing more time for memory/peripherals to respond. The timing of the variable speed MOVX is shown in the *Electrical Specifications* section. Note that full speed access is not the reset default case. Table 2 shows the resulting strobe widths for each Stretch value. The memory stretch is implemented using the Clock Control special-function register at SFR location 8Eh. The stretch value is selected using bits CKCON.2–0. In the table, these bits are referred to as M2 through M0. The first stretch (default) allows the use of common 120ns or 150ns RAMs without dramatically lengthening the memory access.

Table 2. Data Memory Cycle Stretch Values

CKCON.2–0			MEMORY CYCLES	$\overline{RD}$ or $\overline{WR}$ STROBE WIDTH IN CLOCKS	STROBE WIDTH TIME AT 25MHz (ns)
MD2	MD1	MD0			
0	0	0	2	2	80
0	0	1	3 (default)	4	160
0	1	0	4	8	320
0	1	1	5	12	480
1	0	0	6	16	640
1	0	1	7	20	800
1	1	0	8	24	960
1	1	1	9	28	1120

POWER-FAIL RESET

The DS80C320/DS80C323 incorporate a precision bandgap voltage reference to determine when V_{CC} is out of tolerance. While powering up, internal circuits will hold the device in a reset state until V_{CC} rises above the V_{RST} reset threshold. Once V_{CC} is above this level, the oscillator will begin running. An internal reset circuit will then count 65,536 clocks to allow time for power and the oscillator to stabilize. The microcontroller will then exit the reset condition. No external components are needed to generate a power on reset. During power-down or during a severe power glitch, as V_{CC} falls below V_{RST}, the microcontroller will also generate its own reset. It will hold the reset condition as long as power remains below the threshold. This reset will occur automatically, needing no action from the user or from the software. See the *Electrical Specifications* section for the exact value of V_{RST}.

POWER-FAIL INTERRUPT

The same reference that generates a precision reset threshold can also generate an optional early warning Power-fail Interrupt (PFI). When enabled by the application software, this interrupt always has the highest priority. On detecting that the V_{CC} has dropped below V_{PFW} and that the PFI is enabled, the processor will vector to ROM address 0033h. The PFI enable is located in the Watchdog Control SFR (WDCON to D8h). Setting WDCON.5 to logic 1 will enable the PFI. The application software can also read a flag at WDCON.4. This bit is set when a PFI condition has occurred. The flag is independent of the interrupt enable and software must manually clear it.

WATCHDOG TIMER

For applications that cannot afford to run out of control, the DS80C320/DS80C323 incorporate a programmable watchdog timer circuit. The watchdog timer circuit resets the microcontroller if software fails to reset the watchdog before the selected time interval has elapsed. The user selects one of four timeout values. After enabling the watchdog, software must reset the timer prior to expiration of the interval, or the CPU will be reset. Both the Watchdog Enable and the Watchdog Reset bits are protected by a “Timed Access” circuit. This prevents accidentally clearing the watchdog. Timeout values are precise since they are related to the crystal frequency as shown in Table 3. For reference, the time periods at 25MHz are also shown.

The watchdog timer also provides a useful option for systems that may not require a reset. If enabled, then 512 clocks before giving a reset, the watchdog will give an interrupt. The interrupt can also serve as a convenient time-base generator, or be used to wake-up the processor from Idle mode. The watchdog function is controlled in the Clock Control (CKCON to 8Eh), Watchdog Control (WDCON to D8h), and Extended Interrupt Enable (EIE to E8h) SFRs. CKCON.7 and CKCON.6 are called WD1 and WD0, respectively, and are used to select the watchdog timeout period as shown in Table 3.

Table 3. Watchdog Timeout Values

WD1	WD0	INTERRUPT TIMEOUT	TIME (at 25MHz)	RESET TIMEOUT	TIME (at 25MHz)
0	0	2^{17} clocks	5.243ms	2^{17} + 512 clocks	5.263ms
0	1	2^{20} clocks	41.94ms	2^{20} + 512 clocks	41.96ms
1	0	2^{23} clocks	335.54ms	2^{23} + 512 clocks	335.56ms
1	1	2^{26} clocks	2684.35ms	2^{26} + 512 clocks	2684.38ms

As Table 3 shows, the watchdog timer uses the crystal frequency as a time base. A user selects one of four counter values to determine the timeout. These clock counter lengths are 2^{17} = 131,072 clocks; 2^{20} = 1,048,576; 2^{23} = 8,388,608 clocks; or 2^{26} = 67,108,864 clocks. The times shown in Table 4 are with a 25MHz crystal frequency. Note that once the counter chain has reached a conclusion, the optional interrupt is generated. Regardless of whether the user enables this interrupt, there are then 512 clocks left until a reset occurs. There are 5 control bits in special function registers that affect the Watchdog Timer and two status flags that report to the user. The Reset Watchdog Timer bit (WDCON.0) should be asserted prior to modifying the Watchdog Timer Mode Select bits (WD1, WD0) to avoid corruption of the watchdog count.

WDIF (WDCON.3) is the interrupt flag that is set when there are 512 clocks remaining until a reset occurs. WTRF (WDCON.2) is the flag that is set when a Watchdog reset has occurred. This allows the application software to determine the source of a reset.

Setting the EWT (WDCON.1) bit enables the Watchdog Timer. The bit is protected by timed access. Setting the RWT (WDCON.0) bit restarts the Watchdog Timer for another full interval. Application software must set this bit prior to the timeout. As mentioned previously, WD1 and 0 (CKCON .7 and 6) select the timeout. Finally, the Watchdog Interrupt is enabled using EWDI (EIE.4).

INTERRUPTS

The DS80C320/DS80C323 provide 13 sources of interrupt with three priority levels. The Power-fail Interrupt (PFI), if enabled, always has the highest priority. There are two remaining user-selectable priorities: high and low. If two interrupts that have the same priority occur simultaneously, the natural precedence given in Table 4 determines which is acted upon. Except for the PFI, all interrupts that are new to the 8051 family have a lower natural priority than the originals.

Table 4. Interrupt Priority

NAME	FUNCTION	VECTOR	NATURAL PRIORITY	OLD/NEW
PFI	Power-Fail Interrupt	33h	1	New
$\overline{\text{INT0}}$	External Interrupt 0	03h	2	Old
TF0	Timer 0	0Bh	3	Old
$\overline{\text{INT1}}$	External Interrupt 1	13h	4	Old
TF1	Timer 1	1Bh	5	Old
SCON0	TI0 or RI0 from Serial Port 0	23h	6	Old
TF2	Timer 2	2Bh	7	Old
SCON1	TI1 or RI1 from Serial Port 1	3Bh	8	New
INT2	External Interrupt 2	43h	9	New
$\overline{\text{INT3}}$	External Interrupt 3	4Bh	10	New
INT4	External Interrupt 4	53h	11	New
$\overline{\text{INT5}}$	External Interrupt 5	5Bh	12	New
WDTI	Watchdog Timeout Interrupt	63h	13	New

Figure 4. Ring Oscillator Startup

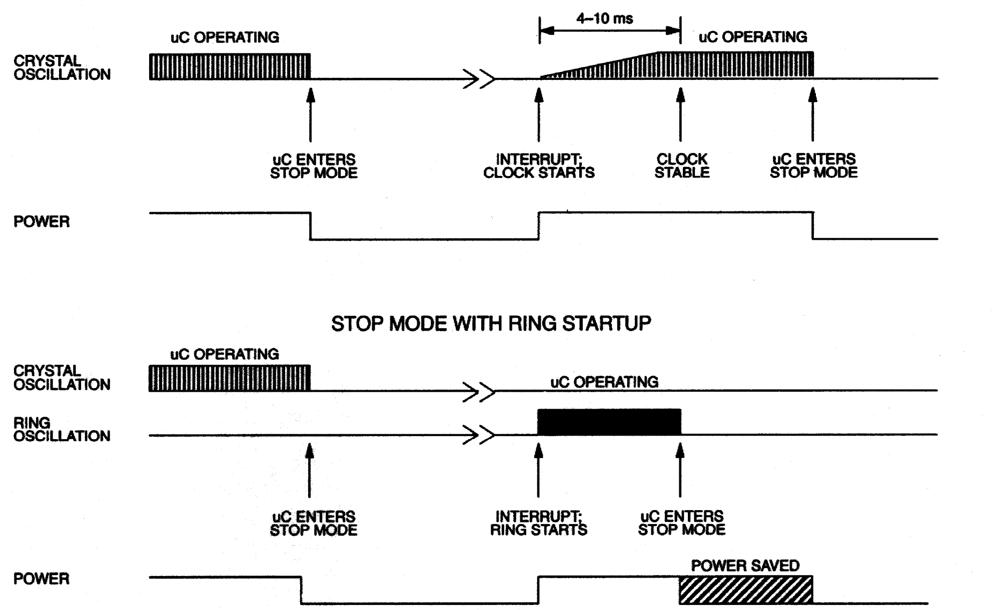


DIAGRAM ASSUMES THAT THE OPERATION FOLLOWING STOP REQUIRES LESS THAN 18ms COMPLETE.

TIMED ACCESS PROTECTION

Selected SFR bits are critical to operation, making it desirable to protect against an accidental write operation. The Timed Access procedure prevents an errant CPU from accidentally altering a bit that would cause difficulty. The Timed Access procedure requires that the write of a protected bit be preceded by the following instructions:

```
MOV     0C7h, #0AAh
MOV     0C7h, #55h
```

By writing an AAh followed by a 55h to the Timed Access register (location C7h), the hardware opens a three-cycle window that allows software to modify one of the protected bits. If the instruction that seeks to modify the protected bit is not immediately proceeded by these instructions, the write will not take effect. The protected bits are:

EXIF.0	BGS Bandgap Select
WDCON.6	POR Power-on Reset flag
WDCON.1	EWT Enable Watchdog
WDCON.0	RWT Reset Watchdog
WDCON.3	WDIF Watchdog Interrupt Flag

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……………………………………….-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground……………………………………………….-0.3V to +6.0V
Operating Temperature Range……………………………………………………………….-40°C to +85°C
Storage Temperature Range…………………………………………………………….-55°C to +125°C
Soldering Temperature…………………………………………See IPC/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS—DS80C320

(V_{CC} = 4.5V to 5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Power-Fail Warning Voltage	V_{PFW}	4.25	4.38	4.55	V	1
Minimum Operating Voltage	V_{RST}	4.0	4.1	4.25	V	1, 12
Supply Current Active Mode at 25MHz	I_{CC}		30	45	mA	2
Supply Current Idle Mode at 25MHz	I_{IDLE}		15	25	mA	3
Supply Current Active Mode at 33MHz	I_{CC}		35		mA	2
Supply Current Idle Mode at 33MHz	I_{IDLE}		20		mA	3
Supply Current Stop Mode, Bandgap Reference Disabled	I_{STOP}		0.01	1	µA	4
Supply Current Stop Mode, Bandgap Reference Enabled	I_{SPBG}		50	80	µA	4, 10
Input Low Level	V_{IL}	-0.3		+0.8	V	1
Input High Level (Except XTAL1 and RST)	V_{IH1}	2.0		V_{CC} + 0.3	V	1
Input High Level XTAL1 and RST	V_{IH2}	3.5		V_{CC} + 0.3	V	1
Output-Low Voltage Ports 1, 3 at I_{OL} = 1.6mA	V_{OL1}			0.45	V	1
Output-Low Voltage Ports 0, 2, ALE, $\overline{\text{PSEN}}$ at I_{OL} = 3.2mA	V_{OL2}			0.45	V	1, 5
Output-High Voltage Ports 1, 3, ALE, $\overline{\text{PSEN}}$ at I_{OH} = -50µA	V_{OH1}	2.4			V	1, 6
Output High Voltage Ports 1, 3 at I_{OH} = -1.5mA	V_{OH2}	2.4			V	1, 7
Output-High Voltage Ports 0, 2, ALE, $\overline{\text{PSEN}}$ at I_{OH} = -8mA	V_{OH3}	2.4			V	1, 5
Input Low Current Ports 1, 3 at 0.45V	I_{IL}			-55	µA	11
Transition Current from 1 to 0 Ports 1, 3 at 2V	I_{TL}			-650	µA	8
Input Leakage Port 0, Bus Mode	I_L	-300		+300	µA	9
RST Pulldown Resistance	R_{RST}	50		170	kΩ	

AC CHARACTERISTICS—DS80C320

PARAMETER		SYMBOL	33MHz		VARIABLE CLOCK		UNITS
			MIN	MAX	MIN	MAX	
Oscillator Frequency	External Oscillator	$1/t_{CLCL}$	0	33	0	33	MHz
	External Crystal		1	33	1	33	
ALE Pulse Width		t_{LHLL}	34		$1.5t_{CLCL}$-11		ns
Port 0 Address Valid to ALE Low		t_{AVLL}	4		$0.5t_{CLCL}$-11		ns
Address Hold After ALE Low		t_{LLAX1}	2	(Note 5)	$0.25t_{CLCL}$-5	(Note 5)	ns
Address Hold After ALE Low for MOVX $\overline{WR}$		t_{LLAX2}	6		$0.5t_{CLCL}$-9		ns
ALE Low to Valid Instruction In		t_{LLIV}		49		$2.5t_{CLCL}$-27	ns
ALE Low to $\overline{PSEN}$ Low		t_{LLPL}	0.5		$0.25t_{CLCL}$-7		ns
$\overline{PSEN}$ Pulse Width		t_{PLPH}	61		$2.25t_{CLCL}$-7		ns
$\overline{PSEN}$ Low to Valid Instruction In		t_{PLIV}		48		$2.25t_{CLCL}$-21	ns
Input Instruction Hold After $\overline{PSEN}$		t_{PXIX}	0		0		ns
Input Instruction Float After $\overline{PSEN}$		t_{PXIZ}		25		t_{CLCL}-5	ns
Port 0 Address to Valid Instruction In		t_{AVIV1}		64		$3t_{CLCL}$-27	ns
Port 2 Address to Valid Instruction In		t_{AVIV2}		73		$3.5t_{CLCL}$-33	ns
$\overline{PSEN}$ Low to Address Float		t_{PLAZ}		(Note 5)		(Note 5)	ns

NOTES FOR DS80C320 AC ELECTRICAL CHARACTERISTICS

All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested. AC electrical characteristics assume 50% duty cycle for the oscillator, oscillator frequency > 16MHz, and are not 100% tested, but are guaranteed by design.

1. All signals rated over operating temperature at 33MHz.
2. All signals characterized with load capacitance of 80pF except Port 0, ALE, $\overline{PSEN}$, $\overline{RD}$ and $\overline{WR}$ at 100pF. Note that loading should be approximately equal for valid timing.
3. Interfacing to memory devices with float times (turn off times) over 30ns may cause contention. This will not damage the parts but will cause an increase in operating current.
4. Specifications assume a 50% duty cycle for the oscillator. Port 2 timing will change with the duty cycle variations.
5. Address is held in a weak latch until over driven by external memory.

MOVX CHARACTERISTICS—DS80C320

PARAMETER	SYMBOL	VARIABLE CLOCK MIN	VARIABLE CLOCK MAX	UNITS	STRETCH
$\overline{RD}$ Pulse Width	t_{RLRH}	$2t_{CLCL}$-11		ns	t_{MCS}=0
		t_{MCS}-11			t_{MCS}>0
$\overline{WR}$ Pulse Width	t_{WLWH}	$2t_{CLCL}$-11		ns	t_{MCS}=0
		t_{MCS}-11			t_{MCS}>0
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2t_{CLCL}$-25	ns	t_{MCS}=0
			t_{MCS}-25		t_{MCS}>0
Data Hold After Read	t_{RHDX}	0		ns	
Data Float After Read	t_{RHDZ}		t_{CLCL}-5	ns	t_{MCS}=0
			$2t_{CLCL}$-5		t_{MCS}>0
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL}$-27	ns	t_{MCS}=0
			$1.5t_{CLCL}$-28+t_{MCS}		t_{MCS}>0
Port 0 Address to Valid Data In	t_{AVDV1}		$3t_{CLCL}$-27	ns	t_{MCS}=0
			$2t_{CLCL}$-31+t_{MCS}		t_{MCS}>0
Port 2 Address to Valid Data In	t_{AVDV2}		$3.5t_{CLCL}$-32	ns	t_{MCS}=0
			$2.5t_{CLCL}$-34+t_{MCS}		t_{MCS}>0
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL}$-8	$0.5t_{CLCL}$+6	ns	t_{MCS}=0
		$1.5t_{CLCL}$-7	$1.5t_{CLCL}$+8		t_{MCS}>0
Port 0 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	t_{CLCL}-11		ns	t_{MCS}=0
		$2t_{CLCL}$-10			t_{MCS}>0
Port 2 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL}$-9		ns	t_{MCS}=0
		$2.5t_{CLCL}$-13			t_{MCS}>0
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-9		ns	t_{MCS}=0
		t_{CLCL}-10			t_{MCS}>0
Data Hold After Write	t_{WHQX}	t_{CLCL}-12		ns	t_{MCS}=0
		$2t_{CLCL}$-7			t_{MCS}>0
$\overline{RD}$ Low to Address Float	t_{RLAZ}		(Note 5)	ns	
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{WHLH}	0	10	ns	t_{MCS}=0
		t_{CLCL}-5	t_{CLCL}+11		t_{MCS}>0

Note: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.

M2	M1	M0	MOVX CYCLES	t_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles (default)	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

NOTES FOR DS80C323 DC ELECTRICAL CHARACTERISTICS (continued)

All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested. Device operating range is 2.7V to 5.5V. DC electrical specifications are for operation 2.7V to 3.3V.

6. RST = V_{CC}. This condition mimics operation of pins in I/O mode.
7. During a 0-to-1 transition, a one-shot drives the ports hard for two clock cycles. This measurement reflects port in transition mode.
8. Ports 1, 2, and 3 source transition current when being pulled down externally. It reaches its maximum at approximately 2V.
9. V_{IN} between ground and V_{CC} - 0.3V. Not a high-impedance input. This port is a weak address latch because Port 0 is dedicated as an address bus on the DS80C323. Peak current occurs near the input transition point of the latch, approximately 2V.
10. Over the industrial temperature range, this specification has a maximum value of 200µA.
11. This is the current from an external circuit to hold a logic low level on an I/O pin while the corresponding port latch bit is set to 1. This is only the current required to *hold* the low level; transitions from 1 to 0 on an I/O pin will also have to overcome the transition current.
12. Device operating range is 2.7V to 5.5V, however device is tested to 2.5V to ensure proper operation at minimum V_{RST}.

AC ELECTRICAL CHARACTERISTICS—DS80C323

PARAMETER		SYMBOL	18 MHz		VARIABLE CLOCK		UNITS
			MIN	MAX	MIN	MAX	
Oscillator Frequency	External Oscillator	$1/t_{CLCL}$	0	18	0	18	MHz
	External Crystal		1	18	1	18	
ALE Pulse Width		t_{LHLL}	68		$1.5t_{CLCL}$-15		ns
Port 0 Address Valid to ALE Low		t_{AVLL}	16		$0.5t_{CLCL}$-11		ns
Address Hold After ALE Low		t_{LLAX1}	6	(Note 5)	$0.25t_{CLCL}$-8	(Note 5)	ns
Address Hold After ALE Low for MOVX $\overline{\text{WR}}$		t_{LLAX2}	14		$0.5t_{CLCL}$-13		ns
ALE Low to Valid Instruction In		t_{LLIV}		93		$2.5t_{CLCL}$-46	ns
ALE Low to $\overline{\text{PSEN}}$ Low		t_{LLPL}	4		$0.25t_{CLCL}$-10		ns
$\overline{\text{PSEN}}$ Pulse Width		t_{PLPH}	118		$2.25t_{CLCL}$-7		ns
$\overline{\text{PSEN}}$ Low to Valid Instruction In		t_{PLIV}		87		$2.25t_{CLCL}$-38	ns
Input Instruction Hold After $\overline{\text{PSEN}}$		t_{PXIX}	0		0		ns
Input Instruction Float After $\overline{\text{PSEN}}$		t_{PXIZ}		51		t_{CLCL}-5	ns
Port 0 Address to Valid Instruction In		t_{AVIV1}		128		$3t_{CLCL}$-39	ns
Port 2 Address to Valid Instruction In		t_{AVIV2}		139		$3.5t_{CLCL}$-56	ns
$\overline{\text{PSEN}}$ Low to Address Float		t_{PLAZ}		(Note 5)		(Note 5)	ns

NOTES FOR DS80C323 AC ELECTRICAL CHARACTERISTICS

All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested. AC electrical characteristics assume 50% duty cycle for the oscillator, oscillator frequency > 16MHz, and are not 100% production tested, but are guaranteed by design.

1. All signals rated over operating temperature at 18MHz.
2. All signals characterized with load capacitance of 80pF except Port 0, ALE, $\overline{\text{PSEN}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ at 100pF. Note that loading should be approximately equal for valid timing.
3. Interfacing to memory devices with float times (turn off times) over 35ns may cause contention. This will not damage the parts, but will cause an increase in operating current.
4. Specifications assume a 50% duty cycle for the oscillator. Port 2 timing will change with the duty cycle variations.
5. Address is held in a weak latch until over-driven by external memory.

MOVX CHARACTERISTICS—DS80C323

PARAMETER	SYMBOL	VARIABLE CLOCK MIN	VARIABLE CLOCK MAX	UNITS	STRETCH
$\overline{RD}$ Pulse Width	t_{RLRH}	$2t_{CLCL}$-11		ns	t_{MCS}=0
		t_{MCS}-11			t_{MCS}>0
$\overline{WR}$ Pulse Width	t_{WLWH}	$2t_{CLCL}$-11		ns	t_{MCS}=0
		t_{MCS}-11			t_{MCS}>0
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2t_{CLCL}$-32	ns	t_{MCS}=0
			t_{MCS}-36		t_{MCS}>0
Data Hold After Read	t_{RHDX}	0		ns	
Data Float After Read	t_{RHDZ}		t_{CLCL}-5	ns	t_{MCS}=0
			$2t_{CLCL}$-7		t_{MCS}>0
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL}$-43	ns	t_{MCS}=0
			$1.5t_{CLCL}$-45+t_{MCS}		t_{MCS}>0
Port 0 Address to Valid Data In	t_{AVDV1}		$3t_{CLCL}$-40	ns	t_{MCS}=0
			$2t_{CLCL}$-42+t_{MCS}		t_{MCS}>0
Port 2 Address to Valid Data In	t_{AVDV2}		$3.5t_{CLCL}$-58	ns	t_{MCS}=0
			$2.5t_{CLCL}$-59+t_{MCS}		t_{MCS}>0
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL}$-18	$0.5t_{CLCL}$+7	ns	t_{MCS}=0
		$1.5t_{CLCL}$-11	$1.5t_{CLCL}$+8		t_{MCS}>0
Port 0 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	t_{CLCL}-10		ns	t_{MCS}=0
		$2t_{CLCL}$-10			t_{MCS}>0
Port 2 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL}$-27		ns	t_{MCS}=0
		$2.5t_{CLCL}$-25			t_{MCS}>0
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-14		ns	t_{MCS}=0
		t_{CLCL}-13			t_{MCS}>0
Data Hold After Write	t_{WHQX}	t_{CLCL}-15		ns	t_{MCS}=0
		$2t_{CLCL}$-13			t_{MCS}>0
$\overline{RD}$ Low to Address Float	t_{RLAZ}		(Note 5)	ns	
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{WHLH}	-1	14	ns	t_{MCS}=0
		t_{CLCL}-5	t_{CLCL}+16		t_{MCS}>0

Note: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.

M2	M1	M0	MOVX CYCLES	t_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles (default)	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Clock High Time	t_{CHCX}	10			ns
Clock Low Time	t_{CLCX}	10			ns
Clock Rise Time	t_{CLCH}			5	ns
Clock Fall Time	t_{CHCL}			5	ns

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Port Clock Cycle Time	t_{XLXL}	SM2 = 0; 12 clocks per cycle		$12t_{CLCL}$		ns
		SM2 = 1; 4 clocks per cycle		$4t_{CLCL}$		
Output Data Setup to Clock Rising Edge	t_{QVXH}	SM2 = 0 12 clocks per cycle		$10t_{CLCL}$		ns
		SM2 = 1; 4 clocks per cycle		$3t_{CLCL}$		
Output Data Hold from Clock Rising	t_{XHQX}	SM2 = 0 12 clocks per cycle		$2t_{CLCL}$		ns
		SM2 = 1; 4 clocks per cycle		t_{CLCL}		
Input Data Hold After Clock Rising	t_{XHDX}	SM2 = 0; 12 clocks per cycle		t_{CLCL}		ns
		SM2 = 1; 4 clocks per cycle		t_{CLCL}		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0; 12 clocks per cycle		$11t_{CLCL}$		ns
		SM2 = 1 4 clocks per cycle		$2t_{CLCL}$		

EXPLANATION OF AC SYMBOLS

In an effort to remain compatible with the original 8051 family, this device specifies the same parameter as such devices, using the same symbols. For completeness, the following is an explanation of the symbols.

t	Time
A	Address
C	Clock
D	Input data
H	Logic level high
L	Logic level low
I	Instruction
P	$\overline{\text{PSEN}}$
Q	Output data
R	$\overline{\text{RD}}$ signal
V	Valid
W	$\overline{\text{WR}}$ signal
X	No longer a valid logic level
Z	Tri-state

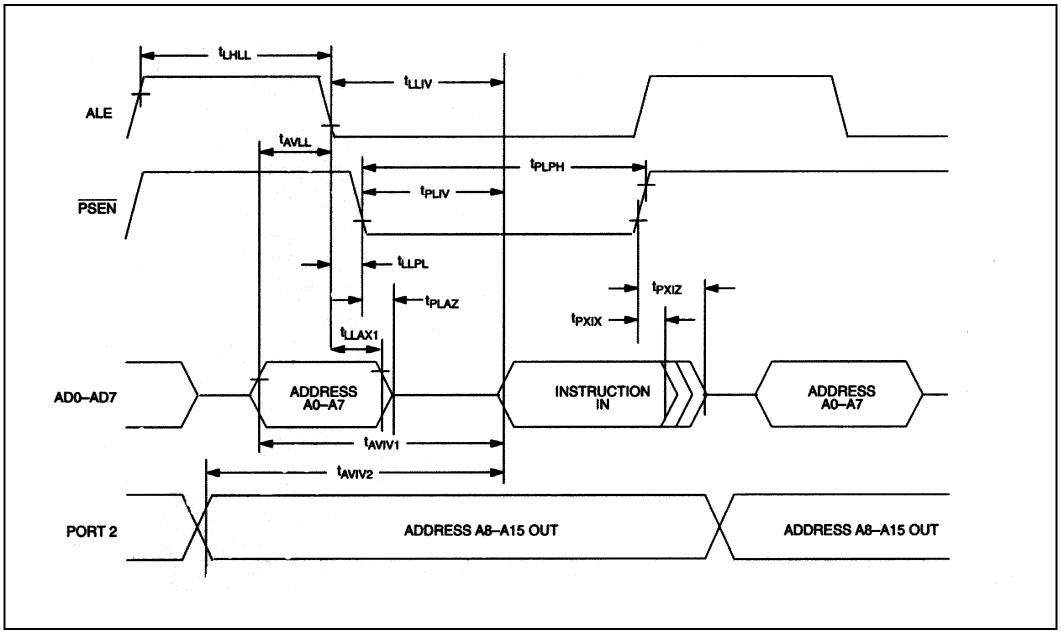
POWER-CYCLE TIMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Crystal Startup Time	t_{CSU}		1.8		ms	1
Power-On Reset Delay	t_{POR}			65,536	t_{CLCL}	2

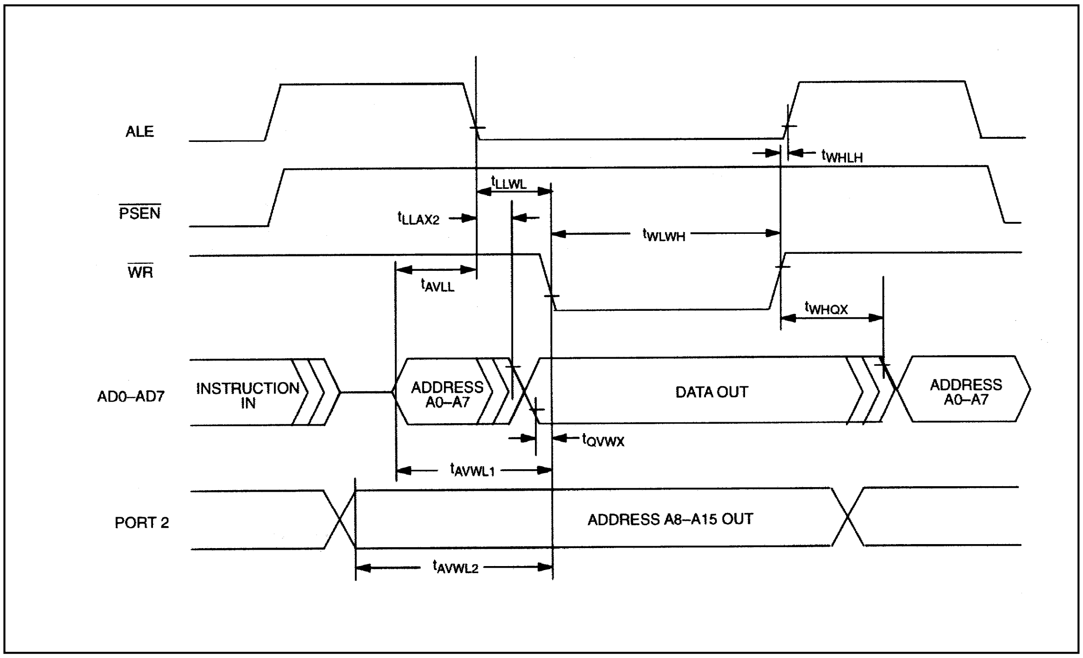
NOTES FOR POWER CYCLE TIMING CHARACTERISTICS

1. Startup time for crystals varies with load capacitance and manufacturer. Time shown is for an 11.0592MHz crystal manufactured by Fox crystal.
2. Reset delay is a synchronous counter of crystal oscillations after crystal startup. Counting begins when the level on the XTAL1 input meets the V_{IH2} criteria. At 25MHz, this time is 2.62ms.

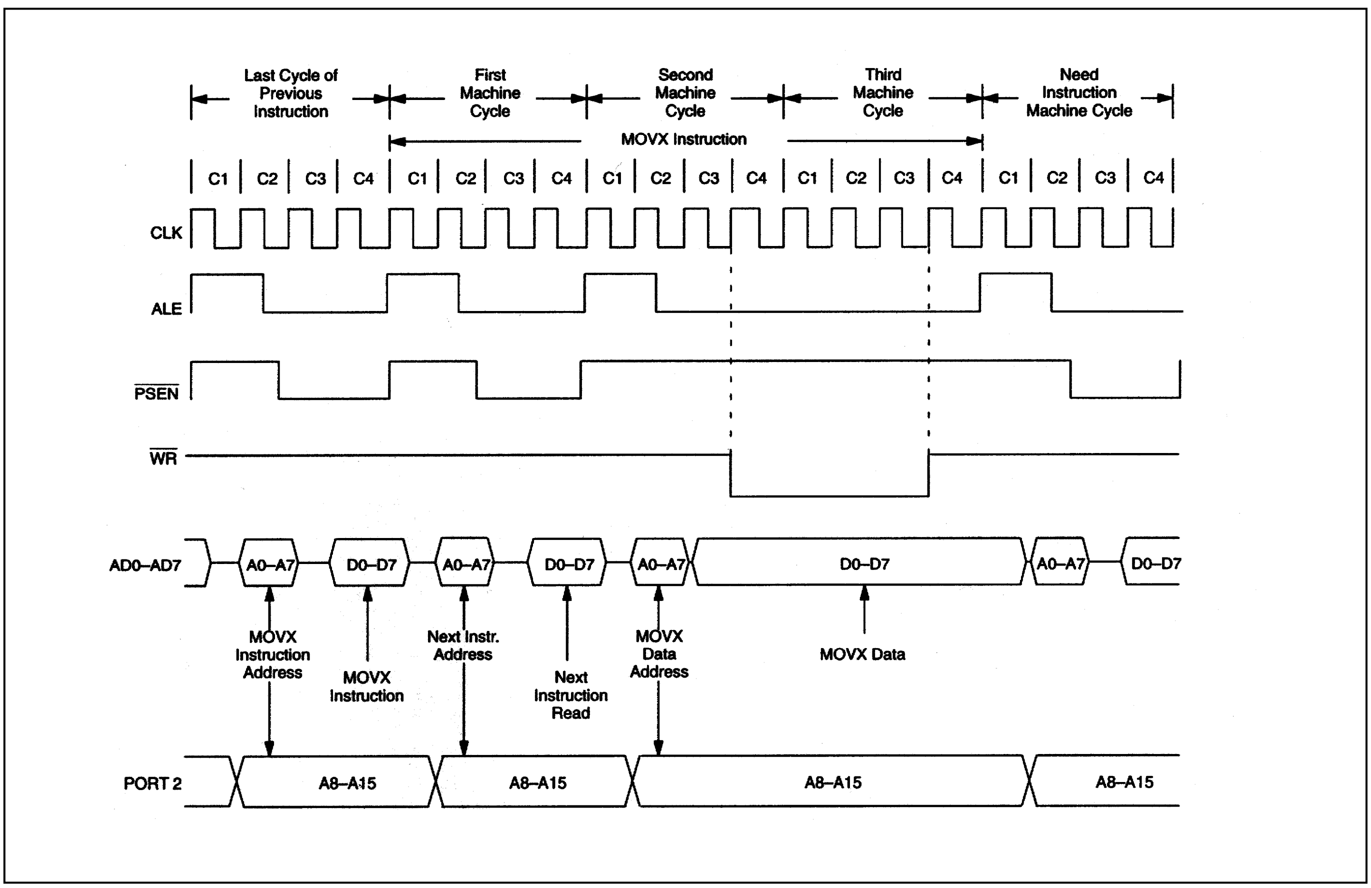
PROGRAM MEMORY READ CYCLE



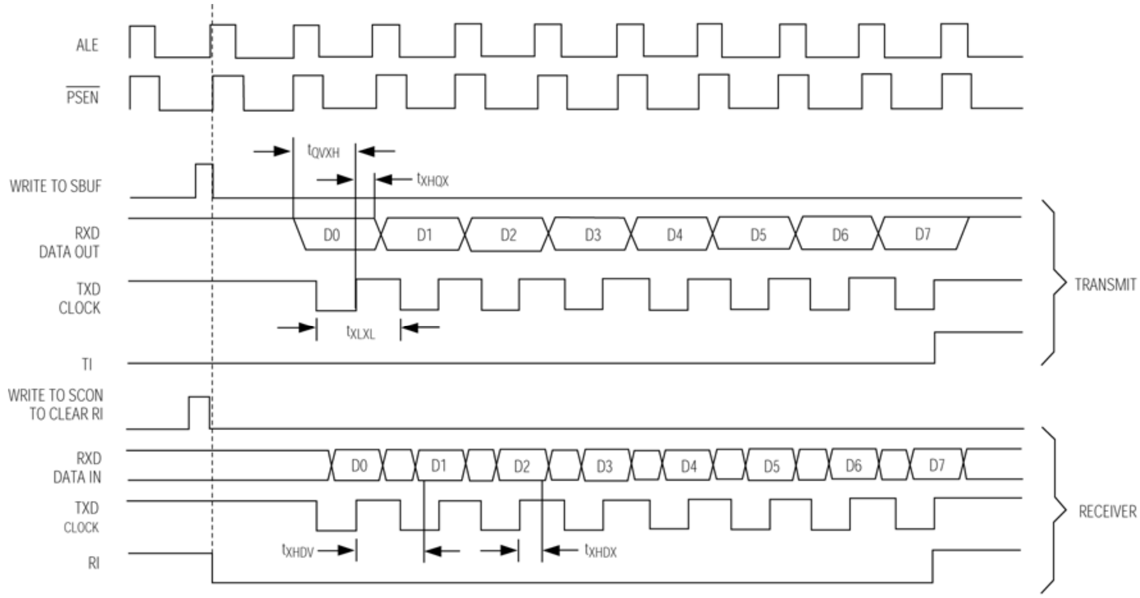
DATA MEMORY WRITE CYCLE



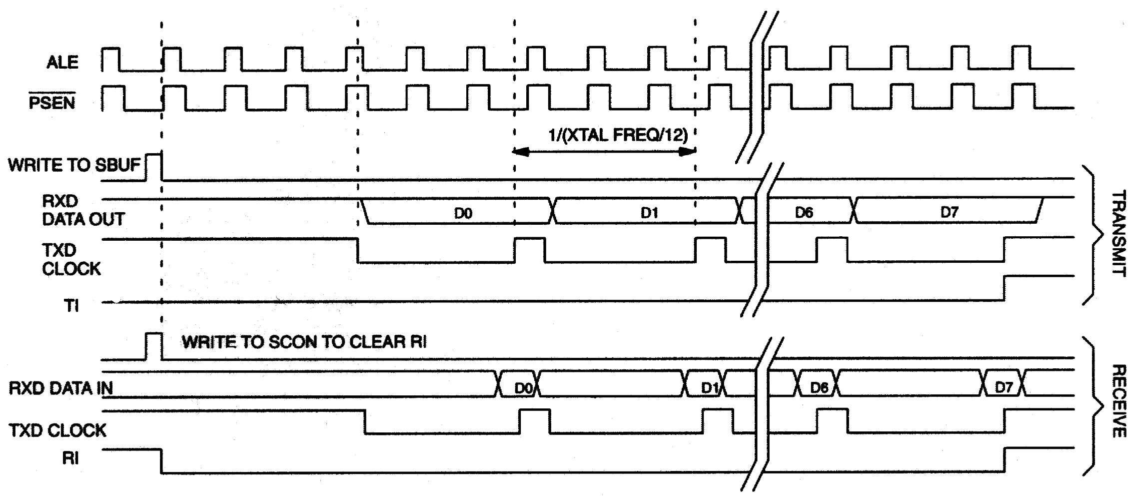
DATA MEMORY WRITE WITH STRETCH = 1



SERIAL PORT MODE 0 TIMING



SERIAL PORT 0 (SYNCHRONOUS MODE)
HIGH SPEED OPERATION SM2 = 1 ≥ TXD CLOCK = XTAL/4



SERIAL PORT 0 (SYNCHRONOUS MODE)
SM2 = 0 ≥ TXD CLOCK = XTAL/12

DATA SHEET REVISION SUMMARY

The following represent the key differences between the 101006 and 070505 version of the DS80C320/DS80C323 data sheet. Please review this summary carefully.

1. Deleted DS80C323-MND from Ordering Information table (page 2). Device was never manufactured.

The following represent the key differences between the 070505 and 051804 version of the DS80C320/DS80C323 data sheet. Please review this summary carefully.

2. Added Pb-free/RoHS-compliant part numbers to Ordering Information table.
3. Deleted the "A" from the IPC/JEDEC J-STD-020 specification in the Absolute Maximum Ratings.

The following represent the key differences between the 051804 and the 112299 version of the DS80C320/DS80C323 data sheet. Please review this summary carefully.

1. Removed "Preliminary" status as a result of final characterization.
2. Added industrial temperature DS80C323 devices to ordering information.
3. Updated soldering temperature specification to reflect JEDEC standards.
4. Updated the following DS80C323 AC timing parameters with final characterization data: t_{LHLL}, t_{LLAX1}, t_{LLAX2}, t_{LLAX2}, t_{LLIV}, t_{LLPL}, t_{PLIV}, t_{AVIV1}, t_{RLDV}, t_{RHDZ}, t_{LLDV}, t_{AVDV1}, t_{AVDV2}, t_{LLWL}, t_{AVWL1}, t_{AVWL2}, t_{QVWX}, t_{WHQX}, t_{WHLH}.
5. Updated the following DS80C320 AC timing parameters with final characterization data: t_{WHQX}, t_{LHLL}, t_{LLAX2}, tLLDV, t_{AVDV1}, t_{LLWL}, t_{AVWL1}, t_{AVWL2}.
6. Added note advising the need to reset watchdog timer before setting the Stop bit.
7. Added note clarifying drive strength of P0, P2, ALE, $\overline{\text{PSEN}}$.
8. Obsoleted DS80C320 25MHz AC timing tables; merged into 33MHz AC timing tables.
9. Corrected Serial Port Mode 0 Timing diagrams to show correct order of D6, D7.

The following represent the key differences between the 041896 and the 052799 version of the DS80C320 data sheet. Please review this summary carefully.

1. Corrected V_{CC} pin description to show DS80C323 operation at +3V.
2. Corrected Timed Access description to show three-cycle window.
3. Modified absolute Maximum Ratings for any pin relative to around, V_{CC} relative to ground.
4. Changed minimum oscillator frequency to 1MHz when using external crystal.
5. Clarified that t_{POR} begins when XTAL1 reaches V_{IH2}.

The following represent the key differences between the 103196 and the 041896 version of the DS80C320 data sheet. Please review this summary carefully.

1. Updated DS80C320 25MHz AC Characteristics.

The following represent the key differences between the 041895 and the 031096 version of the DS80C320 data sheet. Please review this summary carefully.

1. Remove Port 0, Port 2 from V_{OH1} specification (PCN B60802).
2. V_{OH1} test specification clarified (RST = V_{CC}).
3. Add t_{AVWL2} marking to External Memory Read Cycle figure.
4. Correct TQFP drawing to read 44-pin TQFP.
5. Rotate page 1 TQFP illustration to match assembly specifications.

The following represent the key differences between the 031096 and the 052296 version of the DS80C320 data sheet. Please review this summary carefully.

1. Added *Data Sheet Revision Summary* section.

The following represent the key differences between 05/23/96 and 05/22/96 version of the DS80C320 data sheet and between 05/23/96 and 03/27/95 version of the DS80C323 data sheet. Please review this summary carefully.

DS80C320:

1. Add DS80C323 Characteristics.
2. Change DS80C320 V_{PFW} specification from 4.5V to 4.55V (PCN E62802).
3. Update DS80C320 33MHz AC Characteristics.

DS80C323:

1. Delete Data Sheet. Contents moved to DS80C320/DS80C323.

DATA SHEET REVISION SUMMARY (continued)

The following represent the key differences between the 05/22/96 and the 10/21/97 version of the DS80C320 data sheet. Please review this summary carefully.

DS80C320

1. Added note to clarify I_{IL} specification.
2. Added note to clarify AC timing conditions.
3. Corrected erroneous t_{QVXL} label on figure "Serial Port Mode 0 Timing" to read t_{QVXH}.
4. Added note to prevent accidental corruption of Watchdog Timer count while changing counter length.

DS80C323

1. Added note to clarify I_{IL} specification.
2. Remove port 2 from V_{OH1} specification, add port 3.
3. I_{OH} for V_{OH3} specification changed from -3mA to -2mA.
4. Added note to clarify AC timing conditions.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600