Analog Devices Inc./Maxim Integrated - DS80C320-MCL Datasheet

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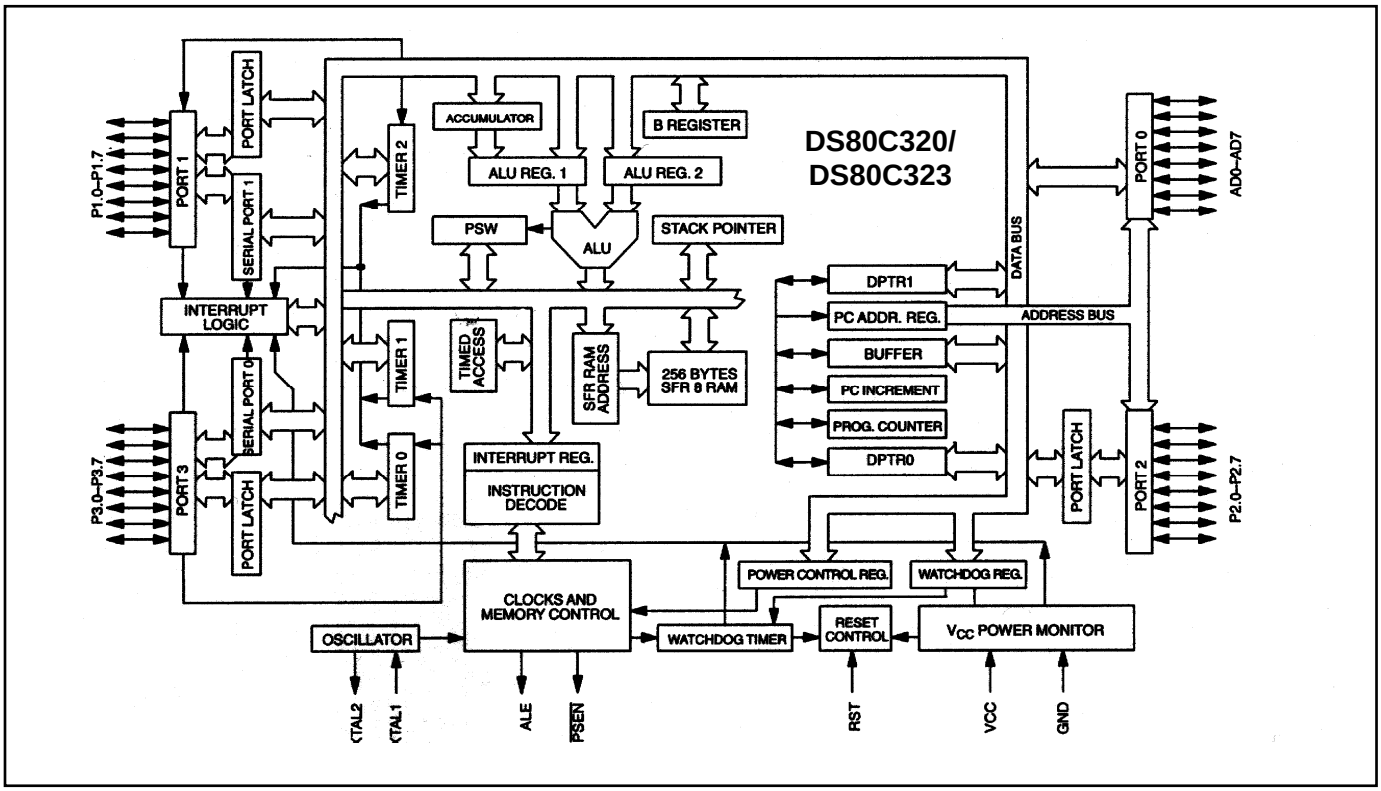
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds80c320-mcl

Figure 1. Block Diagram



PIN DESCRIPTION

PIN			NAME	FUNCTION
DIP	PLCC	TQFP		
40	44	38	V_{CC}	**+5V (+3V for DS80C323)**
20	22, 23	16, 17	GND	**Digital Circuit Ground**
9	10	4	RST	**Reset Input.** The RST input pin contains a Schmitt voltage input to recognize external active-high reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wired OR external reset sources. An RC is ***not*** required for power-up, as the device provides this function internally.
18	20	14	XTAL2	**Crystal Oscillator Pins.** XTAL1 and XTAL2 provide support for parallel-resonant, AT-cut crystals. XTAL1 acts also as an input in the event that an external clock source is used in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
19	21	15	XTAL1	
29	32	26	$\overline{\text{PSEN}}$	**Program Store-Enable Output, Active Low.** This signal is commonly connected to external ROM memory as a chip enable. $\overline{\text{PSEN}}$ provides an active-low pulse width of 2.25 XTAL1 cycles with a period of four XTAL1 cycles. $\overline{\text{PSEN}}$ is driven high when data memory (RAM) is being accessed through the bus and during a reset condition.

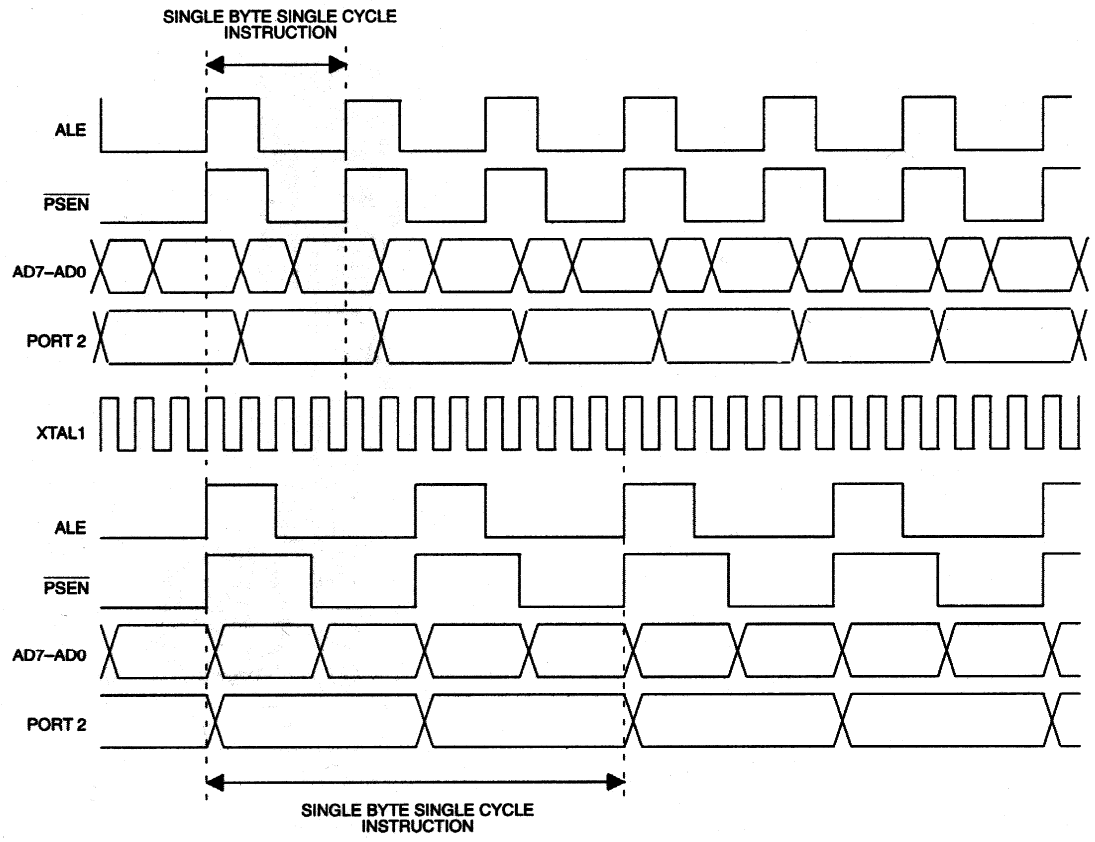
PIN DESCRIPTION (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>TQFP</th></tr>
<tr><td>30</td><td>33</td><td>27</td><td>ALE</td><td>Address Latch-Enable Output. This pin functions as a clock to latch the external address LSB from the multiplexed address/data bus. This signal is commonly connected to the latch enable of an external 373 family transparent latch. ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. ALE is forced high when the device is in a reset condition.</td></tr>
<tr><td>39</td><td>43</td><td>37</td><td>AD0</td><td rowspan="8">Port 0, Input/Output. Port 0 is the multiplexed address/data bus. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls, the port transitions to a bidirectional data bus. This bus is used to read external ROM and read/write external RAM memory or peripherals. The Port 0 has no true port latch and cannot be written directly by software. The reset condition of Port 0 is high. No pullup resistors are needed.</td></tr>
<tr><td>38</td><td>42</td><td>36</td><td>AD1</td></tr>
<tr><td>37</td><td>41</td><td>35</td><td>AD2</td></tr>
<tr><td>36</td><td>40</td><td>34</td><td>AD3</td></tr>
<tr><td>35</td><td>39</td><td>33</td><td>AD4</td></tr>
<tr><td>34</td><td>38</td><td>32</td><td>AD5</td></tr>
<tr><td>33</td><td>37</td><td>31</td><td>AD6</td></tr>
<tr><td>32</td><td>36</td><td>30</td><td>AD7</td></tr>
<tr><td>1–8</td><td>2–9</td><td>40–44, 1–3</td><td>P1.0–P1.7</td><td>Port 1, I/O. Port 1 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for Timer 2 I/O, new External Interrupts, and new Serial Port 1. The reset condition of Port 1 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the device will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port once again becomes the output high (and input) state. The alternate modes of Port 1 are outlined as follows:
<table>
<tr><th colspan="3">PIN</th><th rowspan="2">PORT</th><th rowspan="2">ALTERNATE</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>TQFP</th></tr>
<tr><td>1</td><td>2</td><td>40</td><td>P1.0</td><td>T2</td><td>External I/O for Timer/Counter 2</td></tr>
<tr><td>2</td><td>3</td><td>41</td><td>P1.1</td><td>T2EX</td><td>Timer/Counter 2 Capture/Reload Trigger</td></tr>
<tr><td>3</td><td>4</td><td>42</td><td>P1.2</td><td>RXD1</td><td>Serial Port 1 Input</td></tr>
<tr><td>4</td><td>5</td><td>43</td><td>P1.3</td><td>TXD1</td><td>Serial Port 1 Output</td></tr>
<tr><td>5</td><td>6</td><td>44</td><td>P1.4</td><td>INT2</td><td>External Interrupt 2 (Positive-Edge Detect)</td></tr>
<tr><td>6</td><td>7</td><td>1</td><td>P1.5</td><td>$\overline{\text{INT3}}$</td><td>External Interrupt 3 (Negative-Edge Detect)</td></tr>
<tr><td>7</td><td>8</td><td>2</td><td>P1.6</td><td>INT4</td><td>External Interrupt 4 (Positive-Edge Detect)</td></tr>
<tr><td>8</td><td>9</td><td>3</td><td>P1.7</td><td>$\overline{\text{INT5}}$</td><td>External Interrupt 5 (Negative-Edge Detect)</td></tr>
</table>
</td></tr>
</table>

PIN DESCRIPTION (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>TQFP</th></tr>
<tr><td>21</td><td>24</td><td>18</td><td>A8 (P2.0)</td><td rowspan="8">Port 2, Output. Port 2 serves as the MSB for external addressing. P2.7 is A15 and P2.0 is A8. The device will automatically place the MSB of an address on P2 for external ROM and RAM access. Although Port 2 can be accessed like an ordinary I/O port, the value stored on the Port 2 latch will never be seen on the pins (due to memory access). Therefore, writing to Port 2 in software is only useful for the instructions MOVX A, @Ri or MOVX @Ri, A. These instructions use the Port 2 internal latch to supply the external address MSB. In this case, the Port 2 latch value will be supplied as the address information.</td></tr>
<tr><td>22</td><td>25</td><td>19</td><td>A9 (P2.1)</td></tr>
<tr><td>23</td><td>26</td><td>20</td><td>A10 (P2.2)</td></tr>
<tr><td>24</td><td>27</td><td>21</td><td>A11 (P2.3)</td></tr>
<tr><td>25</td><td>28</td><td>22</td><td>A12 (P2.4)</td></tr>
<tr><td>26</td><td>29</td><td>23</td><td>A13 (P2.5)</td></tr>
<tr><td>27</td><td>30</td><td>24</td><td>A14 (P2.6)</td></tr>
<tr><td>28</td><td>31</td><td>25</td><td>A15 (P2.7)</td></tr>
<tr><td>10–17</td><td>11, 13–19</td><td>5, 7–13</td><td>P3.0–P3.7</td><td>Port 3, Input/Output. Port 3 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for External Interrupts, Serial Port 0, Timer 0 & 1 Inputs, $\overline{RD}$ and $\overline{WR}$ strobes. The reset condition of Port 3 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the device will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port once again becomes both the output high and input state. The alternate modes of Port 3 are outlined below:
<table>
<tr><th colspan="3">PIN</th><th rowspan="2">PORT</th><th rowspan="2">ALTERNATE</th><th rowspan="2">MODE</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>TQFP</th></tr>
<tr><td>10</td><td>11</td><td>5</td><td>P3.0</td><td>RXD0</td><td>Serial Port 0 Input</td></tr>
<tr><td>11</td><td>13</td><td>7</td><td>P3.1</td><td>TXD0</td><td>Serial Port 0 Output</td></tr>
<tr><td>12</td><td>14</td><td>8</td><td>P3.2</td><td>$\overline{INT0}$</td><td>External Interrupt 0</td></tr>
<tr><td>13</td><td>15</td><td>9</td><td>P3.3</td><td>$\overline{INT1}$</td><td>External Interrupt 1</td></tr>
<tr><td>14</td><td>16</td><td>10</td><td>P3.4</td><td>T0</td><td>Timer 0 External Input</td></tr>
<tr><td>15</td><td>17</td><td>11</td><td>P3.5</td><td>T1</td><td>Timer 1 External Input</td></tr>
<tr><td>16</td><td>18</td><td>12</td><td>P3.6</td><td>$\overline{WR}$</td><td>External Data Memory Write Strobe</td></tr>
<tr><td>17</td><td>19</td><td>13</td><td>P3.7</td><td>$\overline{RD}$</td><td>External Data Memory Read Strobe</td></tr>
</table></td></tr>
<tr><td>31</td><td>35</td><td>29</td><td>$\overline{EA}$</td><td>External Access, Active-Low Input. This pin must be connected to ground for proper operation.</td></tr>
<tr><td>—</td><td>12, 34, 1*</td><td>6, 28, 39*</td><td>N.C.</td><td>No Connection (Reserved). These pins should not be connected. They are reserved for use with future devices in this family.
*These pins are reserved for additional ground pins on future products.</td></tr>
</table>

Figure 2. Comparative Timing of the DS80C320/DS80C323 and 80C32



HIGH-SPEED OPERATION

The DS80C320/DS80C323 are built around a high-speed, 80C32-compatible core. Higher speed comes not just from increasing the clock frequency but also from a newer, more efficient design.

In this updated core, dummy memory cycles have been eliminated. In a conventional 80C32, machine cycles are generated by dividing the clock frequency by 12. In the DS80C320/DS80C323, the same machine cycle is performed in 4 clocks. Thus the fastest instruction, one machine cycle, is executed three times faster for the same crystal frequency. Note that these are identical instructions. Figure 2 shows a comparison of the timing differences. The majority of instructions will see the full 3-to-1 speed improvement. Some instructions will get between 1.5X and 2.4X improvement. Note that all instructions are faster than the original 80C51. Table 1 shows a summary of the instruction set, including the speed.

The numerical average of all op codes is approximately a 2.5-to-1 speed improvement. Individual programs are affected differently, depending on the actual instructions used. Speed-sensitive applications would make the most use of instructions that are three times faster. However, the sheer number of 3-to-1 improved op codes makes dramatic speed improvements likely for any code. The Dual Data Pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory.

INSTRUCTION SET SUMMARY

All instructions in the DS80C320/DS80C323 perform the same functions as their 80C32 counterparts. Their effect on bits, flags, and other status functions is identical. However, the timing of each instruction is different. This applies both in absolute and relative number of clocks.

For absolute timing of real-time events, the timing of software loops will need to be calculated using the Table 1. However, counter/timers default to run at the older 12 clocks per increment. Therefore, while software runs at higher speed, timer-based events need no modification to operate as before. Timers can be set to run at 4 clocks per increment cycle to take advantage of higher speed operation.

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture, the “MOVX A, @DPTR” instruction and the “MOV direct, direct” instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS80C320/DS80C323, the MOVX instruction can be done in two machine cycles or eight oscillator cycles, but the “MOV direct, direct” uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times from each other. This is because in most cases, the DS80C320/DS80C323 use one cycle for each byte. The user concerned with precise program timing should examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just four clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV.

Table 1. Instruction Set Summary

SYMBOL	FUNCTION
A	Accumulator
Rn	Register R7 to R0
direct	Internal Register Address
@Ri	Internal Register pointed to by R0 or R1 (except MOVX)
rel	Two's Complement Offset Byte

SYMBOL	FUNCTION
bit	direct bit-address
#data	8-bit constant
#data 16	16-bit constant
addr 16	16-bit destination address
addr 11	11-bit destination address

INSTRUCTION	BYTE	OSCILLATOR CYCLES	INSTRUCTION	BYTE	OSCILLATOR CYCLES
ARITHMATIC INSTRUCTIONS					
ADD A, Rn	1	4	INC A	1	4
ADD A, direct	2	8	INC Rn	1	4
ADD A, @Ri	1	4	INC direct	2	8
ADD A, #data	2	8	INC @Ri	1	4
ADDC A, Rn	1	4	INC DPTR	1	12
ADDC A, direct	2	8	DEC A	1	4
ADDC A, @Ri	1	4	DEC Rn	1	4
ADDC A, #data	2	8	DEC direct	2	8
SUBB A, Rn	1	4	DEC @Ri	1	4
SUBB A, direct	2	8	MUL AB	1	20
SUBB A, @Ri	1	4	DIV AB	1	20
SUBB A, #data	2	8	DA A	1	4
LOGICAL INSTRUCTIONS					
ANL A, Rn	1	4	XRL A, Rn	1	4
ANL A, direct	2	8	XRL A, direct	2	8
ANL A, @Ri	1	4	XRL A, @Ri	1	4
ANL A, #data	2	8	XRL A, #data	2	8
ANL direct, A	2	8	XRL direct, A	2	8
ANL direct, #data	3	12	XRL direct, #data	3	12
ORL A, Rn	1	4	CLR A	1	4
ORL A, direct	2	8	CPL A	1	4
ORL A, @Ri	1	4	RL A	1	4
ORL A, #data	2	8	RLC A	1	4
ORL direct, A	2	8	RR A	1	4
ORL direct, #data	3	12	RRC A	1	4

Table 1. Instruction Set Summary (continued)

INSTRUCTION	BYTE	OSCILLATOR CYCLES	INSTRUCTION	BYTE	OSCILLATOR CYCLES
DATA TRANSFER INSTRUCTIONS					
MOV A, Rn	1	4	MOVC A, @A+DPTR	1	12
MOV A, direct	2	8	MOVC A, @A+PC	1	12
MOV A, @Ri	1	4	MOVX A, @Ri	1	8–36*
MOV A, #data	2	8	MOVX A, @DPTR	1	8–36*
MOV Rn, A	1	4	MOVX @Ri, A	1	8–36*
MOV Rn, direct	2	8	MOVX @DPTR, A	1	8–36*
MOV Rn, #data	2	8	PUSH direct	2	8
MOV direct, A	2	8	POP direct	2	8
MOV direct, Rn	2	8	XCH A, Rn	1	4
MOV direct1, direct2	3	12	XCH A, direct	2	8
MOV direct, @Ri	2	8	XCH A, @Ri	1	4
MOV direct, #data	3	12	XCHD A, @Ri	1	4
MOV @Ri, A	1	4			
MOV @Ri, direct	2	8			
MOV @Ri, #data	2	8			
MOV DPTR, #data 16	3	12			
BIT MANIPULATION INSTRUCTIONS					
CLR C	1	4	ANL C, bit	2	8
CLR bit	2	8	ANL C, $\overline{\text{bit}}$	2	8
SETB C	1	4	ORL C, bit	2	8
SETB bit	2	8	ORL C, $\overline{\text{bit}}$	2	8
CPL C	1	4	MOV C, bit	2	8
CPL bit	2	8	MOV bit, C	2	8
PROGRAM BRANCHING INSTRUCTIONS					
ACALL addr 11	2	12	CJNE A, direct, rel	3	16
LCALL addr 16	3	16	CJNE A, #data, rel	3	16
RET	1	16	CJNE Rn, #data, rel	3	16
RETI	1	16	CJNE Ri, #data, rel	3	16
AJMP addr 11	2	12	NOP	1	4
LJMP addr 16	3	16	JC rel	2	12
SJMP rel	2	12	JNC rel	2	12
JMP @A+DPTR	1	12	JB bit, rel	3	16
JZ rel	2	12	JNB bit, rel	3	16
JNZ rel	2	12	JBC bit, rel	3	16
DJNZ Rn, rel	2	12			
DJNZ direct, rel	3	16			

**User selectable.*

Table 1 shows the speed for each class of instruction. Note that many of the instructions have multiple op codes. There are 255 op codes for 111 instructions. Of the 255 op codes, 159 are three times faster than the original 80C32. While a system that emphasizes those instructions will see the most improvement, the large total number that receive a 3 to 1 improvement assure a dramatic speed increase for any system. The speed improvement summary is provided below.

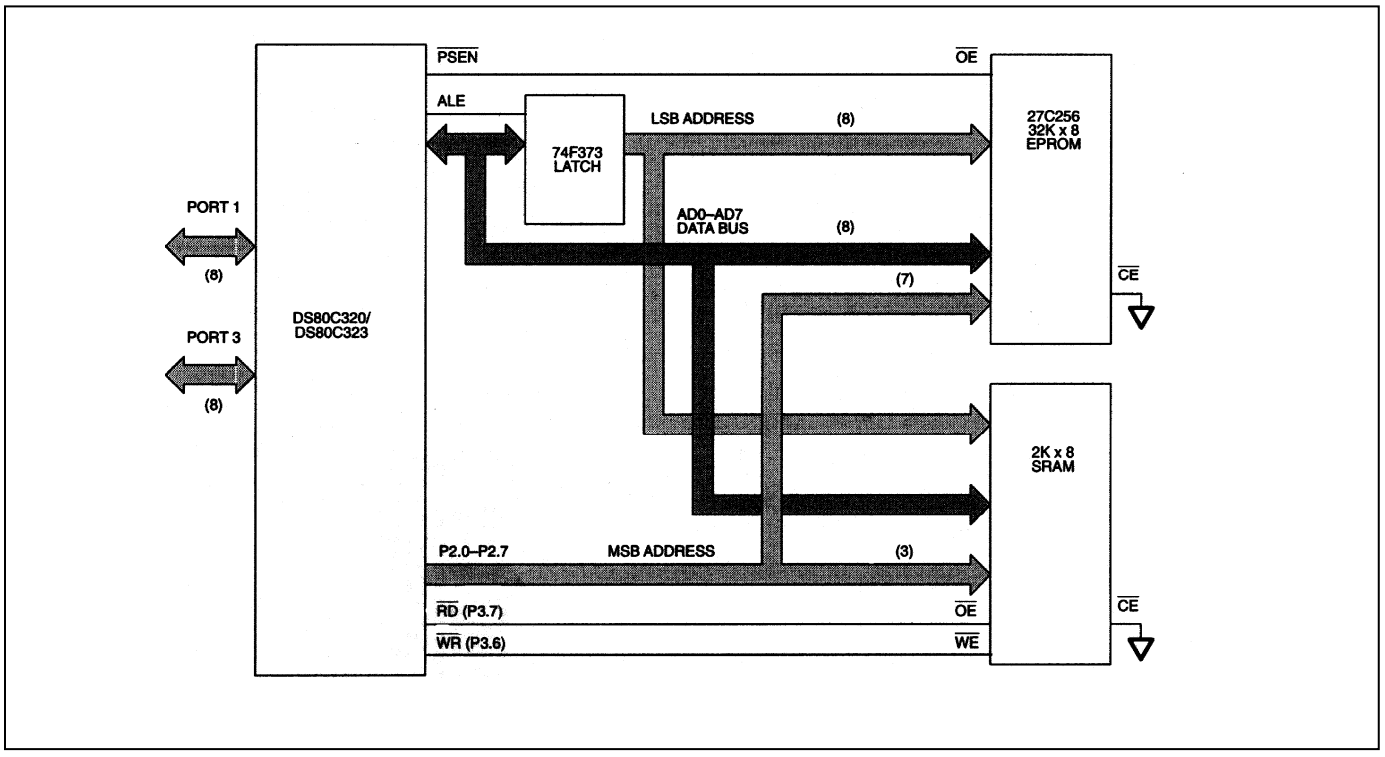
SPEED ADVANTAGE SUMMARY

#OP CODES	SPEED IMPROVEMENT
159	3.0 x
51	1.5 x
43	2.0 x
2	2.4 x
255	Average: 2.5

MEMORY ACCESS

The DS80C320/DS80C323 do not contain on-chip ROM and 256 bytes of scratchpad RAM. Off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. Figure 3 shows a typical memory connection. Timing diagrams are provided in the *Electrical Specifications* section. Program memory (ROM) is accessed at a fixed rate determined by the crystal frequency and the actual instructions. As previously mentioned, an instruction cycle requires 4 clocks. Data memory (RAM) is accessed according to a variable-speed MOVX instruction as described below.

Figure 3. Typical Memory Connection



64-Byte Block Move with Dual Data Pointer

```
; SH and SL are high and low byte source address.
; DH and DL are high and low byte of destination address.
; DPS is the data pointer select. Reset condition is DPS=0, DPTR0 is selected.
                                                                    # CYCLES
EQU     DPS, #86h           ; TELL ASSEMBLER ABOUT DPS

MOV     R5, #64             ; NUMBER OF BYTES TO MOVE               2
MOV     DPTR, #DHDL         ; LOAD DESTINATION ADDRESS              3
INC     DPS                 ; CHANGE ACTIVE DPTR                    2
MOV     DPTR, #SHSL         ; LOAD SOURCE ADDRESS                   2

MOVE:
; THIS LOOP IS PERFORMED THE NUMBER OF TIMES LOADED INTO R5, IN THIS EXAMPLE 64

MOVX    A, @DPTR            ; READ SOURCE DATA BYTE                 2
INC     DPS                 ; CHANGE DPTR TO DESTINATION            2
MOVX    @DPTR, A            ; WRITE DATA TO DESTINATION             2
INC     DPTR                ; NEXT DESTINATION ADDRESS              3
INC     DPS                 ; CHANGE DATA POINTER TO SOURCE         2
INC     DPTR                ; NEXT SOURCE ADDRESS                   3
DJNZ    R5, MOVE            ; FINISHED WITH TABLE?                  3
```

PERIPHERAL OVERVIEW

Peripherals in the DS80C320/DS80C323 are accessed using the SFRs. The devices provide several of the most commonly needed peripheral functions in microcomputer-based systems. These functions are new to the 80C32 family and include a second serial port, power-fail reset, power-fail interrupt, and a programmable watchdog timer. These are briefly described in the following paragraphs. More details are available in the *High-Speed Microcontroller User's Guide*.

SERIAL PORTS

The DS80C320/DS80C323 provide a serial port (UART) that is identical to the 80C32. Many applications require serial communication with multiple devices. Therefore, a second hardware serial port is provided that is a full duplicate of the standard one. It optionally uses pins P1.2 (RXD1) and P1.3 (TXD1). This port has duplicate control functions included in new SFR locations. The second serial port operates in a comparable manner with the first. Both can operate simultaneously but can be at different baud rates.

The second serial port has similar control registers (SCON1 at C0h, SBUF1 at C1h) to the original. One difference is that for timer-based baud rates, the original serial port can use Timer 1 or Timer 2 to generate baud rates. This is selected via SFR bits. The new serial port can only use Timer 1.

TIMER-RATE CONTROL

One important difference exists between the DS80C320/DS80C323 and 80C32 regarding timers. The original 80C32 used a 12 clock-per-cycle scheme for timers and consequently for some serial baud rates (depending on the mode). The DS80C320/DS80C323 architecture normally runs using 4 clocks per cycle. However, in the area of timers, it will default to a 12 clock-per-cycle scheme on a reset. This allows existing code with real-time dependencies such as baud rates to operate properly. If an application needs higher speed timers or serial baud rates, the timers can be set to run at the 4-clock rate.

The Clock Control register (CKCON - 8Eh) determines these timer speeds. When the relevant CKCON bit is a logic 1, the device uses 4 clocks per cycle to generate timer speeds. When the control bit is set to a 0, the device uses 12 clocks for timer speeds. The reset condition is a 0. CKCON.5 selects the speed of Timer 2. CKCON.4 selects Timer 1 and CKCON.3 selects Timer 0. Note that unless a user desires very fast timing, it is unnecessary to alter these bits. Note that the timer controls are independent.

POWER-FAIL RESET

The DS80C320/DS80C323 incorporate a precision bandgap voltage reference to determine when V_{CC} is out of tolerance. While powering up, internal circuits will hold the device in a reset state until V_{CC} rises above the V_{RST} reset threshold. Once V_{CC} is above this level, the oscillator will begin running. An internal reset circuit will then count 65,536 clocks to allow time for power and the oscillator to stabilize. The microcontroller will then exit the reset condition. No external components are needed to generate a power on reset. During power-down or during a severe power glitch, as V_{CC} falls below V_{RST}, the microcontroller will also generate its own reset. It will hold the reset condition as long as power remains below the threshold. This reset will occur automatically, needing no action from the user or from the software. See the *Electrical Specifications* section for the exact value of V_{RST}.

POWER-FAIL INTERRUPT

The same reference that generates a precision reset threshold can also generate an optional early warning Power-fail Interrupt (PFI). When enabled by the application software, this interrupt always has the highest priority. On detecting that the V_{CC} has dropped below V_{PFW} and that the PFI is enabled, the processor will vector to ROM address 0033h. The PFI enable is located in the Watchdog Control SFR (WDCON to D8h). Setting WDCON.5 to logic 1 will enable the PFI. The application software can also read a flag at WDCON.4. This bit is set when a PFI condition has occurred. The flag is independent of the interrupt enable and software must manually clear it.

WATCHDOG TIMER

For applications that cannot afford to run out of control, the DS80C320/DS80C323 incorporate a programmable watchdog timer circuit. The watchdog timer circuit resets the microcontroller if software fails to reset the watchdog before the selected time interval has elapsed. The user selects one of four timeout values. After enabling the watchdog, software must reset the timer prior to expiration of the interval, or the CPU will be reset. Both the Watchdog Enable and the Watchdog Reset bits are protected by a "Timed Access" circuit. This prevents accidentally clearing the watchdog. Timeout values are precise since they are related to the crystal frequency as shown in Table 3. For reference, the time periods at 25MHz are also shown.

The watchdog timer also provides a useful option for systems that may not require a reset. If enabled, then 512 clocks before giving a reset, the watchdog will give an interrupt. The interrupt can also serve as a convenient time-base generator, or be used to wake-up the processor from Idle mode. The watchdog function is controlled in the Clock Control (CKCON to 8Eh), Watchdog Control (WDCON to D8h), and Extended Interrupt Enable (EIE to E8h) SFRs. CKCON.7 and CKCON.6 are called WD1 and WD0, respectively, and are used to select the watchdog timeout period as shown in Table 3.

Table 3. Watchdog Timeout Values

WD1	WD0	INTERRUPT TIMEOUT	TIME (at 25MHz)	RESET TIMEOUT	TIME (at 25MHz)
0	0	2^{17} clocks	5.243ms	2^{17} + 512 clocks	5.263ms
0	1	2^{20} clocks	41.94ms	2^{20} + 512 clocks	41.96ms
1	0	2^{23} clocks	335.54ms	2^{23} + 512 clocks	335.56ms
1	1	2^{26} clocks	2684.35ms	2^{26} + 512 clocks	2684.38ms

As Table 3 shows, the watchdog timer uses the crystal frequency as a time base. A user selects one of four counter values to determine the timeout. These clock counter lengths are 2^{17} = 131,072 clocks; 2^{20} = 1,048,576; 2^{23} = 8,388,608 clocks; or 2^{26} = 67,108,864 clocks. The times shown in Table 4 are with

POWER MANAGEMENT

The DS80C320/DS80C323 provide the standard Idle and power-down (Stop) modes that are available on the standard 80C32. However, the device has enhancements that make these modes more useful, and allow more power saving.

The Idle mode is invoked by setting the LSB of the Power Control register (PCON to 87h). Idle will leave internal clocks, serial port and timer running. No memory access will be performed so power is dramatically reduced. Since clocks are running, the Idle power consumption is related to crystal frequency. It should be approximately one-half the operational power. The CPU can exit the Idle state with any interrupt or a reset.

The power-down or Stop mode is invoked by setting the PCON.1 bit. Stop mode is a lower power state than Idle since it turns off all internal clocking. The I_{CC} of a standard Stop mode is approximately 1 µA but is specified in the *Electrical Specifications* section. The CPU will exit Stop mode from an external interrupt or a reset condition.

Note that internally generated interrupts (timer, serial port, watchdog) are not useful in Idle or Stop since they require clocking activity.

IDLE MODE ENHANCEMENTS

A simple enhancement to Idle mode makes it substantially more useful. The innovation involves not the Idle mode itself, but the watchdog timer. As mentioned above, the Watchdog Timer provides an optional interrupt capability. This interrupt can provide a periodic interval timer to bring the DS80C320/DS80C323 out of Idle mode. This can be useful even if the Watchdog is not normally used. By enabling the Watchdog Timer and its interrupt prior to invoking Idle, a user can periodically come out of Idle perform an operation, then return to Idle until the next operation. This will lower the overall power consumption. When using the Watchdog Interrupt to cancel the Idle state, make sure to restart the Watchdog Timer or it will cause a reset.

STOP MODE ENHANCEMENTS

The DS80C320/DS80C323 provide two enhancements to the Stop mode. As documented above, the device provides a bandgap reference to determine Power-fail Interrupt and Reset thresholds. The default state is that the bandgap reference is off when Stop mode is invoked. This allows the extremely low power state mentioned above. A user can optionally choose to have the bandgap enabled during Stop mode. This means that PFI and power-fail reset will be activated and are valid means for leaving Stop mode.

In Stop mode with the bandgap on, I_{CC} will be approximately 50µA compared with 1µA with the bandgap off. If a user does not require a Power-fail Reset or Interrupt while in Stop mode, the bandgap can remain turned off. Note that only the most power sensitive applications should turn off the bandgap, as this results in an uncontrolled power-down condition.

The control of the bandgap reference is located in the Extended Interrupt Flag register (EXIF to 91h). Setting BGS (EXIF.0) to a 1 will leave the bandgap reference enabled during Stop mode. The default or reset condition is with the bit at a logic 0. This results in the bandgap being turned off during Stop mode. Note that this bit has no control of the reference during full power or Idle modes. Be aware that the DS80C320 and DS80C323 require that the reset watchdog timer bit (RWT;WDCON.0) be set

Figure 4. Ring Oscillator Startup

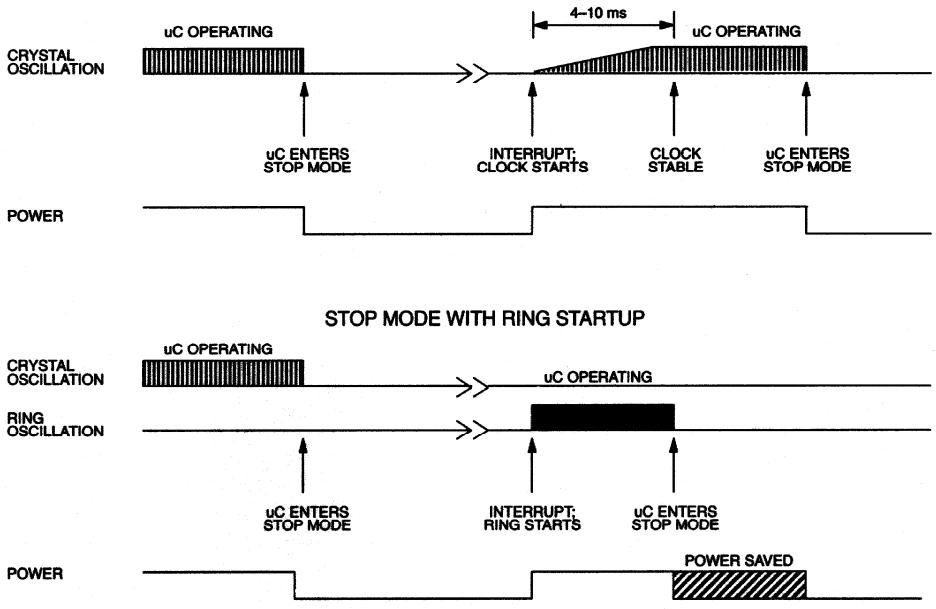


DIAGRAM ASSUMES THAT THE OPERATION FOLLOWING STOP REQUIRES LESS THAN 18ms COMPLETE.

TIMED ACCESS PROTECTION

Selected SFR bits are critical to operation, making it desirable to protect against an accidental write operation. The Timed Access procedure prevents an errant CPU from accidentally altering a bit that would cause difficulty. The Timed Access procedure requires that the write of a protected bit be preceded by the following instructions:

```
MOV     0C7h, #0AAh
MOV     0C7h, #55h
```

By writing an AAh followed by a 55h to the Timed Access register (location C7h), the hardware opens a three-cycle window that allows software to modify one of the protected bits. If the instruction that seeks to modify the protected bit is not immediately proceeded by these instructions, the write will not take effect. The protected bits are:

EXIF.0	BGS Bandgap Select
WDCON.6	POR Power-on Reset flag
WDCON.1	EWT Enable Watchdog
WDCON.0	RWT Reset Watchdog
WDCON.3	WDIF Watchdog Interrupt Flag

SPECIAL-FUNCTION REGISTERS

Most special features of the DS80C320/DS80C323 or 80C32 are controlled by bits in the SFRs, allowing the devices to add many features but use the same instruction set. When writing software to use a new feature, the SFR must be defined to an assembler or compiler using an equate statement. This is the only change needed to access the new function. The DS80C320/DS80C323 duplicate the SFRs that are contained in the standard 80C32. Table 5 shows the register addresses and bit locations. Many are standard 80C32 registers. The *High-Speed Microcontroller User's Guide* describes all SFRs.

Table 5. Special-Function Register Locations

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**SEL**	86h
PCON	SMOD_0	**SMOD0**	—	—	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	**WD1**	**WD0**	**T2M**	**T1M**	**T0M**	**MD2**	**MD1**	**MD0**	8Eh
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
EXIF	**IE5**	**IE4**	**IE3**	**IE2**	—	**RGMD**	**RGSL**	**BGS**	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
P2	P2.0	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	A8h
SADDR0									A9h
SADDR1									AAh
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
IP	—	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
SCON1	**SM0/FE_0**	**SM1_0**	**SM2_0**	**REN_0**	**TB8_0**	**RB8_0**	**TI_0**	**RI_0**	C0h
SBUF1									C1h
STATUS	PIP	HIP	LIP	1	1	1	1	1	C5h
TA									C7h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	C8h
T2MOD	—	—	—	—	—	—	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	FL	P	D0h
WDCON	**SMOD_1**	**POR**	**EPFI**	**PFI**	**WDIF**	**WTRF**	**EWT**	**RWT**	D8h
ACC									E0h
EIE	—	—	—	**EWDI**	**EX5**	**EX4**	**EX3**	**EX2**	E8h
B									F0h
EIP	—	—	—	**PWDI**	**PX5**	**PX4**	**PX3**	**PX2**	F8h

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground……..-0.3V to +6.0V
Operating Temperature Range……-40°C to +85°C
Storage Temperature Range……..-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS—DS80C320

(V_{CC} = 4.5V to 5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Power-Fail Warning Voltage	V_{PFW}	4.25	4.38	4.55	V	1
Minimum Operating Voltage	V_{RST}	4.0	4.1	4.25	V	1, 12
Supply Current Active Mode at 25MHz	I_{CC}		30	45	mA	2
Supply Current Idle Mode at 25MHz	I_{IDLE}		15	25	mA	3
Supply Current Active Mode at 33MHz	I_{CC}		35		mA	2
Supply Current Idle Mode at 33MHz	I_{IDLE}		20		mA	3
Supply Current Stop Mode, Bandgap Reference Disabled	I_{STOP}		0.01	1	µA	4
Supply Current Stop Mode, Bandgap Reference Enabled	I_{SPBG}		50	80	µA	4, 10
Input Low Level	V_{IL}	-0.3		+0.8	V	1
Input High Level (Except XTAL1 and RST)	V_{IH1}	2.0		V_{CC} + 0.3	V	1
Input High Level XTAL1 and RST	V_{IH2}	3.5		V_{CC} + 0.3	V	1
Output-Low Voltage Ports 1, 3 at I_{OL} = 1.6mA	V_{OL1}			0.45	V	1
Output-Low Voltage Ports 0, 2, ALE, $\overline{PSEN}$ at I_{OL} = 3.2mA	V_{OL2}			0.45	V	1, 5
Output-High Voltage Ports 1, 3, ALE, $\overline{PSEN}$ at I_{OH} = -50µA	V_{OH1}	2.4			V	1, 6
Output High Voltage Ports 1, 3 at I_{OH} = -1.5mA	V_{OH2}	2.4			V	1, 7
Output-High Voltage Ports 0, 2, ALE, $\overline{PSEN}$ at I_{OH} = -8mA	V_{OH3}	2.4			V	1, 5
Input Low Current Ports 1, 3 at 0.45V	I_{IL}			-55	µA	11
Transition Current from 1 to 0 Ports 1, 3 at 2V	I_{TL}			-650	µA	8
Input Leakage Port 0, Bus Mode	I_L	-300		+300	µA	9
RST Pulldown Resistance	R_{RST}	50		170	kΩ	

MOVX CHARACTERISTICS—DS80C320

PARAMETER	SYMBOL	VARIABLE CLOCK		UNITS	STRETCH
		MIN	MAX		
$\overline{RD}$ Pulse Width	t_{RLRH}	$2t_{CLCL}$-11		ns	t_{MCS}=0
		t_{MCS}-11			t_{MCS}>0
$\overline{WR}$ Pulse Width	t_{WLWH}	$2t_{CLCL}$-11		ns	t_{MCS}=0
		t_{MCS}-11			t_{MCS}>0
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2t_{CLCL}$-25	ns	t_{MCS}=0
			t_{MCS}-25		t_{MCS}>0
Data Hold After Read	t_{RHDX}	0		ns	
Data Float After Read	t_{RHDZ}		t_{CLCL}-5	ns	t_{MCS}=0
			$2t_{CLCL}$-5		t_{MCS}>0
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL}$-27	ns	t_{MCS}=0
			$1.5t_{CLCL}$-28+t_{MCS}		t_{MCS}>0
Port 0 Address to Valid Data In	t_{AVDV1}		$3t_{CLCL}$-27	ns	t_{MCS}=0
			$2t_{CLCL}$-31+t_{MCS}		t_{MCS}>0
Port 2 Address to Valid Data In	t_{AVDV2}		$3.5t_{CLCL}$-32	ns	t_{MCS}=0
			$2.5t_{CLCL}$-34+t_{MCS}		t_{MCS}>0
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL}$-8	$0.5t_{CLCL}$+6	ns	t_{MCS}=0
		$1.5t_{CLCL}$-7	$1.5t_{CLCL}$+8		t_{MCS}>0
Port 0 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	t_{CLCL}-11		ns	t_{MCS}=0
		$2t_{CLCL}$-10			t_{MCS}>0
Port 2 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL}$-9		ns	t_{MCS}=0
		$2.5t_{CLCL}$-13			t_{MCS}>0
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-9		ns	t_{MCS}=0
		t_{CLCL}-10			t_{MCS}>0
Data Hold After Write	t_{WHQX}	t_{CLCL}-12		ns	t_{MCS}=0
		$2t_{CLCL}$-7			t_{MCS}>0
$\overline{RD}$ Low to Address Float	t_{RLAZ}		(Note 5)	ns	
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{WHLH}	0	10	ns	t_{MCS}=0
		t_{CLCL}-5	t_{CLCL}+11		t_{MCS}>0

Note: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.

M2	M1	M0	MOVX CYCLES	t_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles (default)	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

AC ELECTRICAL CHARACTERISTICS—DS80C323

PARAMETER		SYMBOL	18 MHz		VARIABLE CLOCK		UNITS
			MIN	MAX	MIN	MAX	
Oscillator Frequency	External Oscillator	$1/t_{CLCL}$	0	18	0	18	MHz
	External Crystal		1	18	1	18	
ALE Pulse Width		t_{LHLL}	68		$1.5t_{CLCL}$-15		ns
Port 0 Address Valid to ALE Low		t_{AVLL}	16		$0.5t_{CLCL}$-11		ns
Address Hold After ALE Low		t_{LLAX1}	6	(Note 5)	$0.25t_{CLCL}$-8	(Note 5)	ns
Address Hold After ALE Low for MOVX $\overline{WR}$		t_{LLAX2}	14		$0.5t_{CLCL}$-13		ns
ALE Low to Valid Instruction In		t_{LLIV}		93		$2.5t_{CLCL}$-46	ns
ALE Low to $\overline{PSEN}$ Low		t_{LLPL}	4		$0.25t_{CLCL}$-10		ns
$\overline{PSEN}$ Pulse Width		t_{PLPH}	118		$2.25t_{CLCL}$-7		ns
$\overline{PSEN}$ Low to Valid Instruction In		t_{PLIV}		87		$2.25t_{CLCL}$-38	ns
Input Instruction Hold After $\overline{PSEN}$		t_{PXIX}	0		0		ns
Input Instruction Float After $\overline{PSEN}$		t_{PXIZ}		51		t_{CLCL}-5	ns
Port 0 Address to Valid Instruction In		t_{AVIV1}		128		$3t_{CLCL}$-39	ns
Port 2 Address to Valid Instruction In		t_{AVIV2}		139		$3.5t_{CLCL}$-56	ns
$\overline{PSEN}$ Low to Address Float		t_{PLAZ}		(Note 5)		(Note 5)	ns

NOTES FOR DS80C323 AC ELECTRICAL CHARACTERISTICS

All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested. AC electrical characteristics assume 50% duty cycle for the oscillator, oscillator frequency > 16MHz, and are not 100% production tested, but are guaranteed by design.

1. All signals rated over operating temperature at 18MHz.
2. All signals characterized with load capacitance of 80pF except Port 0, ALE, $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}$ at 100pF. Note that loading should be approximately equal for valid timing.
3. Interfacing to memory devices with float times (turn off times) over 35ns may cause contention. This will not damage the parts, but will cause an increase in operating current.
4. Specifications assume a 50% duty cycle for the oscillator. Port 2 timing will change with the duty cycle variations.
5. Address is held in a weak latch until over-driven by external memory.

EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Clock High Time	t_{CHCX}	10			ns
Clock Low Time	t_{CLCX}	10			ns
Clock Rise Time	t_{CLCH}			5	ns
Clock Fall Time	t_{CHCL}			5	ns

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

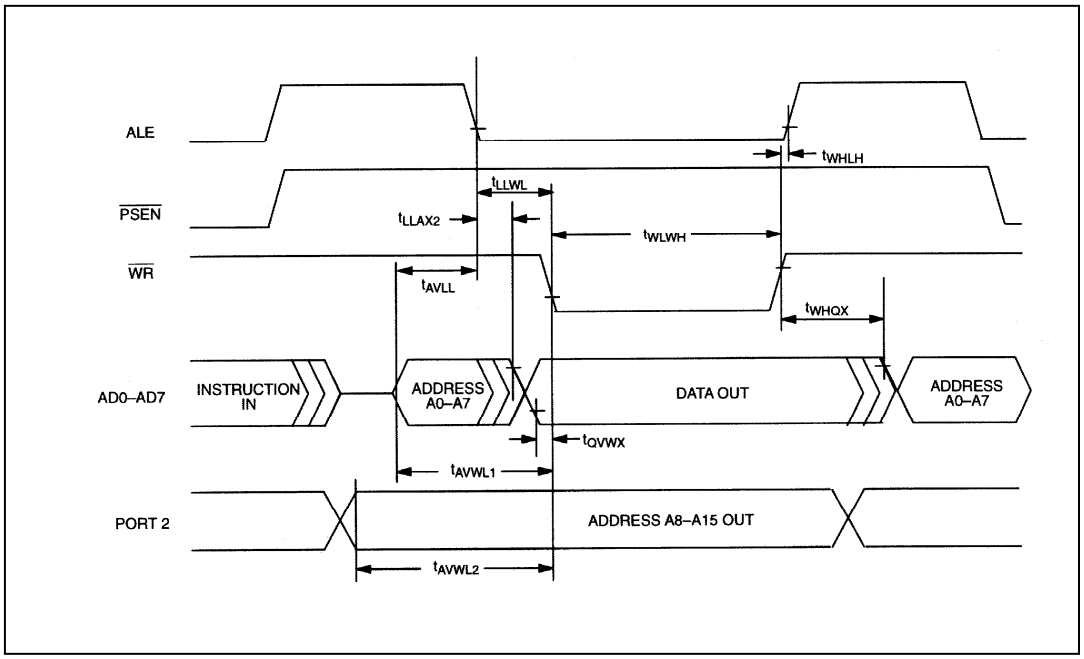
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Port Clock Cycle Time	t_{XLXL}	SM2 = 0; 12 clocks per cycle		$12t_{CLCL}$		ns
		SM2 = 1; 4 clocks per cycle		$4t_{CLCL}$		
Output Data Setup to Clock Rising Edge	t_{QVXH}	SM2 = 0 12 clocks per cycle		$10t_{CLCL}$		ns
		SM2 = 1; 4 clocks per cycle		$3t_{CLCL}$		
Output Data Hold from Clock Rising	t_{XHQX}	SM2 = 0 12 clocks per cycle		$2t_{CLCL}$		ns
		SM2 = 1; 4 clocks per cycle		t_{CLCL}		
Input Data Hold After Clock Rising	t_{XHDX}	SM2 = 0; 12 clocks per cycle		t_{CLCL}		ns
		SM2 = 1; 4 clocks per cycle		t_{CLCL}		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0; 12 clocks per cycle		$11t_{CLCL}$		ns
		SM2 = 1 4 clocks per cycle		$2t_{CLCL}$		

EXPLANATION OF AC SYMBOLS

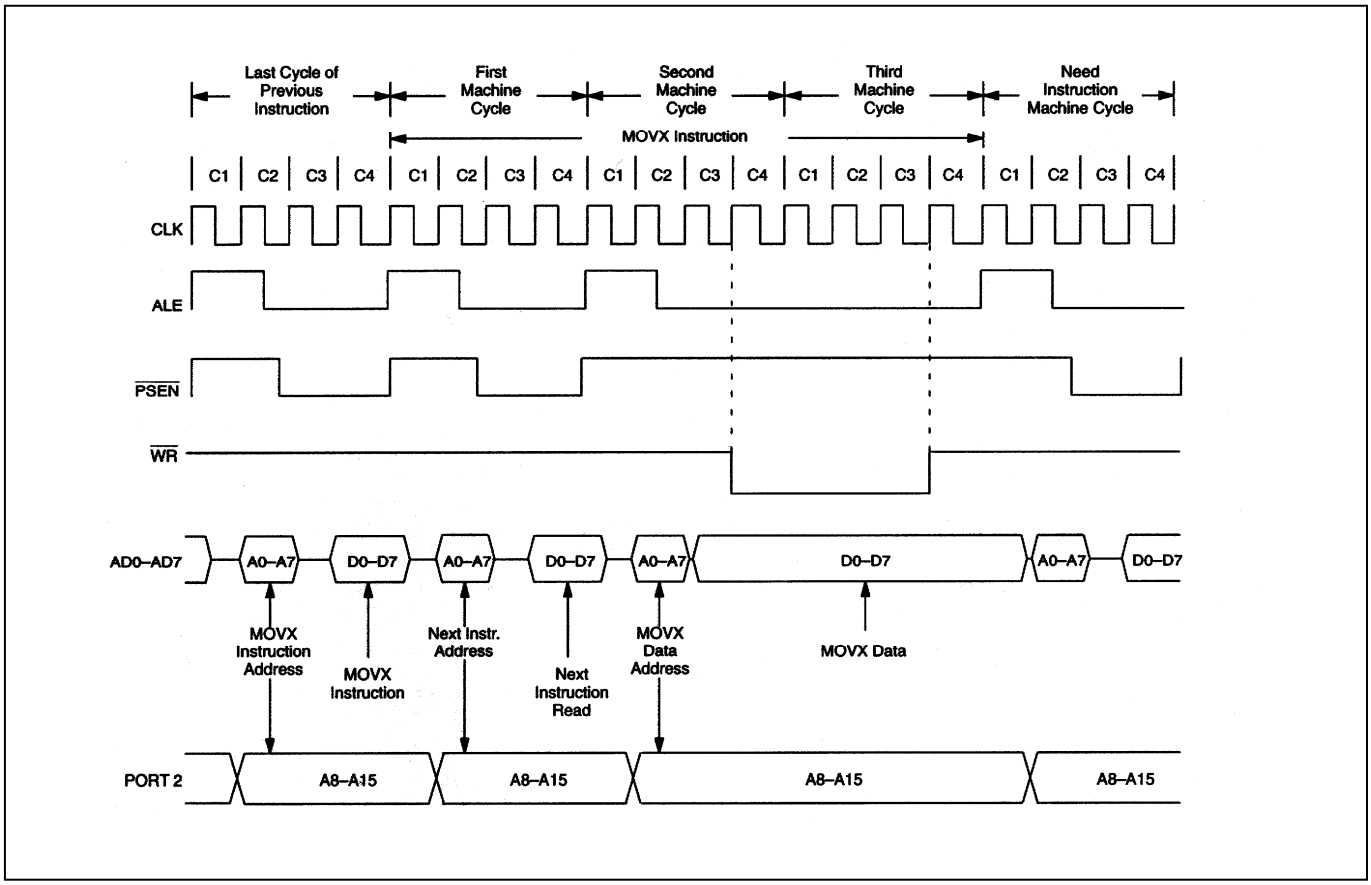
In an effort to remain compatible with the original 8051 family, this device specifies the same parameter as such devices, using the same symbols. For completeness, the following is an explanation of the symbols.

t	Time
A	Address
C	Clock
D	Input data
H	Logic level high
L	Logic level low
I	Instruction
P	$\overline{\text{PSEN}}$
Q	Output data
R	$\overline{\text{RD}}$ signal
V	Valid
W	$\overline{\text{WR}}$ signal
X	No longer a valid logic level
Z	Tri-state

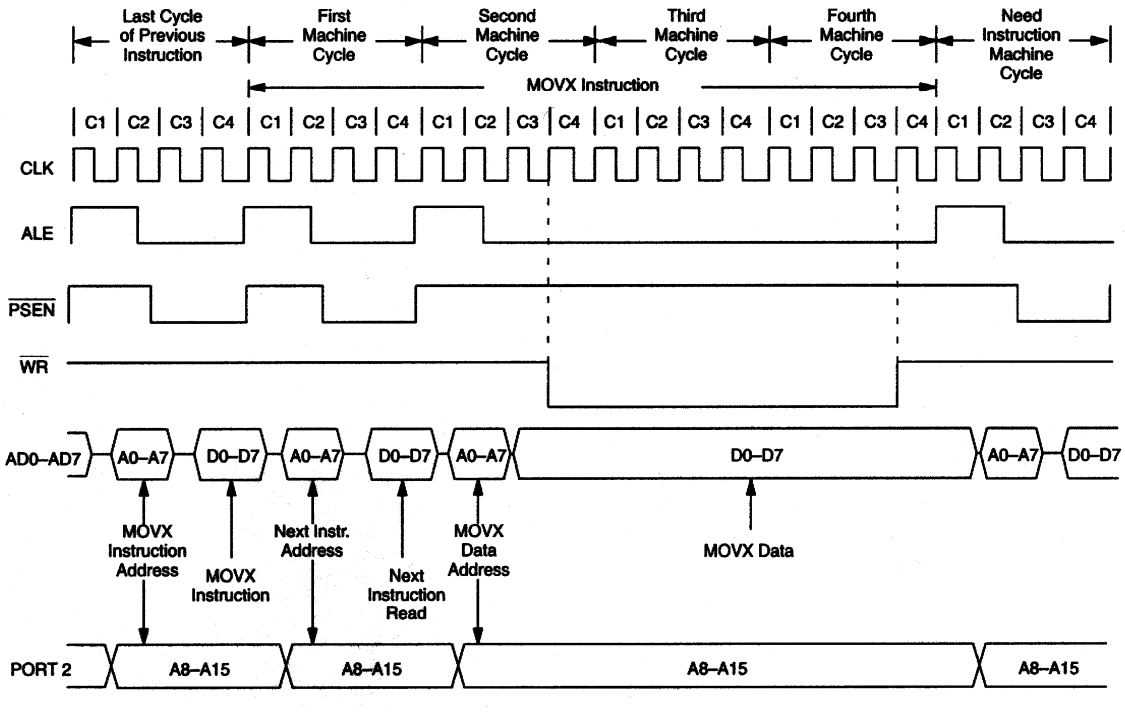
DATA MEMORY WRITE CYCLE



DATA MEMORY WRITE WITH STRETCH = 1

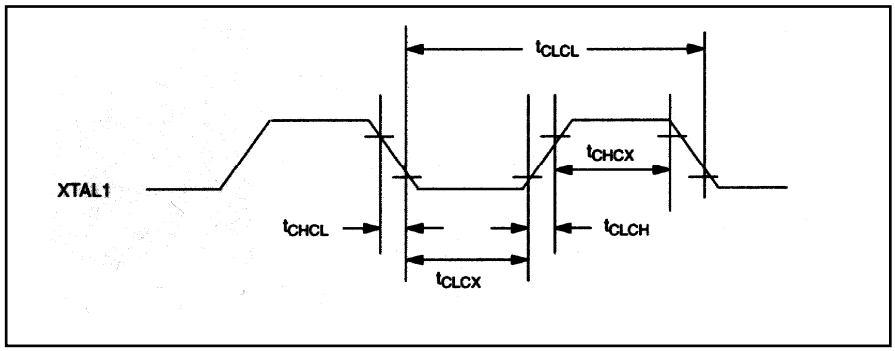


DATA MEMORY WRITE WITH STRETCH = 2



4-CYCLE DATA MEMORY WRITE
STRETCH VALUE = 2

EXTERNAL CLOCK DRIVE



DATA SHEET REVISION SUMMARY (continued)

The following represent the key differences between the 05/22/96 and the 10/21/97 version of the DS80C320 data sheet. Please review this summary carefully.

DS80C320

1. Added note to clarify I_{IL} specification.
2. Added note to clarify AC timing conditions.
3. Corrected erroneous t_{QVXL} label on figure "Serial Port Mode 0 Timing" to read t_{QVXH}.
4. Added note to prevent accidental corruption of Watchdog Timer count while changing counter length.

DS80C323

1. Added note to clarify I_{IL} specification.
2. Remove port 2 from V_{OH1} specification, add port 3.
3. I_{OH} for V_{OH3} specification changed from -3mA to -2mA.
4. Added note to clarify AC timing conditions.

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