# Analog Devices Inc./Maxim Integrated - DS80C320-MNL Datasheet

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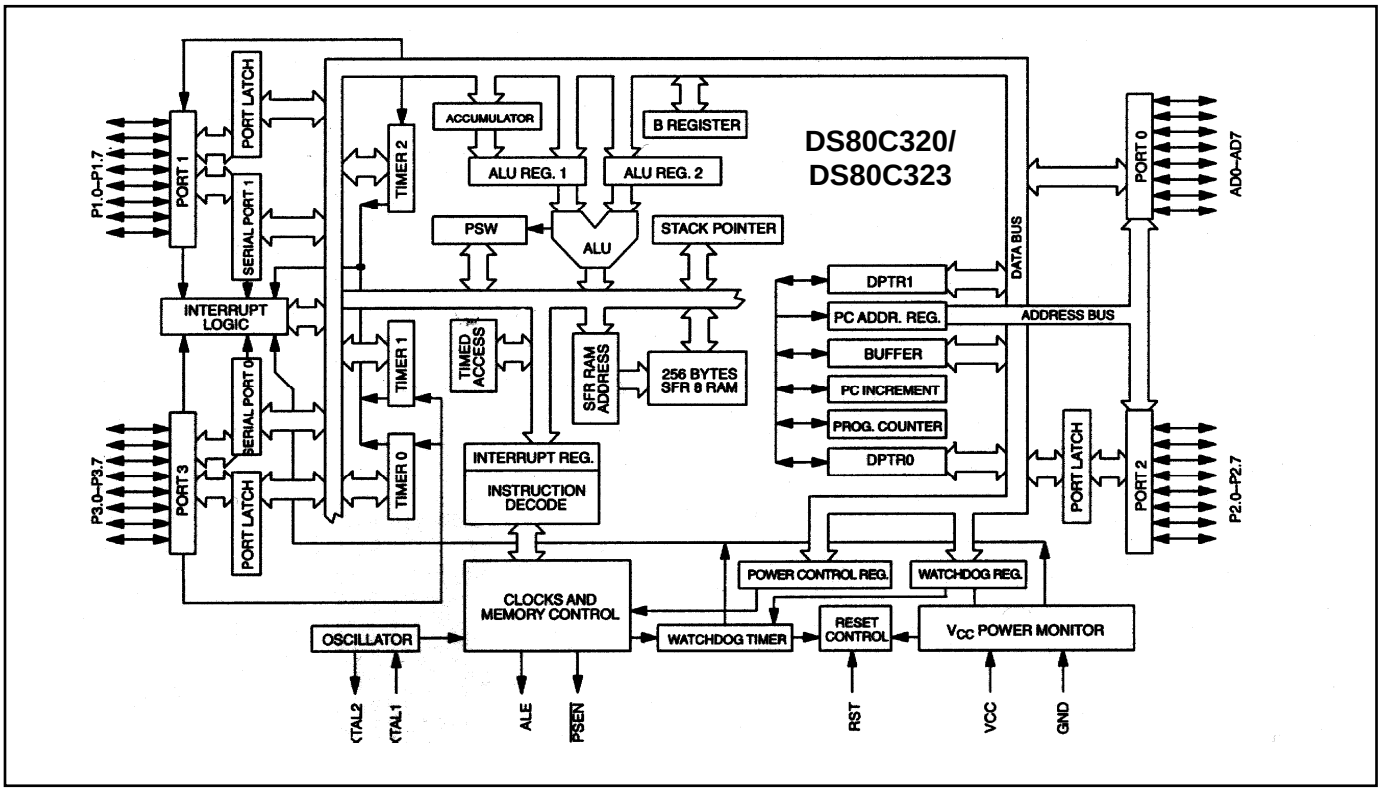
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 33MHz |
| Connectivity | EBI/EMI, SIO, UART/USART |
| Peripherals | Power-Fail Reset, WDT |
| Number of I/O | 32 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 40-DIP (0.600", 15.24mm) |
| Supplier Device Package | 40-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/ds80c320-mnl |

## Figure 1. Block Diagram




## PIN DESCRIPTION

| PIN | | | NAME | FUNCTION |
|---|---|---|---|---|
| DIP | PLCC | TQFP | | |
| 40 | 44 | 38 | $V_{CC}$ | **+5V (+3V for DS80C323)** |
| 20 | 22, 23 | 16, 17 | GND | **Digital Circuit Ground** |
| 9 | 10 | 4 | RST | **Reset Input.** The RST input pin contains a Schmitt voltage input to recognize external active-high reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wired OR external reset sources. An RC is ***not*** required for power-up, as the device provides this function internally. |
| 18 | 20 | 14 | XTAL2 | **Crystal Oscillator Pins.** XTAL1 and XTAL2 provide support for parallel-resonant, AT-cut crystals. XTAL1 acts also as an input in the event that an external clock source is used in place of a crystal. XTAL2 serves as the output of the crystal amplifier. |
| 19 | 21 | 15 | XTAL1 | |
| 29 | 32 | 26 | $\overline{\text{PSEN}}$ | **Program Store-Enable Output, Active Low.** This signal is commonly connected to external ROM memory as a chip enable. $\overline{\text{PSEN}}$ provides an active-low pulse width of 2.25 XTAL1 cycles with a period of four XTAL1 cycles. $\overline{\text{PSEN}}$ is driven high when data memory (RAM) is being accessed through the bus and during a reset condition. |

## 80C32 COMPATIBILITY

The DS80C320/DS80C323 are CMOS 80C32-compatible microcontrollers designed for high performance. In most cases, the devices will drop into an existing 80C32 design to significantly improve the operation. Every effort has been made to keep the devices familiar to 8032 users, yet they have many new features. In general, software written for existing 80C32-based systems will work on the DS80C320 and DS80C323. The exception is critical timing, because the high-speed microcontroller performs its instructions much faster than the original. It may be necessary to use memories with faster access times if the same crystal frequency is used.

*Application Note 57: DS80C320 Memory Interface Timing* is a useful tool to help the embedded system designer select the proper memories for her or his application.

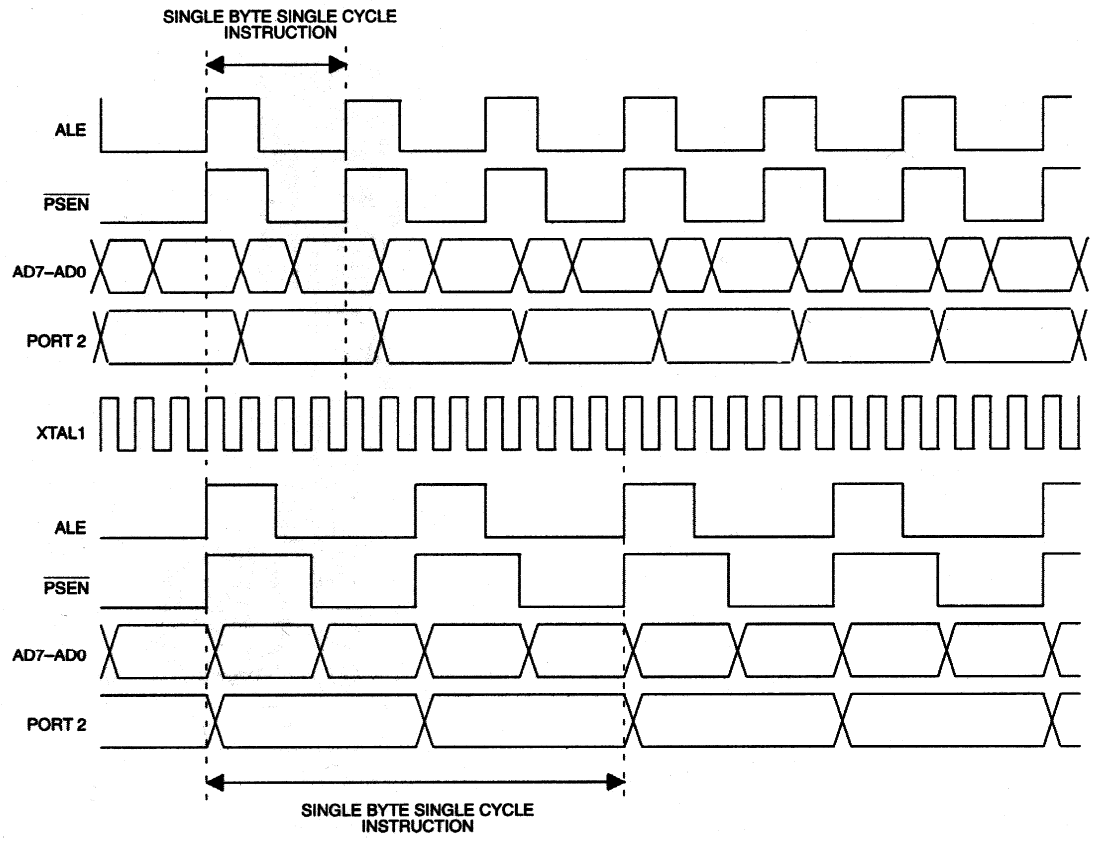
The DS80C320/DS80C323 run the standard 8051 instruction set and is pin compatible with an 80C32 in any of three standard packages. They also provide the same timer/counter resources, full-duplex serial port, 256 bytes of scratchpad RAM, and I/O ports as the standard 80C32. Timers will default to a 12 clock-per-cycle operation to keep timing compatible with original 8051 systems. However, they can be programmed to run at the new 4 clocks per cycle if desired.

New hardware features are accessed using special-function registers that do not overlap with standard 80C32 locations. A summary of these SFRs is provided below.

The DS80C320/DS80C323 address memory in an identical fashion to the standard 80C32. Electrical timing appears different due to the high-speed nature of the product. However, the signals are essentially the same. Detailed timing diagrams are provided in the *Electrical Specifications* section.

This data sheet assumes the user is familiar with the basic features of the standard 80C32. In addition to these standard features, the DS80C320/DS80C323 include many new functions. This data sheet provides only a summary and overview. Detailed descriptions are available in the *High-Speed Microcontroller User's Guide*.

## Figure 2. Comparative Timing of the DS80C320/DS80C323 and 80C32




## HIGH-SPEED OPERATION

The DS80C320/DS80C323 are built around a high-speed, 80C32-compatible core. Higher speed comes not just from increasing the clock frequency but also from a newer, more efficient design.

In this updated core, dummy memory cycles have been eliminated. In a conventional 80C32, machine cycles are generated by dividing the clock frequency by 12. In the DS80C320/DS80C323, the same machine cycle is performed in 4 clocks. Thus the fastest instruction, one machine cycle, is executed three times faster for the same crystal frequency. Note that these are identical instructions. Figure 2 shows a comparison of the timing differences. The majority of instructions will see the full 3-to-1 speed improvement. Some instructions will get between 1.5X and 2.4X improvement. Note that all instructions are faster than the original 80C51. Table 1 shows a summary of the instruction set, including the speed.

The numerical average of all op codes is approximately a 2.5-to-1 speed improvement. Individual programs are affected differently, depending on the actual instructions used. Speed-sensitive applications would make the most use of instructions that are three times faster. However, the sheer number of 3-to-1 improved op codes makes dramatic speed improvements likely for any code. The Dual Data Pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory.

## INSTRUCTION SET SUMMARY

All instructions in the DS80C320/DS80C323 perform the same functions as their 80C32 counterparts. Their effect on bits, flags, and other status functions is identical. However, the timing of each instruction is different. This applies both in absolute and relative number of clocks.

For absolute timing of real-time events, the timing of software loops will need to be calculated using the Table 1. However, counter/timers default to run at the older 12 clocks per increment. Therefore, while software runs at higher speed, timer-based events need no modification to operate as before. Timers can be set to run at 4 clocks per increment cycle to take advantage of higher speed operation.

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture, the “MOVX A, @DPTR” instruction and the “MOV direct, direct” instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS80C320/DS80C323, the MOVX instruction can be done in two machine cycles or eight oscillator cycles, but the “MOV direct, direct” uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times from each other. This is because in most cases, the DS80C320/DS80C323 use one cycle for each byte. The user concerned with precise program timing should examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just four clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV.

## Table 1. Instruction Set Summary

| SYMBOL | FUNCTION |
|---|---|
| A | Accumulator |
| Rn | Register R7 to R0 |
| direct | Internal Register Address |
| @Ri | Internal Register pointed to by R0 or R1 (except MOVX) |
| rel | Two's Complement Offset Byte |

| SYMBOL | FUNCTION |
|---|---|
| bit | direct bit-address |
| #data | 8-bit constant |
| #data 16 | 16-bit constant |
| addr 16 | 16-bit destination address |
| addr 11 | 11-bit destination address |

| INSTRUCTION | BYTE | OSCILLATOR CYCLES | INSTRUCTION | BYTE | OSCILLATOR CYCLES |
|---|---|---|---|---|---|
| **ARITHMATIC INSTRUCTIONS** | | | | | |
| ADD A, Rn | 1 | 4 | INC A | 1 | 4 |
| ADD A, direct | 2 | 8 | INC Rn | 1 | 4 |
| ADD A, @Ri | 1 | 4 | INC direct | 2 | 8 |
| ADD A, #data | 2 | 8 | INC @Ri | 1 | 4 |
| ADDC A, Rn | 1 | 4 | INC DPTR | 1 | 12 |
| ADDC A, direct | 2 | 8 | DEC A | 1 | 4 |
| ADDC A, @Ri | 1 | 4 | DEC Rn | 1 | 4 |
| ADDC A, #data | 2 | 8 | DEC direct | 2 | 8 |
| SUBB A, Rn | 1 | 4 | DEC @Ri | 1 | 4 |
| SUBB A, direct | 2 | 8 | MUL AB | 1 | 20 |
| SUBB A, @Ri | 1 | 4 | DIV AB | 1 | 20 |
| SUBB A, #data | 2 | 8 | DA A | 1 | 4 |
| **LOGICAL INSTRUCTIONS** | | | | | |
| ANL A, Rn | 1 | 4 | XRL A, Rn | 1 | 4 |
| ANL A, direct | 2 | 8 | XRL A, direct | 2 | 8 |
| ANL A, @Ri | 1 | 4 | XRL A, @Ri | 1 | 4 |
| ANL A, #data | 2 | 8 | XRL A, #data | 2 | 8 |
| ANL direct, A | 2 | 8 | XRL direct, A | 2 | 8 |
| ANL direct, #data | 3 | 12 | XRL direct, #data | 3 | 12 |
| ORL A, Rn | 1 | 4 | CLR A | 1 | 4 |
| ORL A, direct | 2 | 8 | CPL A | 1 | 4 |
| ORL A, @Ri | 1 | 4 | RL A | 1 | 4 |
| ORL A, #data | 2 | 8 | RLC A | 1 | 4 |
| ORL direct, A | 2 | 8 | RR A | 1 | 4 |
| ORL direct, #data | 3 | 12 | RRC A | 1 | 4 |

Table 1 shows the speed for each class of instruction. Note that many of the instructions have multiple op codes. There are 255 op codes for 111 instructions. Of the 255 op codes, 159 are three times faster than the original 80C32. While a system that emphasizes those instructions will see the most improvement, the large total number that receive a 3 to 1 improvement assure a dramatic speed increase for any system. The speed improvement summary is provided below.

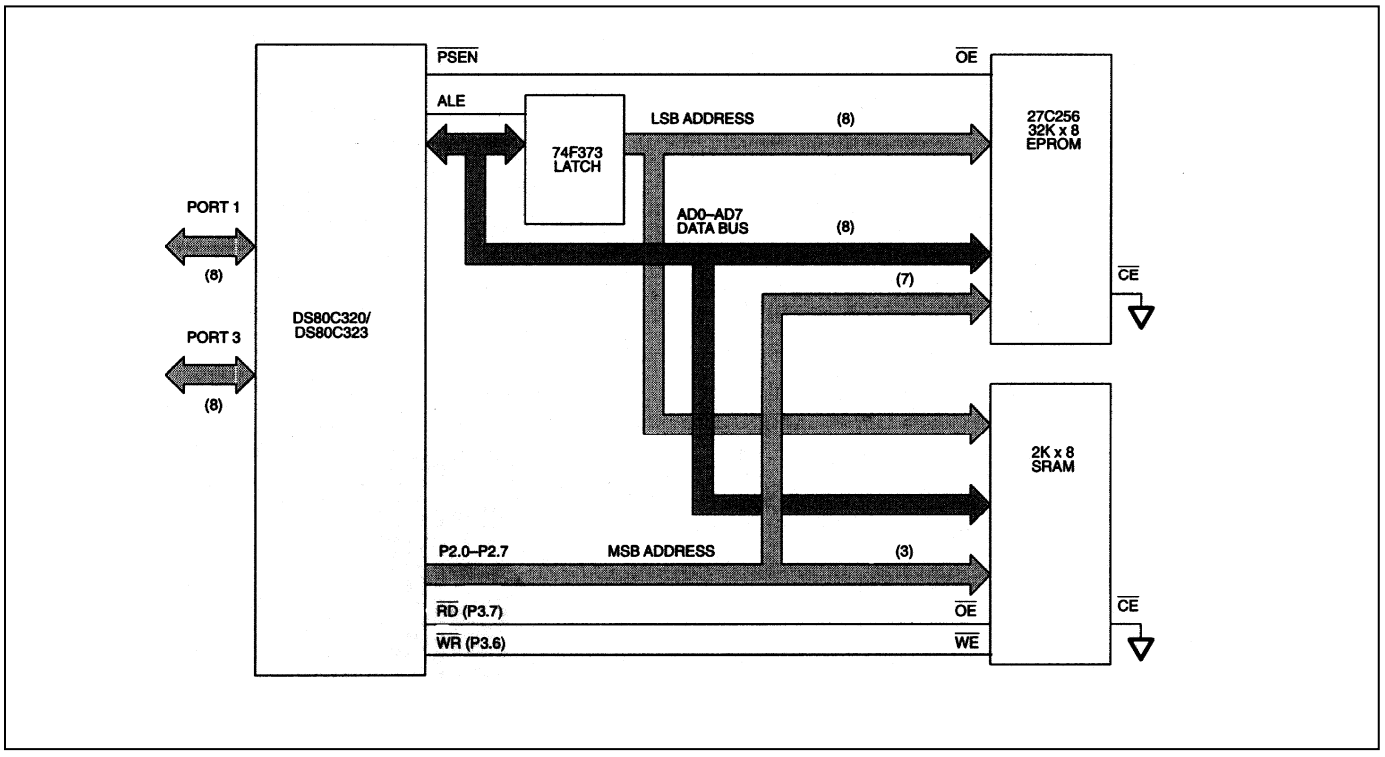
**SPEED ADVANTAGE SUMMARY**

| #OP CODES | SPEED IMPROVEMENT |
|---|---|
| 159 | 3.0 x |
| 51 | 1.5 x |
| 43 | 2.0 x |
| 2 | 2.4 x |
| 255 | Average: 2.5 |

## MEMORY ACCESS

The DS80C320/DS80C323 do not contain on-chip ROM and 256 bytes of scratchpad RAM. Off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. Figure 3 shows a typical memory connection. Timing diagrams are provided in the *Electrical Specifications* section. Program memory (ROM) is accessed at a fixed rate determined by the crystal frequency and the actual instructions. As previously mentioned, an instruction cycle requires 4 clocks. Data memory (RAM) is accessed according to a variable-speed MOVX instruction as described below.

## Figure 3. Typical Memory Connection



## DUAL DATA POINTER

Data memory block moves can be accelerated using the Dual Data Pointer (DPTR). The standard 8032 DPTR is a 16-bit value that is used to address off-chip data RAM or peripherals. In the DS80C320/DS80C323, the standard 16-bit data pointer is called DPTR0 and is located at SFR addresses 82h and 83h. These are the standard locations. The new DPTR is located at SFR 84h and 85h and is called DPTR1. The DPTR Select bit (DPS) chooses the active pointer and is located at the LSB of the SFR location 86h. No other bits in register 86h have any effect and are set to 0. The user switches between data pointers by toggling the LSB of register 86h. The increment (INC) instruction is the fastest way to accomplish this. All DPTR-related instructions use the currently selected DPTR for any activity. Therefore only one instruction is required to switch from a source to a destination address. Using the Dual-Data Pointer saves code from needing to save source and destination addresses when doing a block move. Once loaded, the software simply switches between DPTR and 1. The relevant register locations are as follows.

| | | |
|---|---|---|
| DPL | 82h | Low byte original DPTR |
| DPH | 83h | High byte original DPTR |
| DPL1 | 84h | Low byte new DPTR |
| DPH1 | 85h | High byte new DPTR |
| DPS | 86h | DPTR Select (LSB) |

Sample code listed below illustrates the saving from using the dual DPTR. The example program was original code written for an 8051 and requires a total of 1869 DS80C320/DS80C323 machine cycles. This takes 299µs to execute at 25MHz. The new code using the Dual DPTR requires only 1097 machine cycles taking 175.5µs. The Dual DPTR saves 772 machine cycles or 123.5µs for a 64-byte block move. Since each pass through the loop saves 12 machine cycles when compared to the single DPTR approach, larger blocks gain more efficiency using this feature.

### 64-Byte Block Move without Dual Data Pointer

```
; SH and SL are high and low byte source address.
; DH and DL are high and low byte of destination address.
                                                                    # CYCLES
MOV     R5, #64d            ; NUMBER OF BYTES TO MOVE               2
MOV     DPTR, #SHSL         ; LOAD SOURCE ADDRESS                   3
MOV     R1, #SL             ; SAVE LOW BYTE OF SOURCE               2
MOV     R2, #SH             ; SAVE HIGH BYTE OF SOURCE              2
MOV     R3, #DL             ; SAVE LOW BYTE OF DESTINATION          2
MOV     R4, #DH             ; SAVE HIGH BYTE OF DESTINATION         2

MOVE:
; THIS LOOP IS PERFORMED THE NUMBER OF TIMES LOADED INTO R5, IN THIS EXAMPLE 64

MOVX    A, @DPTR            ; READ SOURCE DATA BYTE                 2
MOV     R1, DPL             ; SAVE NEW SOURCE POINTER               2
MOV     R2, DPH             ;                                       2
MOV     DPL, R3             ; LOAD NEW DESTINATION                  2
MOV     DPH, R4             ;                                       2
MOVX    @DPTR, A            ; WRITE DATA TO DESTINATION             2
INC     DPTR                ; NEXT DESTINATION ADDRESS              3
MOV     R3, DPL             ; SAVE NEW DESTINATION POINTER          2
MOV     R4, DPH             ;                                       2
MOV     DPL, R1             ; GET NEW SOURCE POINTER                2
MOV     DPH, R2             ;                                       2
INC     DPTR                ; NEXT SOURCE ADDRESS                   3
DJNZ    R5, MOVE            ; FINISHED WITH TABLE?                  3
```

a 25MHz crystal frequency. Note that once the counter chain has reached a conclusion, the optional interrupt is generated. Regardless of whether the user enables this interrupt, there are then 512 clocks left until a reset occurs. There are 5 control bits in special function registers that affect the Watchdog Timer and two status flags that report to the user. The Reset Watchdog Timer bit (WDCON.0) should be asserted prior to modifying the Watchdog Timer Mode Select bits (WD1, WD0) to avoid corruption of the watchdog count.

WDIF (WDCON.3) is the interrupt flag that is set when there are 512 clocks remaining until a reset occurs. WTRF (WDCON.2) is the flag that is set when a Watchdog reset has occurred. This allows the application software to determine the source of a reset.

Setting the EWT (WDCON.1) bit enables the Watchdog Timer. The bit is protected by timed access. Setting the RWT (WDCON.0) bit restarts the Watchdog Timer for another full interval. Application software must set this bit prior to the timeout. As mentioned previously, WD1 and 0 (CKCON .7 and 6) select the timeout. Finally, the Watchdog Interrupt is enabled using EWDI (EIE.4).

## INTERRUPTS

The DS80C320/DS80C323 provide 13 sources of interrupt with three priority levels. The Power-fail Interrupt (PFI), if enabled, always has the highest priority. There are two remaining user-selectable priorities: high and low. If two interrupts that have the same priority occur simultaneously, the natural precedence given in Table 4 determines which is acted upon. Except for the PFI, all interrupts that are new to the 8051 family have a lower natural priority than the originals.

**Table 4. Interrupt Priority**

| NAME | FUNCTION | VECTOR | NATURAL PRIORITY | OLD/NEW |
|---|---|---|---|---|
| PFI | Power-Fail Interrupt | 33h | 1 | New |
| $\overline{\text{INT0}}$ | External Interrupt 0 | 03h | 2 | Old |
| TF0 | Timer 0 | 0Bh | 3 | Old |
| $\overline{\text{INT1}}$ | External Interrupt 1 | 13h | 4 | Old |
| TF1 | Timer 1 | 1Bh | 5 | Old |
| SCON0 | TI0 or RI0 from Serial Port 0 | 23h | 6 | Old |
| TF2 | Timer 2 | 2Bh | 7 | Old |
| SCON1 | TI1 or RI1 from Serial Port 1 | 3Bh | 8 | New |
| INT2 | External Interrupt 2 | 43h | 9 | New |
| $\overline{\text{INT3}}$ | External Interrupt 3 | 4Bh | 10 | New |
| INT4 | External Interrupt 4 | 53h | 11 | New |
| $\overline{\text{INT5}}$ | External Interrupt 5 | 5Bh | 12 | New |
| WDTI | Watchdog Timeout Interrupt | 63h | 13 | New |

## POWER MANAGEMENT

The DS80C320/DS80C323 provide the standard Idle and power-down (Stop) modes that are available on the standard 80C32. However, the device has enhancements that make these modes more useful, and allow more power saving.

The Idle mode is invoked by setting the LSB of the Power Control register (PCON to 87h). Idle will leave internal clocks, serial port and timer running. No memory access will be performed so power is dramatically reduced. Since clocks are running, the Idle power consumption is related to crystal frequency. It should be approximately one-half the operational power. The CPU can exit the Idle state with any interrupt or a reset.

The power-down or Stop mode is invoked by setting the PCON.1 bit. Stop mode is a lower power state than Idle since it turns off all internal clocking. The $I_{CC}$ of a standard Stop mode is approximately 1 µA but is specified in the *Electrical Specifications* section. The CPU will exit Stop mode from an external interrupt or a reset condition.

Note that internally generated interrupts (timer, serial port, watchdog) are not useful in Idle or Stop since they require clocking activity.

## IDLE MODE ENHANCEMENTS

A simple enhancement to Idle mode makes it substantially more useful. The innovation involves not the Idle mode itself, but the watchdog timer. As mentioned above, the Watchdog Timer provides an optional interrupt capability. This interrupt can provide a periodic interval timer to bring the DS80C320/DS80C323 out of Idle mode. This can be useful even if the Watchdog is not normally used. By enabling the Watchdog Timer and its interrupt prior to invoking Idle, a user can periodically come out of Idle perform an operation, then return to Idle until the next operation. This will lower the overall power consumption. When using the Watchdog Interrupt to cancel the Idle state, make sure to restart the Watchdog Timer or it will cause a reset.

## STOP MODE ENHANCEMENTS

The DS80C320/DS80C323 provide two enhancements to the Stop mode. As documented above, the device provides a bandgap reference to determine Power-fail Interrupt and Reset thresholds. The default state is that the bandgap reference is off when Stop mode is invoked. This allows the extremely low power state mentioned above. A user can optionally choose to have the bandgap enabled during Stop mode. This means that PFI and power-fail reset will be activated and are valid means for leaving Stop mode.

In Stop mode with the bandgap on, $I_{CC}$ will be approximately 50µA compared with 1µA with the bandgap off. If a user does not require a Power-fail Reset or Interrupt while in Stop mode, the bandgap can remain turned off. Note that only the most power sensitive applications should turn off the bandgap, as this results in an uncontrolled power-down condition.

The control of the bandgap reference is located in the Extended Interrupt Flag register (EXIF to 91h). Setting BGS (EXIF.0) to a 1 will leave the bandgap reference enabled during Stop mode. The default or reset condition is with the bit at a logic 0. This results in the bandgap being turned off during Stop mode. Note that this bit has no control of the reference during full power or Idle modes. Be aware that the DS80C320 and DS80C323 require that the reset watchdog timer bit (RWT;WDCON.0) be set

immediately preceding the setting of the Stop bit to guarantee a correct power-on delay when exiting Stop mode.

The second feature allows an additional power saving option. This is the ability to start instantly when exiting Stop mode. It is accomplished using an internal ring oscillator that can be used when exiting Stop mode in response to an interrupt. The benefit of the ring oscillator is as follows.

Using Stop mode turns off the crystal oscillator and all internal clocks to save power. This requires that the oscillator be restarted when exiting Stop mode. Actual start-up time is crystal dependent, but is normally at least 4ms. A common recommendation is 10ms. In an application that will wakeup, perform a short operation, then return to sleep, the crystal startup can be longer than the real transaction. However, the ring oscillator will start instantly. The user can perform a simple operation and return to sleep before the crystal has even stabilized. If the ring is used to start and the processor remains running, hardware will automatically switch to the crystal once a power-on reset interval (65,536 clocks) has expired. This value is used to guarantee stability even though power is not being cycled.

If the user returns to Stop mode prior to switching of crystal, then all clocks will be turned off again. The ring oscillator runs at approximately 3MHz (1.5MHz at 3V) but will not be a precision value. No real-time precision operations (including serial communication) should be conducted during this ring period. Figure 4 shows how the operation would compare when using the ring, and when starting up normally. The default state is to come out of Stop mode without using the ring oscillator.

This function is controlled using the RGSL - Ring Select bit at EXIF.1 (EXIF to 91h). When EXIF.1 is set, the ring oscillator will be used to come out of Stop mode quickly. As mentioned above, the processor will automatically switch from the ring (if enabled) to the crystal after a delay of 65,536 crystal clocks. For a 3.57MHz crystal, this is approximately 18ms. The processor sets a flag called RGMD - Ring Mode to tell software that the ring is being used. This bit at EXIF.2 will be logic 1 when the ring is in use. No serial communication or precision timing should be attempted while this bit is set, since the operating frequency is not precise.

## Figure 4. Ring Oscillator Startup

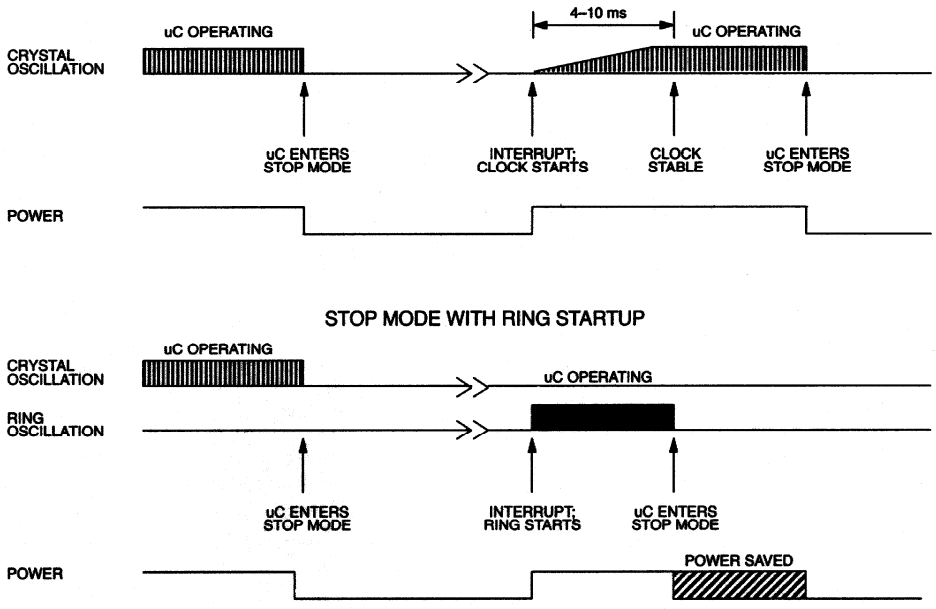



DIAGRAM ASSUMES THAT THE OPERATION FOLLOWING STOP REQUIRES LESS THAN 18ms COMPLETE.

## TIMED ACCESS PROTECTION

Selected SFR bits are critical to operation, making it desirable to protect against an accidental write operation. The Timed Access procedure prevents an errant CPU from accidentally altering a bit that would cause difficulty. The Timed Access procedure requires that the write of a protected bit be preceded by the following instructions:

```
MOV     0C7h, #0AAh
MOV     0C7h, #55h
```

By writing an AAh followed by a 55h to the Timed Access register (location C7h), the hardware opens a three-cycle window that allows software to modify one of the protected bits. If the instruction that seeks to modify the protected bit is not immediately proceeded by these instructions, the write will not take effect. The protected bits are:

| | |
|---|---|
| EXIF.0 | BGS Bandgap Select |
| WDCON.6 | POR Power-on Reset flag |
| WDCON.1 | EWT Enable Watchdog |
| WDCON.0 | RWT Reset Watchdog |
| WDCON.3 | WDIF Watchdog Interrupt Flag |

## SPECIAL-FUNCTION REGISTERS

Most special features of the DS80C320/DS80C323 or 80C32 are controlled by bits in the SFRs, allowing the devices to add many features but use the same instruction set. When writing software to use a new feature, the SFR must be defined to an assembler or compiler using an equate statement. This is the only change needed to access the new function. The DS80C320/DS80C323 duplicate the SFRs that are contained in the standard 80C32. Table 5 shows the register addresses and bit locations. Many are standard 80C32 registers. The *High-Speed Microcontroller User's Guide* describes all SFRs.

### Table 5. Special-Function Register Locations

| REGISTER | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | ADDRESS |
|---|---|---|---|---|---|---|---|---|---|
| SP | | | | | | | | | 81h |
| DPL | | | | | | | | | 82h |
| DPH | | | | | | | | | 83h |
| **DPL1** | | | | | | | | | 84h |
| **DPH1** | | | | | | | | | 85h |
| **DPS** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **SEL** | 86h |
| PCON | SMOD_0 | **SMOD0** | — | — | GF1 | GF0 | STOP | IDLE | 87h |
| TCON | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | 88h |
| TMOD | GATE | C/$\overline{T}$ | M1 | M0 | GATE | C/$\overline{T}$ | M1 | M0 | 89h |
| TL0 | | | | | | | | | 8Ah |
| TL1 | | | | | | | | | 8Bh |
| TH0 | | | | | | | | | 8Ch |
| TH1 | | | | | | | | | 8Dh |
| **CKCON** | **WD1** | **WD0** | **T2M** | **T1M** | **T0M** | **MD2** | **MD1** | **MD0** | 8Eh |
| P1 | P1.7 | P1.6 | P1.5 | P1.4 | P1.3 | P1.2 | P1.1 | P1.0 | 90h |
| **EXIF** | **IE5** | **IE4** | **IE3** | **IE2** | — | **RGMD** | **RGSL** | **BGS** | 91h |
| SCON0 | SM0/FE_0 | SM1_0 | SM2_0 | REN_0 | TB8_0 | RB8_0 | TI_0 | RI_0 | 98h |
| SBUF0 | | | | | | | | | 99h |
| P2 | P2.0 | P2.6 | P2.5 | P2.4 | P2.3 | P2.2 | P2.1 | P2.0 | A0h |
| IE | EA | ES1 | ET2 | ES0 | ET1 | EX1 | ET0 | EX0 | A8h |
| SADDR0 | | | | | | | | | A9h |
| SADDR1 | | | | | | | | | AAh |
| P3 | P3.7 | P3.6 | P3.5 | P3.4 | P3.3 | P3.2 | P3.1 | P3.0 | B0h |
| IP | — | PS1 | PT2 | PS0 | PT1 | PX1 | PT0 | PX0 | B8h |
| SADEN0 | | | | | | | | | B9h |
| SADEN1 | | | | | | | | | BAh |
| **SCON1** | **SM0/FE_0** | **SM1_0** | **SM2_0** | **REN_0** | **TB8_0** | **RB8_0** | **TI_0** | **RI_0** | C0h |
| **SBUF1** | | | | | | | | | C1h |
| STATUS | PIP | HIP | LIP | 1 | 1 | 1 | 1 | 1 | C5h |
| **TA** | | | | | | | | | C7h |
| T2CON | TF2 | EXF2 | RCLK | TCLK | EXEN2 | TR2 | C/$\overline{T2}$ | CP/$\overline{RL2}$ | C8h |
| T2MOD | — | — | — | — | — | — | T2OE | DCEN | C9h |
| RCAP2L | | | | | | | | | CAh |
| RCAP2H | | | | | | | | | CBh |
| TL2 | | | | | | | | | CCh |
| TH2 | | | | | | | | | CDh |
| PSW | CY | AC | F0 | RS1 | RS0 | OV | FL | P | D0h |
| **WDCON** | **SMOD_1** | **POR** | **EPFI** | **PFI** | **WDIF** | **WTRF** | **EWT** | **RWT** | D8h |
| ACC | | | | | | | | | E0h |
| **EIE** | — | — | — | **EWDI** | **EX5** | **EX4** | **EX3** | **EX2** | E8h |
| B | | | | | | | | | F0h |
| **EIP** | — | — | — | **PWDI** | **PX5** | **PX4** | **PX3** | **PX2** | F8h |

# ELECTRICAL SPECIFICATIONS

## ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to ($V_{CC}$ + 0.5V)
Voltage Range on $V_{CC}$ Relative to Ground……..-0.3V to +6.0V
Operating Temperature Range……-40°C to +85°C
Storage Temperature Range……..-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020 Specification

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

## DC ELECTRICAL CHARACTERISTICS—DS80C320

($V_{CC}$ = 4.5V to 5.5V, $T_A$ = -40°C to +85°C.)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Operating Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Power-Fail Warning Voltage | $V_{PFW}$ | 4.25 | 4.38 | 4.55 | V | 1 |
| Minimum Operating Voltage | $V_{RST}$ | 4.0 | 4.1 | 4.25 | V | 1, 12 |
| Supply Current Active Mode at 25MHz | $I_{CC}$ | | 30 | 45 | mA | 2 |
| Supply Current Idle Mode at 25MHz | $I_{IDLE}$ | | 15 | 25 | mA | 3 |
| Supply Current Active Mode at 33MHz | $I_{CC}$ | | 35 | | mA | 2 |
| Supply Current Idle Mode at 33MHz | $I_{IDLE}$ | | 20 | | mA | 3 |
| Supply Current Stop Mode, Bandgap Reference Disabled | $I_{STOP}$ | | 0.01 | 1 | µA | 4 |
| Supply Current Stop Mode, Bandgap Reference Enabled | $I_{SPBG}$ | | 50 | 80 | µA | 4, 10 |
| Input Low Level | $V_{IL}$ | -0.3 | | +0.8 | V | 1 |
| Input High Level (Except XTAL1 and RST) | $V_{IH1}$ | 2.0 | | $V_{CC}$ + 0.3 | V | 1 |
| Input High Level XTAL1 and RST | $V_{IH2}$ | 3.5 | | $V_{CC}$ + 0.3 | V | 1 |
| Output-Low Voltage Ports 1, 3 at $I_{OL}$ = 1.6mA | $V_{OL1}$ | | | 0.45 | V | 1 |
| Output-Low Voltage Ports 0, 2, ALE, $\overline{PSEN}$ at $I_{OL}$ = 3.2mA | $V_{OL2}$ | | | 0.45 | V | 1, 5 |
| Output-High Voltage Ports 1, 3, ALE, $\overline{PSEN}$ at $I_{OH}$ = -50µA | $V_{OH1}$ | 2.4 | | | V | 1, 6 |
| Output High Voltage Ports 1, 3 at $I_{OH}$ = -1.5mA | $V_{OH2}$ | 2.4 | | | V | 1, 7 |
| Output-High Voltage Ports 0, 2, ALE, $\overline{PSEN}$ at $I_{OH}$ = -8mA | $V_{OH3}$ | 2.4 | | | V | 1, 5 |
| Input Low Current Ports 1, 3 at 0.45V | $I_{IL}$ | | | -55 | µA | 11 |
| Transition Current from 1 to 0 Ports 1, 3 at 2V | $I_{TL}$ | | | -650 | µA | 8 |
| Input Leakage Port 0, Bus Mode | $I_L$ | -300 | | +300 | µA | 9 |
| RST Pulldown Resistance | $R_{RST}$ | 50 | | 170 | kΩ | |

## MOVX CHARACTERISTICS—DS80C323

| PARAMETER | SYMBOL | VARIABLE CLOCK | | UNITS | STRETCH |
|---|---|---|---|---|---|
| | | MIN | MAX | | |
| $\overline{RD}$ Pulse Width | $t_{RLRH}$ | $2t_{CLCL}$-11 | | ns | $t_{MCS}$=0 |
| | | $t_{MCS}$-11 | | | $t_{MCS}$>0 |
| $\overline{WR}$ Pulse Width | $t_{WLWH}$ | $2t_{CLCL}$-11 | | ns | $t_{MCS}$=0 |
| | | $t_{MCS}$-11 | | | $t_{MCS}$>0 |
| $\overline{RD}$ Low to Valid Data In | $t_{RLDV}$ | | $2t_{CLCL}$-32 | ns | $t_{MCS}$=0 |
| | | | $t_{MCS}$-36 | | $t_{MCS}$>0 |
| Data Hold After Read | $t_{RHDX}$ | 0 | | ns | |
| Data Float After Read | $t_{RHDZ}$ | | $t_{CLCL}$-5 | ns | $t_{MCS}$=0 |
| | | | $2t_{CLCL}$-7 | | $t_{MCS}$>0 |
| ALE Low to Valid Data In | $t_{LLDV}$ | | $2.5t_{CLCL}$-43 | ns | $t_{MCS}$=0 |
| | | | $1.5t_{CLCL}$-45+$t_{MCS}$ | | $t_{MCS}$>0 |
| Port 0 Address to Valid Data In | $t_{AVDV1}$ | | $3t_{CLCL}$-40 | ns | $t_{MCS}$=0 |
| | | | $2t_{CLCL}$-42+$t_{MCS}$ | | $t_{MCS}$>0 |
| Port 2 Address to Valid Data In | $t_{AVDV2}$ | | $3.5t_{CLCL}$-58 | ns | $t_{MCS}$=0 |
| | | | $2.5t_{CLCL}$-59+$t_{MCS}$ | | $t_{MCS}$>0 |
| ALE Low to $\overline{RD}$ or $\overline{WR}$ Low | $t_{LLWL}$ | $0.5t_{CLCL}$-18 | $0.5t_{CLCL}$+7 | ns | $t_{MCS}$=0 |
| | | $1.5t_{CLCL}$-11 | $1.5t_{CLCL}$+8 | | $t_{MCS}$>0 |
| Port 0 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low | $t_{AVWL1}$ | $t_{CLCL}$-10 | | ns | $t_{MCS}$=0 |
| | | $2t_{CLCL}$-10 | | | $t_{MCS}$>0 |
| Port 2 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low | $t_{AVWL2}$ | $1.5t_{CLCL}$-27 | | ns | $t_{MCS}$=0 |
| | | $2.5t_{CLCL}$-25 | | | $t_{MCS}$>0 |
| Data Valid to $\overline{WR}$ Transition | $t_{QVWX}$ | -14 | | ns | $t_{MCS}$=0 |
| | | $t_{CLCL}$-13 | | | $t_{MCS}$>0 |
| Data Hold After Write | $t_{WHQX}$ | $t_{CLCL}$-15 | | ns | $t_{MCS}$=0 |
| | | $2t_{CLCL}$-13 | | | $t_{MCS}$>0 |
| $\overline{RD}$ Low to Address Float | $t_{RLAZ}$ | | (Note 5) | ns | |
| $\overline{RD}$ or $\overline{WR}$ High to ALE High | $t_{WHLH}$ | -1 | 14 | ns | $t_{MCS}$=0 |
| | | $t_{CLCL}$-5 | $t_{CLCL}$+16 | | $t_{MCS}$>0 |

**Note:** $t_{MCS}$ is a time period related to the Stretch memory cycle selection. The following table shows the value of $t_{MCS}$ for each Stretch selection.

| M2 | M1 | M0 | MOVX CYCLES | $t_{MCS}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 2 machine cycles | 0 |
| 0 | 0 | 1 | 3 machine cycles (default) | 4 $t_{CLCL}$ |
| 0 | 1 | 0 | 4 machine cycles | 8 $t_{CLCL}$ |
| 0 | 1 | 1 | 5 machine cycles | 12 $t_{CLCL}$ |
| 1 | 0 | 0 | 6 machine cycles | 16 $t_{CLCL}$ |
| 1 | 0 | 1 | 7 machine cycles | 20 $t_{CLCL}$ |
| 1 | 1 | 0 | 8 machine cycles | 24 $t_{CLCL}$ |
| 1 | 1 | 1 | 9 machine cycles | 28 $t_{CLCL}$ |

## EXTERNAL CLOCK CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Clock High Time | $t_{CHCX}$ | 10 | | | ns |
| Clock Low Time | $t_{CLCX}$ | 10 | | | ns |
| Clock Rise Time | $t_{CLCH}$ | | | 5 | ns |
| Clock Fall Time | $t_{CHCL}$ | | | 5 | ns |

## SERIAL PORT MODE 0 TIMING CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Serial Port Clock Cycle Time | $t_{XLXL}$ | SM2 = 0; 12 clocks per cycle | | $12t_{CLCL}$ | | ns |
| | | SM2 = 1; 4 clocks per cycle | | $4t_{CLCL}$ | | |
| Output Data Setup to Clock Rising Edge | $t_{QVXH}$ | SM2 = 0 12 clocks per cycle | | $10t_{CLCL}$ | | ns |
| | | SM2 = 1; 4 clocks per cycle | | $3t_{CLCL}$ | | |
| Output Data Hold from Clock Rising | $t_{XHQX}$ | SM2 = 0 12 clocks per cycle | | $2t_{CLCL}$ | | ns |
| | | SM2 = 1; 4 clocks per cycle | | $t_{CLCL}$ | | |
| Input Data Hold After Clock Rising | $t_{XHDX}$ | SM2 = 0; 12 clocks per cycle | | $t_{CLCL}$ | | ns |
| | | SM2 = 1; 4 clocks per cycle | | $t_{CLCL}$ | | |
| Clock Rising Edge to Input Data Valid | $t_{XHDV}$ | SM2 = 0; 12 clocks per cycle | | $11t_{CLCL}$ | | ns |
| | | SM2 = 1 4 clocks per cycle | | $2t_{CLCL}$ | | |

## EXPLANATION OF AC SYMBOLS

In an effort to remain compatible with the original 8051 family, this device specifies the same parameter as such devices, using the same symbols. For completeness, the following is an explanation of the symbols.

| | |
|---|---|
| t | Time |
| A | Address |
| C | Clock |
| D | Input data |
| H | Logic level high |
| L | Logic level low |
| I | Instruction |
| P | $\overline{\text{PSEN}}$ |
| Q | Output data |
| R | $\overline{\text{RD}}$ signal |
| V | Valid |
| W | $\overline{\text{WR}}$ signal |
| X | No longer a valid logic level |
| Z | Tri-state |

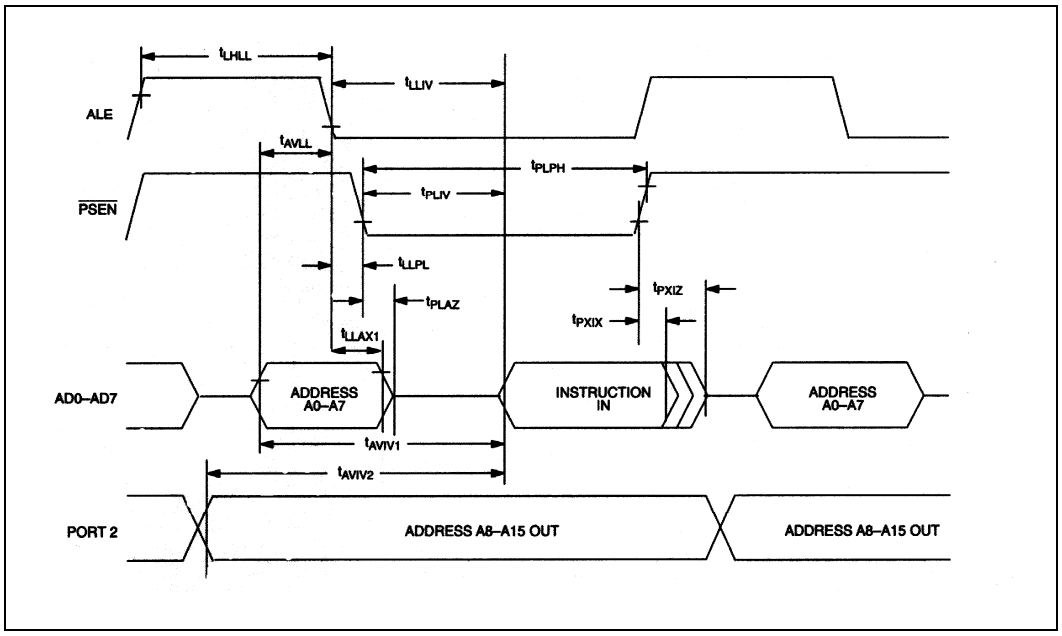
## POWER-CYCLE TIMING CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Crystal Startup Time | $t_{CSU}$ | | 1.8 | | ms | 1 |
| Power-On Reset Delay | $t_{POR}$ | | | 65,536 | $t_{CLCL}$ | 2 |

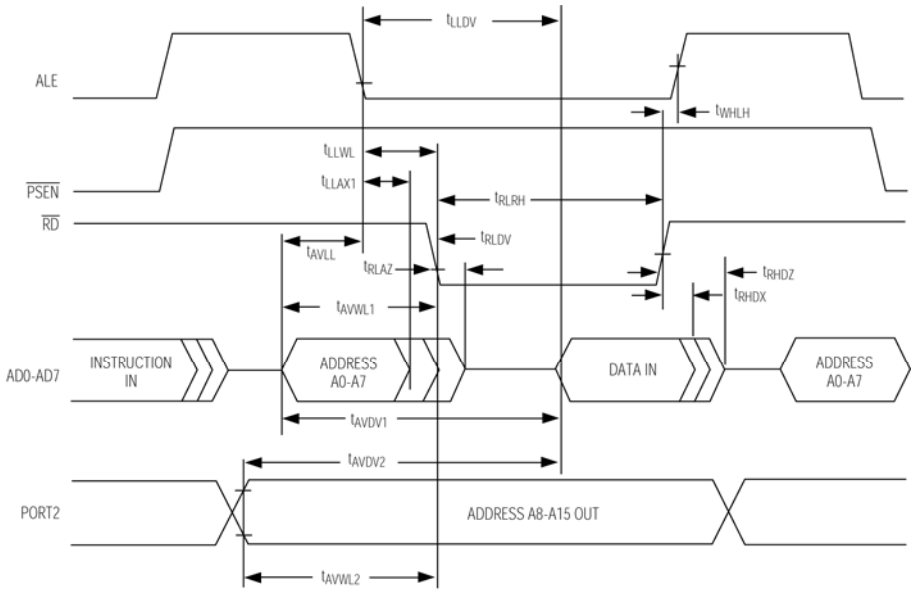
## NOTES FOR POWER CYCLE TIMING CHARACTERISTICS

1. Startup time for crystals varies with load capacitance and manufacturer. Time shown is for an 11.0592MHz crystal manufactured by Fox crystal.
2. Reset delay is a synchronous counter of crystal oscillations after crystal startup. Counting begins when the level on the XTAL1 input meets the $V_{IH2}$ criteria. At 25MHz, this time is 2.62ms.

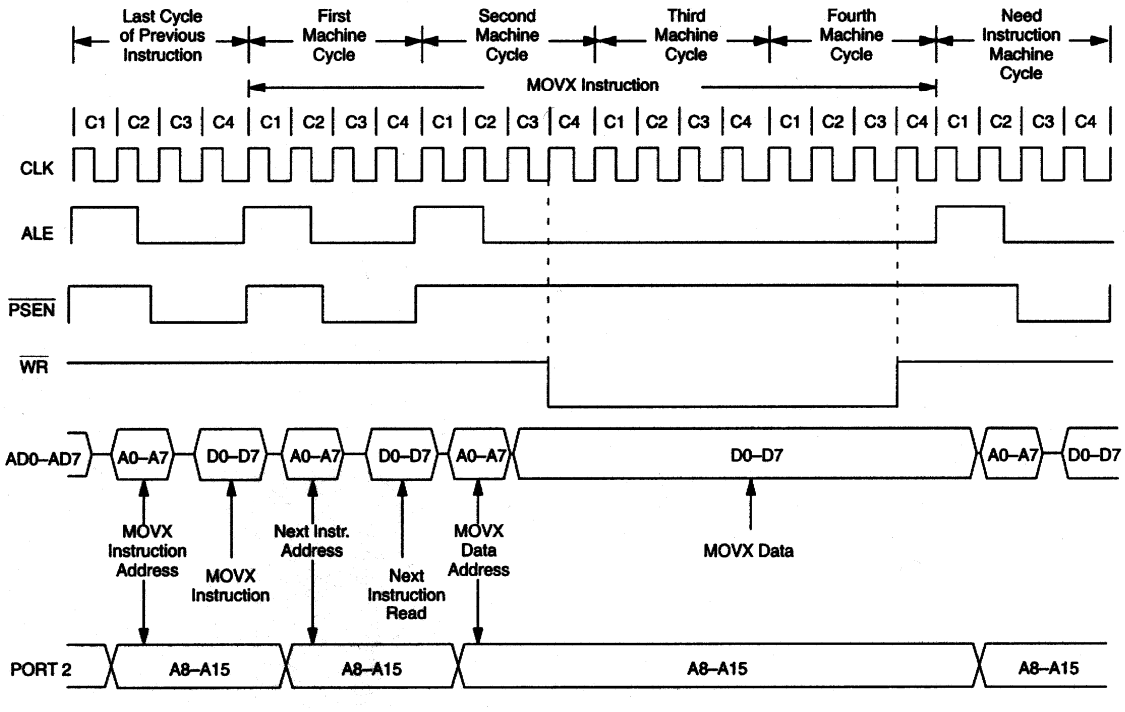
## PROGRAM MEMORY READ CYCLE



## DATA MEMORY READ CYCLE

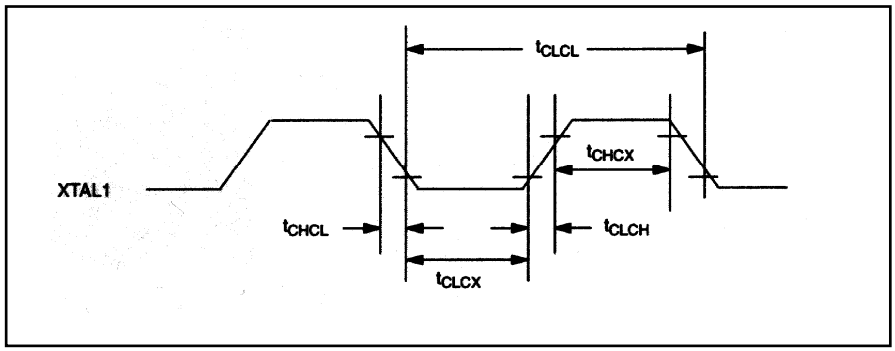


## DATA MEMORY WRITE WITH STRETCH = 2




4-CYCLE DATA MEMORY WRITE
STRETCH VALUE = 2

## EXTERNAL CLOCK DRIVE



## PACKAGE INFORMATION

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 44 TQFP | C44+2 | **21-0293** |
| 44 MQFP | M44+10 | **21-0269** |
| 44 MQFP | M44+5 | **21-0826** |
| 40 PDIP | P40+1 | **21-0044** |
| 44 PLCC | Q44+1 | **21-0049** |

# DATA SHEET REVISION SUMMARY

***The following represent the key differences between the 101006 and 070505 version of the DS80C320/DS80C323 data sheet. Please review this summary carefully.***

1. Deleted DS80C323-MND from Ordering Information table (page 2). Device was never manufactured.

***The following represent the key differences between the 070505 and 051804 version of the DS80C320/DS80C323 data sheet. Please review this summary carefully.***

2. Added Pb-free/RoHS-compliant part numbers to Ordering Information table.
3. Deleted the "A" from the IPC/JEDEC J-STD-020 specification in the Absolute Maximum Ratings.

***The following represent the key differences between the 051804 and the 112299 version of the DS80C320/DS80C323 data sheet. Please review this summary carefully.***

1. Removed "Preliminary" status as a result of final characterization.
2. Added industrial temperature DS80C323 devices to ordering information.
3. Updated soldering temperature specification to reflect JEDEC standards.
4. Updated the following DS80C323 AC timing parameters with final characterization data: $t_{LHLL}$, $t_{LLAX1}$, $t_{LLAX2}$, $t_{LLAX2}$, $t_{LLIV}$, $t_{LLPL}$, $t_{PLIV}$, $t_{AVIV1}$, $t_{RLDV}$, $t_{RHDZ}$, $t_{LLDV}$, $t_{AVDV1}$, $t_{AVDV2}$, $t_{LLWL}$, $t_{AVWL1}$, $t_{AVWL2}$, $t_{QVWX}$, $t_{WHQX}$, $t_{WHLH}$.
5. Updated the following DS80C320 AC timing parameters with final characterization data: $t_{WHQX}$, $t_{LHLL}$, $t_{LLAX2}$, tLLDV, $t_{AVDV1}$, $t_{LLWL}$, $t_{AVWL1}$, $t_{AVWL2}$.
6. Added note advising the need to reset watchdog timer before setting the Stop bit.
7. Added note clarifying drive strength of P0, P2, ALE, $\overline{PSEN}$.
8. Obsoleted DS80C320 25MHz AC timing tables; merged into 33MHz AC timing tables.
9. Corrected Serial Port Mode 0 Timing diagrams to show correct order of D6, D7.

***The following represent the key differences between the 041896 and the 052799 version of the DS80C320 data sheet. Please review this summary carefully.***

1. Corrected $V_{CC}$ pin description to show DS80C323 operation at +3V.
2. Corrected Timed Access description to show three-cycle window.
3. Modified absolute Maximum Ratings for any pin relative to around, $V_{CC}$ relative to ground.
4. Changed minimum oscillator frequency to 1MHz when using external crystal.
5. Clarified that $t_{POR}$ begins when XTAL1 reaches $V_{IH2}$.

***The following represent the key differences between the 103196 and the 041896 version of the DS80C320 data sheet. Please review this summary carefully.***

1. Updated DS80C320 25MHz AC Characteristics.

***The following represent the key differences between the 041895 and the 031096 version of the DS80C320 data sheet. Please review this summary carefully.***

1. Remove Port 0, Port 2 from $V_{OH1}$ specification (PCN B60802).
2. $V_{OH1}$ test specification clarified (RST = $V_{CC}$).
3. Add $t_{AVWL2}$ marking to External Memory Read Cycle figure.
4. Correct TQFP drawing to read 44-pin TQFP.
5. Rotate page 1 TQFP illustration to match assembly specifications.

***The following represent the key differences between the 031096 and the 052296 version of the DS80C320 data sheet. Please review this summary carefully.***

1. Added *Data Sheet Revision Summary* section.

***The following represent the key differences between 05/23/96 and 05/22/96 version of the DS80C320 data sheet and between 05/23/96 and 03/27/95 version of the DS80C323 data sheet. Please review this summary carefully.***

**DS80C320:**

1. Add DS80C323 Characteristics.
2. Change DS80C320 $V_{PFW}$ specification from 4.5V to 4.55V (PCN E62802).
3. Update DS80C320 33MHz AC Characteristics.

**DS80C323:**

1. Delete Data Sheet. Contents moved to DS80C320/DS80C323.