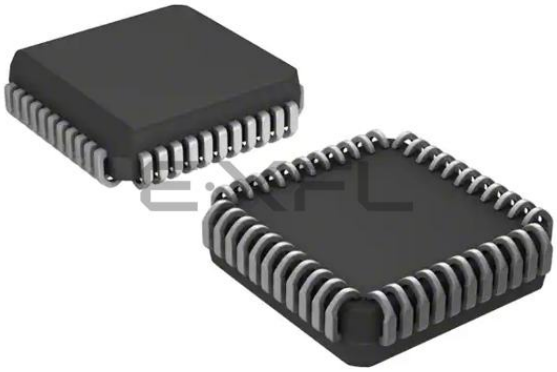

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Details	
Product Status	Last Time Buy
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds80c320-qng

DETAILED DESCRIPTION

The DS80C320/DS80C323 are fast 80C31/80C32-compatible microcontrollers. Wasted clock and memory cycles have been removed using a redesigned processor core. As a result, every 8051 instruction is executed between 1.5 and 3 times faster than the original for the same crystal speed. Typical applications see a speed improvement of 2.5 times using the same code and same crystal. The DS80C320 offers a maximum crystal rate of 33MHz, resulting in apparent execution speeds of 82.5MHz (approximately 2.5X).

The DS80C320/DS80C323 are pin compatible with all three packages of the standard 80C32 and offer the same timer/counters, serial port, and I/O ports. In short, the devices are extremely familiar to 8051 users, but provide the speed of a 16-bit processor.

The DS80C320 provides several extras in addition to greater speed. These include a second full hardware serial port, seven additional interrupts, programmable watchdog timer, power-fail interrupt and reset. The device also provides dual data pointers (DPTRs) to speed block data memory moves. It can also adjust the speed of off-chip data memory access to between two and nine machine cycles for flexibility in selecting memory and peripherals.

The DS80C320 operating voltage ranges from 4.25V to 5.5V, making it ideal as a high-performance upgrade to existing 5V systems. For applications in which power consumption is critical, the DS80C323 offers the same feature set as the DS80C320, but with 2.7V to 5.5V operation.

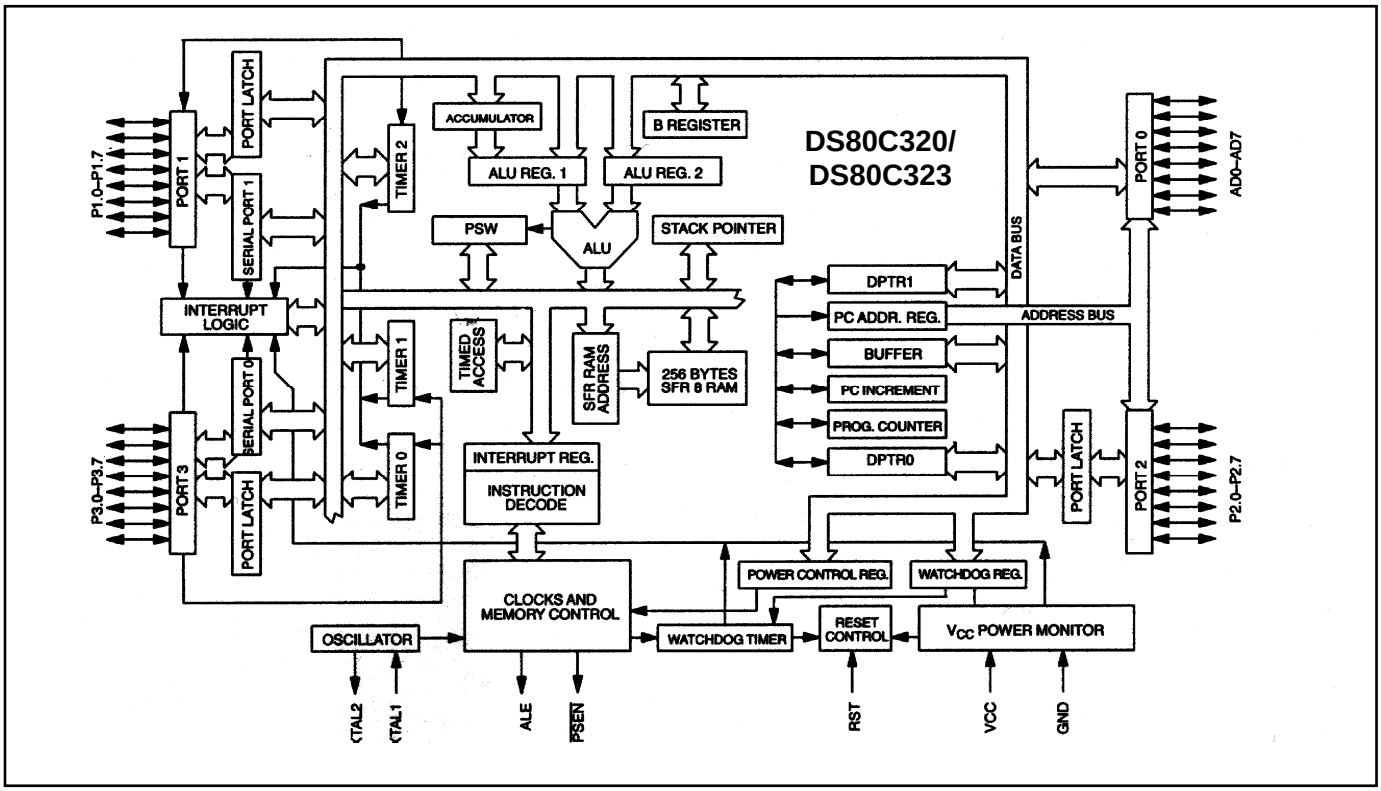
Designers must have two documents to fully use all the features of this device: this data sheet and the *High-Speed Microcontroller User's Guide*, available on our website at www.maxim-ic.com/microcontrollers. Data sheets contain pin descriptions, feature overviews, and electrical specifications, whereas our user's guides contain detailed information about device features and operation.

ORDERING INFORMATION

PART	Pb-FREE/RoHS-COMPLIANT	TEMP RANGE	MAX CLOCK SPEED (MHz)	PIN-PACKAGE
DS80C320-MCG	**DS80C320**-MCG+	0°C to +70°C	25	40 Plastic DIP
DS80C320-QCG	DS80C320-QCG+	0°C to +70°C	25	44 PLCC
DS80C320-ECG	DS80C320-ECG+	0°C to +70°C	25	44 TQFP
DS80C320-MNG	DS80C320-MNG+	-40°C to +85°C	25	40 Plastic DIP
DS80C320-QNG	DS80C320-QNG+	-40°C to +85°C	25	44 PLCC
DS80C320-ENG	DS80C320-ENG+	-40°C to +85°C	25	44 TQFP
DS80C320-MCL	DS80C320-MCL+	0°C to +70°C	33	40 Plastic DIP
DS80C320-QCL	DS80C320-QCL+	0°C to +70°C	33	44 PLCC
DS80C320-ECL	DS80C320-ECL+	0°C to +70°C	33	44 TQFP
DS80C320-MNL	DS80C320-MNL+	-40°C to +85°C	33	40 Plastic DIP
DS80C320-QNL	DS80C320-QNL+	-40°C to +85°C	33	44 PLCC
DS80C320-ENL	DS80C320-ENL+	-40°C to +85°C	33	44 TQFP
DS80C323-MCD	**DS80C323**-MCD+	0°C to +70°C	18	40 Plastic DIP
DS80C323-QCD	DS80C323-QCD+	0°C to +70°C	18	44 PLCC
DS80C323-ECD	DS80C323-ECD+	0°C to +70°C	18	44 TQFP
DS80C323-QND	DS80C323-QND+	-40°C to +85°C	18	44 PLCC
DS80C323-END	DS80C323-END+	-40°C to +85°C	18	44 TQFP

+ Denotes a lead(Pb)-free/RoHS-compliant device.

Figure 1. Block Diagram



PIN DESCRIPTION

PIN			NAME	FUNCTION
DIP	PLCC	TQFP		
40	44	38	V_{CC}	**+5V (+3V for DS80C323)**
20	22, 23	16, 17	GND	**Digital Circuit Ground**
9	10	4	RST	**Reset Input.** The RST input pin contains a Schmitt voltage input to recognize external active-high reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wired OR external reset sources. An RC is ***not*** required for power-up, as the device provides this function internally.
18	20	14	XTAL2	**Crystal Oscillator Pins.** XTAL1 and XTAL2 provide support for parallel-resonant, AT-cut crystals. XTAL1 acts also as an input in the event that an external clock source is used in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
19	21	15	XTAL1	
29	32	26	$\overline{\text{PSEN}}$	**Program Store-Enable Output, Active Low.** This signal is commonly connected to external ROM memory as a chip enable. $\overline{\text{PSEN}}$ provides an active-low pulse width of 2.25 XTAL1 cycles with a period of four XTAL1 cycles. $\overline{\text{PSEN}}$ is driven high when data memory (RAM) is being accessed through the bus and during a reset condition.

PIN DESCRIPTION (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>TQFP</th></tr>
<tr><td>21</td><td>24</td><td>18</td><td>A8 (P2.0)</td><td rowspan="8">Port 2, Output. Port 2 serves as the MSB for external addressing. P2.7 is A15 and P2.0 is A8. The device will automatically place the MSB of an address on P2 for external ROM and RAM access. Although Port 2 can be accessed like an ordinary I/O port, the value stored on the Port 2 latch will never be seen on the pins (due to memory access). Therefore, writing to Port 2 in software is only useful for the instructions MOVX A, @Ri or MOVX @Ri, A. These instructions use the Port 2 internal latch to supply the external address MSB. In this case, the Port 2 latch value will be supplied as the address information.</td></tr>
<tr><td>22</td><td>25</td><td>19</td><td>A9 (P2.1)</td></tr>
<tr><td>23</td><td>26</td><td>20</td><td>A10 (P2.2)</td></tr>
<tr><td>24</td><td>27</td><td>21</td><td>A11 (P2.3)</td></tr>
<tr><td>25</td><td>28</td><td>22</td><td>A12 (P2.4)</td></tr>
<tr><td>26</td><td>29</td><td>23</td><td>A13 (P2.5)</td></tr>
<tr><td>27</td><td>30</td><td>24</td><td>A14 (P2.6)</td></tr>
<tr><td>28</td><td>31</td><td>25</td><td>A15 (P2.7)</td></tr>
<tr><td>10–17</td><td>11, 13–19</td><td>5, 7–13</td><td>P3.0–P3.7</td><td>Port 3, Input/Output. Port 3 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for External Interrupts, Serial Port 0, Timer 0 & 1 Inputs, $\overline{RD}$ and $\overline{WR}$ strobes. The reset condition of Port 3 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the device will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port once again becomes both the output high and input state. The alternate modes of Port 3 are outlined below:
<table>
<tr><th colspan="3">PIN</th><th rowspan="2">PORT</th><th rowspan="2">ALTERNATE</th><th rowspan="2">MODE</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>TQFP</th></tr>
<tr><td>10</td><td>11</td><td>5</td><td>P3.0</td><td>RXD0</td><td>Serial Port 0 Input</td></tr>
<tr><td>11</td><td>13</td><td>7</td><td>P3.1</td><td>TXD0</td><td>Serial Port 0 Output</td></tr>
<tr><td>12</td><td>14</td><td>8</td><td>P3.2</td><td>$\overline{INT0}$</td><td>External Interrupt 0</td></tr>
<tr><td>13</td><td>15</td><td>9</td><td>P3.3</td><td>$\overline{INT1}$</td><td>External Interrupt 1</td></tr>
<tr><td>14</td><td>16</td><td>10</td><td>P3.4</td><td>T0</td><td>Timer 0 External Input</td></tr>
<tr><td>15</td><td>17</td><td>11</td><td>P3.5</td><td>T1</td><td>Timer 1 External Input</td></tr>
<tr><td>16</td><td>18</td><td>12</td><td>P3.6</td><td>$\overline{WR}$</td><td>External Data Memory Write Strobe</td></tr>
<tr><td>17</td><td>19</td><td>13</td><td>P3.7</td><td>$\overline{RD}$</td><td>External Data Memory Read Strobe</td></tr>
</table></td></tr>
<tr><td>31</td><td>35</td><td>29</td><td>$\overline{EA}$</td><td>External Access, Active-Low Input. This pin must be connected to ground for proper operation.</td></tr>
<tr><td>—</td><td>12, 34, 1*</td><td>6, 28, 39*</td><td>N.C.</td><td>No Connection (Reserved). These pins should not be connected. They are reserved for use with future devices in this family.
*These pins are reserved for additional ground pins on future products.</td></tr>
</table>

80C32 COMPATIBILITY

The DS80C320/DS80C323 are CMOS 80C32-compatible microcontrollers designed for high performance. In most cases, the devices will drop into an existing 80C32 design to significantly improve the operation. Every effort has been made to keep the devices familiar to 8032 users, yet they have many new features. In general, software written for existing 80C32-based systems will work on the DS80C320 and DS80C323. The exception is critical timing, because the high-speed microcontroller performs its instructions much faster than the original. It may be necessary to use memories with faster access times if the same crystal frequency is used.

Application Note 57: DS80C320 Memory Interface Timing is a useful tool to help the embedded system designer select the proper memories for her or his application.

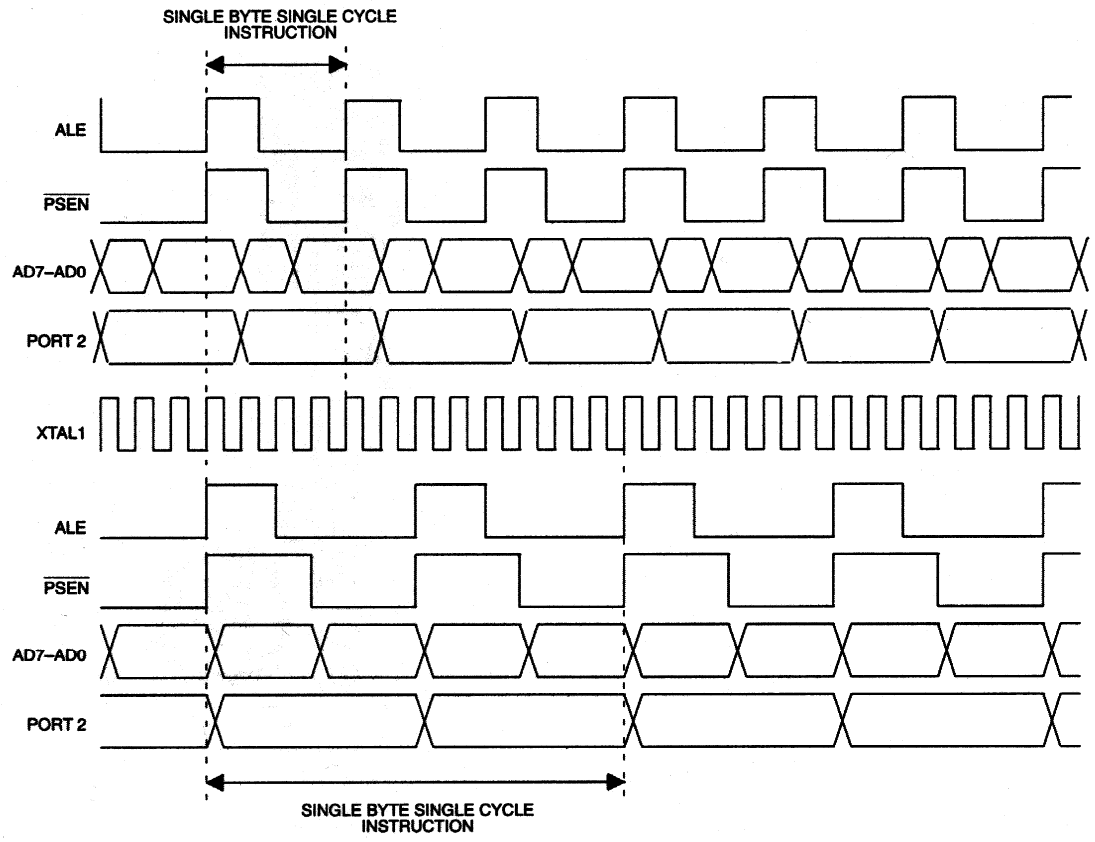
The DS80C320/DS80C323 run the standard 8051 instruction set and is pin compatible with an 80C32 in any of three standard packages. They also provide the same timer/counter resources, full-duplex serial port, 256 bytes of scratchpad RAM, and I/O ports as the standard 80C32. Timers will default to a 12 clock-per-cycle operation to keep timing compatible with original 8051 systems. However, they can be programmed to run at the new 4 clocks per cycle if desired.

New hardware features are accessed using special-function registers that do not overlap with standard 80C32 locations. A summary of these SFRs is provided below.

The DS80C320/DS80C323 address memory in an identical fashion to the standard 80C32. Electrical timing appears different due to the high-speed nature of the product. However, the signals are essentially the same. Detailed timing diagrams are provided in the *Electrical Specifications* section.

This data sheet assumes the user is familiar with the basic features of the standard 80C32. In addition to these standard features, the DS80C320/DS80C323 include many new functions. This data sheet provides only a summary and overview. Detailed descriptions are available in the *High-Speed Microcontroller User's Guide*.

Figure 2. Comparative Timing of the DS80C320/DS80C323 and 80C32



HIGH-SPEED OPERATION

The DS80C320/DS80C323 are built around a high-speed, 80C32-compatible core. Higher speed comes not just from increasing the clock frequency but also from a newer, more efficient design.

In this updated core, dummy memory cycles have been eliminated. In a conventional 80C32, machine cycles are generated by dividing the clock frequency by 12. In the DS80C320/DS80C323, the same machine cycle is performed in 4 clocks. Thus the fastest instruction, one machine cycle, is executed three times faster for the same crystal frequency. Note that these are identical instructions. Figure 2 shows a comparison of the timing differences. The majority of instructions will see the full 3-to-1 speed improvement. Some instructions will get between 1.5X and 2.4X improvement. Note that all instructions are faster than the original 80C51. Table 1 shows a summary of the instruction set, including the speed.

The numerical average of all op codes is approximately a 2.5-to-1 speed improvement. Individual programs are affected differently, depending on the actual instructions used. Speed-sensitive applications would make the most use of instructions that are three times faster. However, the sheer number of 3-to-1 improved op codes makes dramatic speed improvements likely for any code. The Dual Data Pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory.

Table 1. Instruction Set Summary

SYMBOL	FUNCTION
A	Accumulator
Rn	Register R7 to R0
direct	Internal Register Address
@Ri	Internal Register pointed to by R0 or R1 (except MOVX)
rel	Two's Complement Offset Byte

SYMBOL	FUNCTION
bit	direct bit-address
#data	8-bit constant
#data 16	16-bit constant
addr 16	16-bit destination address
addr 11	11-bit destination address

INSTRUCTION	BYTE	OSCILLATOR CYCLES	INSTRUCTION	BYTE	OSCILLATOR CYCLES
ARITHMATIC INSTRUCTIONS					
ADD A, Rn	1	4	INC A	1	4
ADD A, direct	2	8	INC Rn	1	4
ADD A, @Ri	1	4	INC direct	2	8
ADD A, #data	2	8	INC @Ri	1	4
ADDC A, Rn	1	4	INC DPTR	1	12
ADDC A, direct	2	8	DEC A	1	4
ADDC A, @Ri	1	4	DEC Rn	1	4
ADDC A, #data	2	8	DEC direct	2	8
SUBB A, Rn	1	4	DEC @Ri	1	4
SUBB A, direct	2	8	MUL AB	1	20
SUBB A, @Ri	1	4	DIV AB	1	20
SUBB A, #data	2	8	DA A	1	4
LOGICAL INSTRUCTIONS					
ANL A, Rn	1	4	XRL A, Rn	1	4
ANL A, direct	2	8	XRL A, direct	2	8
ANL A, @Ri	1	4	XRL A, @Ri	1	4
ANL A, #data	2	8	XRL A, #data	2	8
ANL direct, A	2	8	XRL direct, A	2	8
ANL direct, #data	3	12	XRL direct, #data	3	12
ORL A, Rn	1	4	CLR A	1	4
ORL A, direct	2	8	CPL A	1	4
ORL A, @Ri	1	4	RL A	1	4
ORL A, #data	2	8	RLC A	1	4
ORL direct, A	2	8	RR A	1	4
ORL direct, #data	3	12	RRC A	1	4

Table 1 shows the speed for each class of instruction. Note that many of the instructions have multiple op codes. There are 255 op codes for 111 instructions. Of the 255 op codes, 159 are three times faster than the original 80C32. While a system that emphasizes those instructions will see the most improvement, the large total number that receive a 3 to 1 improvement assure a dramatic speed increase for any system. The speed improvement summary is provided below.

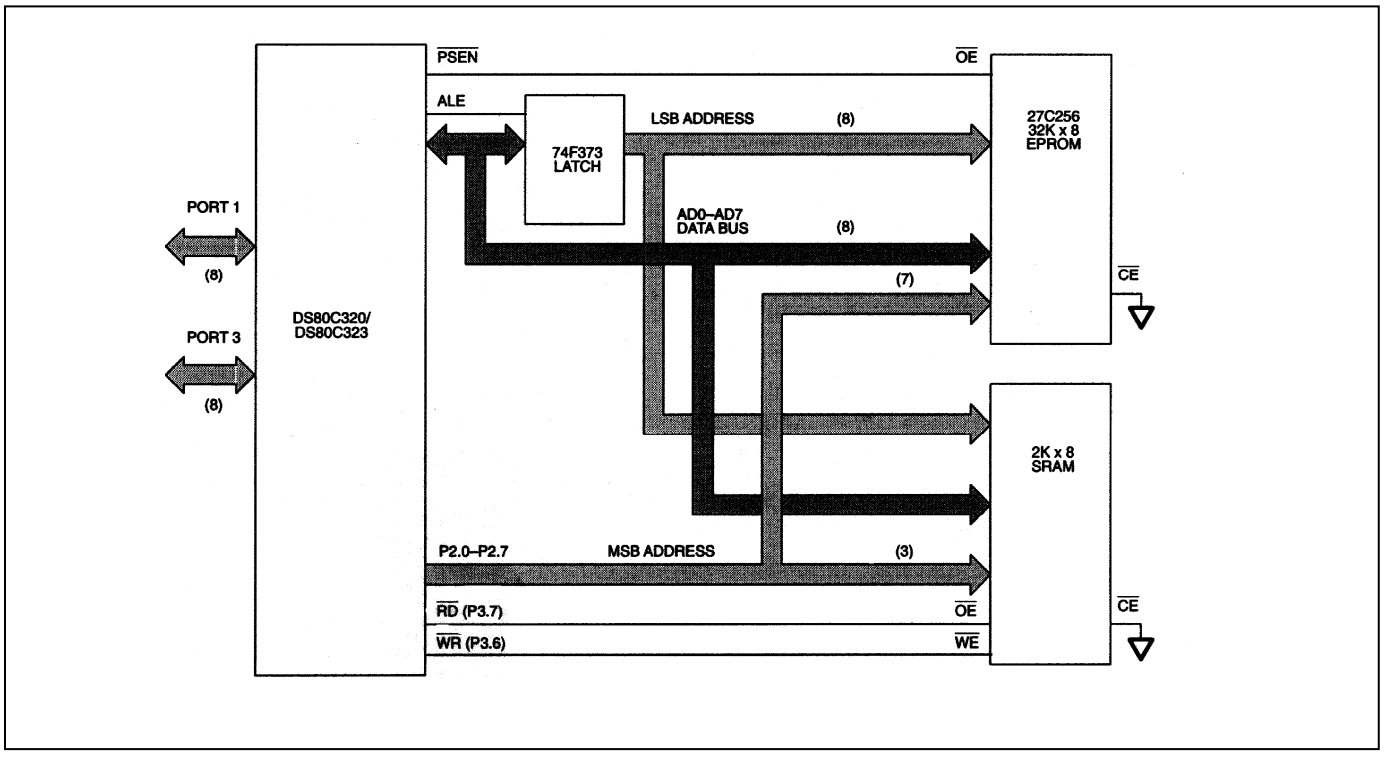
SPEED ADVANTAGE SUMMARY

#OP CODES	SPEED IMPROVEMENT
159	3.0 x
51	1.5 x
43	2.0 x
2	2.4 x
255	Average: 2.5

MEMORY ACCESS

The DS80C320/DS80C323 do not contain on-chip ROM and 256 bytes of scratchpad RAM. Off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. Figure 3 shows a typical memory connection. Timing diagrams are provided in the *Electrical Specifications* section. Program memory (ROM) is accessed at a fixed rate determined by the crystal frequency and the actual instructions. As previously mentioned, an instruction cycle requires 4 clocks. Data memory (RAM) is accessed according to a variable-speed MOVX instruction as described below.

Figure 3. Typical Memory Connection



STRETCH MEMORY CYCLE

The DS80C320/DS80C323 allow the application software to adjust the speed of data memory access. The microcontroller is capable of performing the MOVX in as little as two instruction cycles. However, this value can be stretched as needed so that both fast memory and slow memory or peripherals can be accessed with no glue logic. Even in high-speed systems, it may not be necessary or desirable to perform data memory access at full speed. In addition, there are a variety of memory-mapped peripherals such as LCD displays or UARTs that are not fast.

The Stretch MOVX is controlled by the Clock Control Register at SFR location 8Eh as described below. This allows the user to select a stretch value between 0 and 7. A Stretch of 0 will result in a two-machine cycle MOVX. A Stretch of 7 will result in a MOVX of nine machine cycles. Software can dynamically change this value depending on the particular memory or peripheral.

On reset, the Stretch value will default to 1, resulting in a three-cycle MOVX. Therefore, RAM access will not be performed at full speed. This is a convenience to existing designs that may not have fast RAM in place. When maximum speed is desired, the software should select a Stretch value of 0. When using very slow RAM or peripherals, a larger stretch value can be selected. Note that this affects data memory only and the only way to slow program memory (ROM) access is to use a slower crystal.

Using a Stretch value between 1 and 7 causes the microcontroller to stretch the read/write strobe and all related timing. This results in a wider read/write strobe allowing more time for memory/peripherals to respond. The timing of the variable speed MOVX is shown in the *Electrical Specifications* section. Note that full speed access is not the reset default case. Table 2 shows the resulting strobe widths for each Stretch value. The memory stretch is implemented using the Clock Control special-function register at SFR location 8Eh. The stretch value is selected using bits CKCON.2–0. In the table, these bits are referred to as M2 through M0. The first stretch (default) allows the use of common 120ns or 150ns RAMs without dramatically lengthening the memory access.

Table 2. Data Memory Cycle Stretch Values

CKCON.2–0			MEMORY CYCLES	$\overline{RD}$ or $\overline{WR}$ STROBE WIDTH IN CLOCKS	STROBE WIDTH TIME AT 25MHz (ns)
MD2	MD1	MD0			
0	0	0	2	2	80
0	0	1	3 (default)	4	160
0	1	0	4	8	320
0	1	1	5	12	480
1	0	0	6	16	640
1	0	1	7	20	800
1	1	0	8	24	960
1	1	1	9	28	1120

POWER-FAIL RESET

The DS80C320/DS80C323 incorporate a precision bandgap voltage reference to determine when V_{CC} is out of tolerance. While powering up, internal circuits will hold the device in a reset state until V_{CC} rises above the V_{RST} reset threshold. Once V_{CC} is above this level, the oscillator will begin running. An internal reset circuit will then count 65,536 clocks to allow time for power and the oscillator to stabilize. The microcontroller will then exit the reset condition. No external components are needed to generate a power on reset. During power-down or during a severe power glitch, as V_{CC} falls below V_{RST}, the microcontroller will also generate its own reset. It will hold the reset condition as long as power remains below the threshold. This reset will occur automatically, needing no action from the user or from the software. See the *Electrical Specifications* section for the exact value of V_{RST}.

POWER-FAIL INTERRUPT

The same reference that generates a precision reset threshold can also generate an optional early warning Power-fail Interrupt (PFI). When enabled by the application software, this interrupt always has the highest priority. On detecting that the V_{CC} has dropped below V_{PFW} and that the PFI is enabled, the processor will vector to ROM address 0033h. The PFI enable is located in the Watchdog Control SFR (WDCON to D8h). Setting WDCON.5 to logic 1 will enable the PFI. The application software can also read a flag at WDCON.4. This bit is set when a PFI condition has occurred. The flag is independent of the interrupt enable and software must manually clear it.

WATCHDOG TIMER

For applications that cannot afford to run out of control, the DS80C320/DS80C323 incorporate a programmable watchdog timer circuit. The watchdog timer circuit resets the microcontroller if software fails to reset the watchdog before the selected time interval has elapsed. The user selects one of four timeout values. After enabling the watchdog, software must reset the timer prior to expiration of the interval, or the CPU will be reset. Both the Watchdog Enable and the Watchdog Reset bits are protected by a "Timed Access" circuit. This prevents accidentally clearing the watchdog. Timeout values are precise since they are related to the crystal frequency as shown in Table 3. For reference, the time periods at 25MHz are also shown.

The watchdog timer also provides a useful option for systems that may not require a reset. If enabled, then 512 clocks before giving a reset, the watchdog will give an interrupt. The interrupt can also serve as a convenient time-base generator, or be used to wake-up the processor from Idle mode. The watchdog function is controlled in the Clock Control (CKCON to 8Eh), Watchdog Control (WDCON to D8h), and Extended Interrupt Enable (EIE to E8h) SFRs. CKCON.7 and CKCON.6 are called WD1 and WD0, respectively, and are used to select the watchdog timeout period as shown in Table 3.

Table 3. Watchdog Timeout Values

WD1	WD0	INTERRUPT TIMEOUT	TIME (at 25MHz)	RESET TIMEOUT	TIME (at 25MHz)
0	0	2^{17} clocks	5.243ms	2^{17} + 512 clocks	5.263ms
0	1	2^{20} clocks	41.94ms	2^{20} + 512 clocks	41.96ms
1	0	2^{23} clocks	335.54ms	2^{23} + 512 clocks	335.56ms
1	1	2^{26} clocks	2684.35ms	2^{26} + 512 clocks	2684.38ms

As Table 3 shows, the watchdog timer uses the crystal frequency as a time base. A user selects one of four counter values to determine the timeout. These clock counter lengths are 2^{17} = 131,072 clocks; 2^{20} = 1,048,576; 2^{23} = 8,388,608 clocks; or 2^{26} = 67,108,864 clocks. The times shown in Table 4 are with

Figure 4. Ring Oscillator Startup

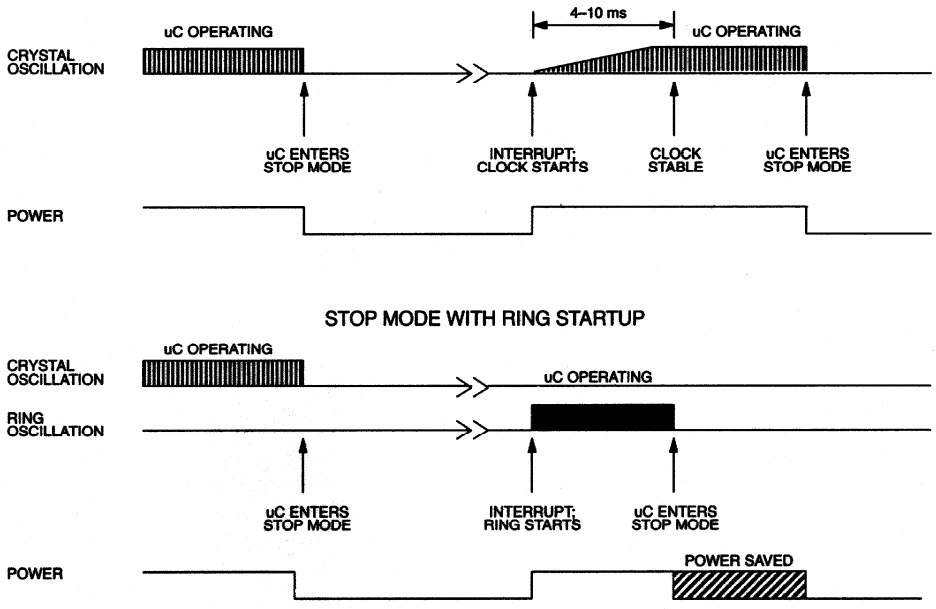


DIAGRAM ASSUMES THAT THE OPERATION FOLLOWING STOP REQUIRES LESS THAN 18ms COMPLETE.

TIMED ACCESS PROTECTION

Selected SFR bits are critical to operation, making it desirable to protect against an accidental write operation. The Timed Access procedure prevents an errant CPU from accidentally altering a bit that would cause difficulty. The Timed Access procedure requires that the write of a protected bit be preceded by the following instructions:

```
MOV     0C7h, #0AAh
MOV     0C7h, #55h
```

By writing an AAh followed by a 55h to the Timed Access register (location C7h), the hardware opens a three-cycle window that allows software to modify one of the protected bits. If the instruction that seeks to modify the protected bit is not immediately proceeded by these instructions, the write will not take effect. The protected bits are:

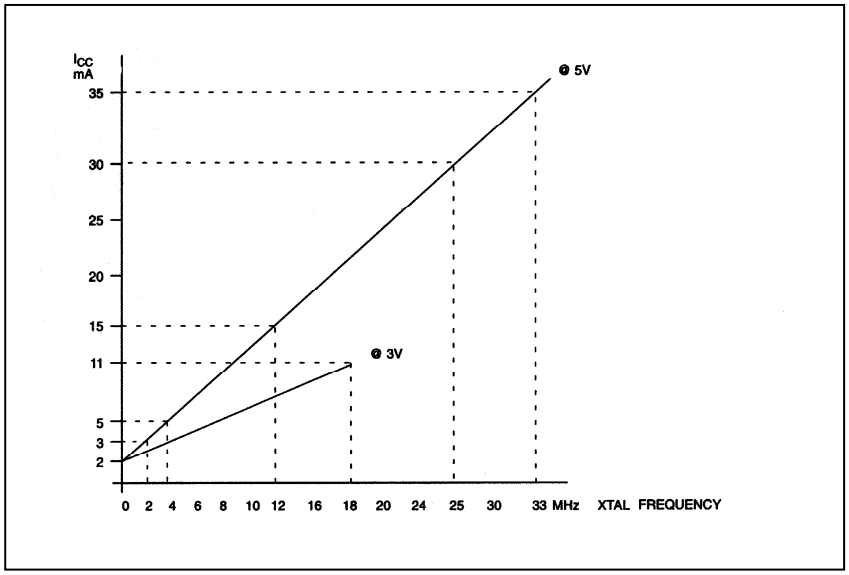
EXIF.0	BGS Bandgap Select
WDCON.6	POR Power-on Reset flag
WDCON.1	EWT Enable Watchdog
WDCON.0	RWT Reset Watchdog
WDCON.3	WDIF Watchdog Interrupt Flag

NOTES FOR DS80C320 DC ELECTRICAL CHARACTERISTICS

All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested.

1. All voltages are referenced to ground.
2. Active current is measured with a 25MHz clock source driving XTAL1, V_{CC} = RST = 5.5V, all other pins disconnected.
3. Idle mode current is measured with a 25MHz clock source driving XTAL1, V_{CC} = 5.5V, RST at ground, all other pins disconnected.
4. Stop mode current measured with XTAL1 and RST grounded, V_{CC} = 5.5V, all other pins disconnected.
5. When addressing external memory. This specification only applies to the first clock cycle following transition.
6. RST = V_{CC}. This condition mimics operation of pins in I/O mode.
7. During a 0-to-1 transition, a one-shot drives the ports hard for two clock cycles. This measurement reflects port in transition mode.
8. Ports 1 and 3 source transition current when being pulled down externally. It reaches its maximum at approximately 2V.
9. $0.45<V_{IN}<V_{CC}$. Not a high-impedance input. This port is a weak address holding latch because Port 0 is dedicated as an address bus on the DS80C320. Peak current occurs near the input transition point of the latch, approximately 2V.
10. Over the industrial temperature range, this specification has a maximum value of 200µA.
11. This is the current required from an external circuit to hold a logic low level on an I/O pin while the corresponding port latch bit is set to 1. This is only the current required to *hold* the low level; transitions from 1 to 0 on an I/O pin will also have to overcome the transition current.
12. Device operating range is 4.5V to 5.5V; however, device is tested to 4.0V to ensure proper operation at minimum V_{RST}.

TYPICAL I_{CC} vs. FREQUENCY



AC CHARACTERISTICS—DS80C320

PARAMETER		SYMBOL	33MHz		VARIABLE CLOCK		UNITS
			MIN	MAX	MIN	MAX	
Oscillator Frequency	External Oscillator	$1/t_{CLCL}$	0	33	0	33	MHz
	External Crystal		1	33	1	33	
ALE Pulse Width		t_{LHLL}	34		$1.5t_{CLCL}$-11		ns
Port 0 Address Valid to ALE Low		t_{AVLL}	4		$0.5t_{CLCL}$-11		ns
Address Hold After ALE Low		t_{LLAX1}	2	(Note 5)	$0.25t_{CLCL}$-5	(Note 5)	ns
Address Hold After ALE Low for MOVX $\overline{WR}$		t_{LLAX2}	6		$0.5t_{CLCL}$-9		ns
ALE Low to Valid Instruction In		t_{LLIV}		49		$2.5t_{CLCL}$-27	ns
ALE Low to $\overline{PSEN}$ Low		t_{LLPL}	0.5		$0.25t_{CLCL}$-7		ns
$\overline{PSEN}$ Pulse Width		t_{PLPH}	61		$2.25t_{CLCL}$-7		ns
$\overline{PSEN}$ Low to Valid Instruction In		t_{PLIV}		48		$2.25t_{CLCL}$-21	ns
Input Instruction Hold After $\overline{PSEN}$		t_{PXIX}	0		0		ns
Input Instruction Float After $\overline{PSEN}$		t_{PXIZ}		25		t_{CLCL}-5	ns
Port 0 Address to Valid Instruction In		t_{AVIV1}		64		$3t_{CLCL}$-27	ns
Port 2 Address to Valid Instruction In		t_{AVIV2}		73		$3.5t_{CLCL}$-33	ns
$\overline{PSEN}$ Low to Address Float		t_{PLAZ}		(Note 5)		(Note 5)	ns

NOTES FOR DS80C320 AC ELECTRICAL CHARACTERISTICS

All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested. AC electrical characteristics assume 50% duty cycle for the oscillator, oscillator frequency > 16MHz, and are not 100% tested, but are guaranteed by design.

1. All signals rated over operating temperature at 33MHz.
2. All signals characterized with load capacitance of 80pF except Port 0, ALE, $\overline{PSEN}$, $\overline{RD}$ and $\overline{WR}$ at 100pF. Note that loading should be approximately equal for valid timing.
3. Interfacing to memory devices with float times (turn off times) over 30ns may cause contention. This will not damage the parts but will cause an increase in operating current.
4. Specifications assume a 50% duty cycle for the oscillator. Port 2 timing will change with the duty cycle variations.
5. Address is held in a weak latch until over driven by external memory.

DC ELECTRICAL CHARACTERISTICS—DS80C323

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Voltage	V_{CC}	2.7	3.0	5.5	V	1
Power-Fail Warning Voltage	V_{PFW}	2.6	2.7	2.8	V	1
Minimum Operating Voltage	V_{RST}	2.5	2.6	2.7	V	1, 12
Supply Current Active Mode at 18MHz	I_{CC}		10		mA	2
Supply Current Idle Mode at 18MHz	I_{IDLE}		6		mA	3
Supply Current Stop Mode, Bandgap Reference Disabled	I_{STOP}		0.1		µA	2
Supply Current Stop Mode, Bandgap Reference Enabled	I_{SPBG}		40		µA	4, 10
Input Low Level	V_{IL}	-0.3		+0.2 x V_{CC}	V	1
Input High Level (Except XTAL1 and RST)	V_{IH1}	0.7 x V_{CC}		V_{CC}+0.3	V	1
Input High Level XTAL1 and RST	V_{IH2}	0.7 x V_{CC} +0.25V		V_{CC}+0.3	V	1
Output Low Voltage Ports 1, 3 at I_{OL} = 1.6mA	V_{OL1}			0.4	V	1
Output Low Voltage Ports 0, 2, $\overline{PSEN}$ /ALE at I_{OL} = 3.2mA	V_{OL2}			0.4	V	1, 5
Output High Voltage Ports 1, 3, $\overline{PSEN}$ /ALE at I_{OH} = -15µA	V_{OH1}	V_{DD} -0.4V			V	1, 6
Output High Voltage Ports 1, 3 at I_{OH} = -1.5mA	V_{OH2}	V_{DD} -0.4V			V	1, 7
Output High Voltage Ports 0, 2, $\overline{PSEN}$ /ALE at I_{OH} = -2mA	V_{OH3}	V_{DD} -0.4V			V	1, 5
Input Low Current Ports 1, 3 at 0.45V	I_{IL}			-30	µA	11
Transition Current from 1 ≥ 0, Ports 1, 3 at 2V	I_{TL}			-400	µA	8
Input Leakage Port 0, Bus Mode	I_L	-300		+300	µA	9
RST Pulldown Resistance	R_{RST}	50		170	kΩ	

NOTES FOR DS80C323 DC ELECTRICAL CHARACTERISTICS

All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested. Device operating range is 2.7V to 5.5V. DC electrical specifications are for operation 2.7V to 3.3V.

1. All voltages are referenced to ground.
2. Active mode current is measured with an 18MHz clock source driving XTAL1, V_{CC} = RST = 3.3V, all other pins disconnected.
3. Idle mode current is measured with an 18MHz clock source driving XTAL1, V_{CC} = 3.3V, all other pins disconnected.
4. Stop mode current measured with XTAL1 and RST grounded, V_{CC} = 3.3V, all other pins disconnected.
5. When addressing external memory. This specification only applies to the first clock cycle following the transition.

AC ELECTRICAL CHARACTERISTICS—DS80C323

PARAMETER		SYMBOL	18 MHz		VARIABLE CLOCK		UNITS
			MIN	MAX	MIN	MAX	
Oscillator Frequency	External Oscillator	$1/t_{CLCL}$	0	18	0	18	MHz
	External Crystal		1	18	1	18	
ALE Pulse Width		t_{LHLL}	68		$1.5t_{CLCL}$-15		ns
Port 0 Address Valid to ALE Low		t_{AVLL}	16		$0.5t_{CLCL}$-11		ns
Address Hold After ALE Low		t_{LLAX1}	6	(Note 5)	$0.25t_{CLCL}$-8	(Note 5)	ns
Address Hold After ALE Low for MOVX $\overline{WR}$		t_{LLAX2}	14		$0.5t_{CLCL}$-13		ns
ALE Low to Valid Instruction In		t_{LLIV}		93		$2.5t_{CLCL}$-46	ns
ALE Low to $\overline{PSEN}$ Low		t_{LLPL}	4		$0.25t_{CLCL}$-10		ns
$\overline{PSEN}$ Pulse Width		t_{PLPH}	118		$2.25t_{CLCL}$-7		ns
$\overline{PSEN}$ Low to Valid Instruction In		t_{PLIV}		87		$2.25t_{CLCL}$-38	ns
Input Instruction Hold After $\overline{PSEN}$		t_{PXIX}	0		0		ns
Input Instruction Float After $\overline{PSEN}$		t_{PXIZ}		51		t_{CLCL}-5	ns
Port 0 Address to Valid Instruction In		t_{AVIV1}		128		$3t_{CLCL}$-39	ns
Port 2 Address to Valid Instruction In		t_{AVIV2}		139		$3.5t_{CLCL}$-56	ns
$\overline{PSEN}$ Low to Address Float		t_{PLAZ}		(Note 5)		(Note 5)	ns

NOTES FOR DS80C323 AC ELECTRICAL CHARACTERISTICS

All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested. AC electrical characteristics assume 50% duty cycle for the oscillator, oscillator frequency > 16MHz, and are not 100% production tested, but are guaranteed by design.

1. All signals rated over operating temperature at 18MHz.
2. All signals characterized with load capacitance of 80pF except Port 0, ALE, $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}$ at 100pF. Note that loading should be approximately equal for valid timing.
3. Interfacing to memory devices with float times (turn off times) over 35ns may cause contention. This will not damage the parts, but will cause an increase in operating current.
4. Specifications assume a 50% duty cycle for the oscillator. Port 2 timing will change with the duty cycle variations.
5. Address is held in a weak latch until over-driven by external memory.

MOVX CHARACTERISTICS—DS80C323

PARAMETER	SYMBOL	VARIABLE CLOCK		UNITS	STRETCH
		MIN	MAX		
$\overline{RD}$ Pulse Width	t_{RLRH}	$2t_{CLCL}$-11		ns	t_{MCS}=0
		t_{MCS}-11			t_{MCS}>0
$\overline{WR}$ Pulse Width	t_{WLWH}	$2t_{CLCL}$-11		ns	t_{MCS}=0
		t_{MCS}-11			t_{MCS}>0
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2t_{CLCL}$-32	ns	t_{MCS}=0
			t_{MCS}-36		t_{MCS}>0
Data Hold After Read	t_{RHDX}	0		ns	
Data Float After Read	t_{RHDZ}		t_{CLCL}-5	ns	t_{MCS}=0
			$2t_{CLCL}$-7		t_{MCS}>0
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL}$-43	ns	t_{MCS}=0
			$1.5t_{CLCL}$-45+t_{MCS}		t_{MCS}>0
Port 0 Address to Valid Data In	t_{AVDV1}		$3t_{CLCL}$-40	ns	t_{MCS}=0
			$2t_{CLCL}$-42+t_{MCS}		t_{MCS}>0
Port 2 Address to Valid Data In	t_{AVDV2}		$3.5t_{CLCL}$-58	ns	t_{MCS}=0
			$2.5t_{CLCL}$-59+t_{MCS}		t_{MCS}>0
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL}$-18	$0.5t_{CLCL}$+7	ns	t_{MCS}=0
		$1.5t_{CLCL}$-11	$1.5t_{CLCL}$+8		t_{MCS}>0
Port 0 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	t_{CLCL}-10		ns	t_{MCS}=0
		$2t_{CLCL}$-10			t_{MCS}>0
Port 2 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL}$-27		ns	t_{MCS}=0
		$2.5t_{CLCL}$-25			t_{MCS}>0
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-14		ns	t_{MCS}=0
		t_{CLCL}-13			t_{MCS}>0
Data Hold After Write	t_{WHQX}	t_{CLCL}-15		ns	t_{MCS}=0
		$2t_{CLCL}$-13			t_{MCS}>0
$\overline{RD}$ Low to Address Float	t_{RLAZ}		(Note 5)	ns	
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{WHLH}	-1	14	ns	t_{MCS}=0
		t_{CLCL}-5	t_{CLCL}+16		t_{MCS}>0

Note: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.

M2	M1	M0	MOVX CYCLES	t_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles (default)	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Clock High Time	t_{CHCX}	10			ns
Clock Low Time	t_{CLCX}	10			ns
Clock Rise Time	t_{CLCH}			5	ns
Clock Fall Time	t_{CHCL}			5	ns

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

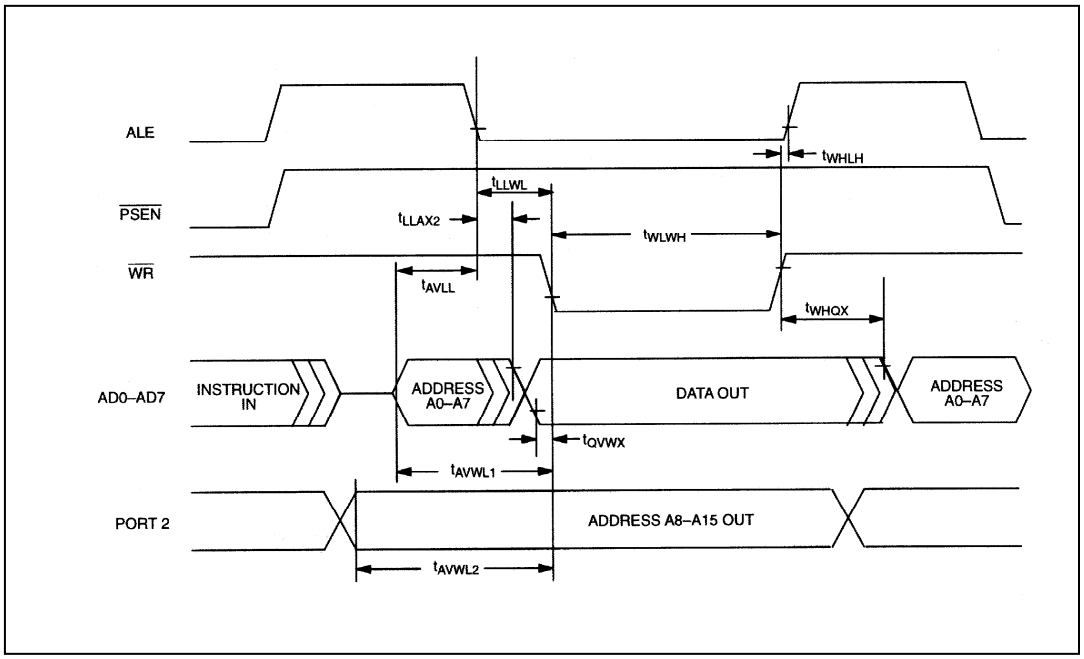
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Port Clock Cycle Time	t_{XLXL}	SM2 = 0; 12 clocks per cycle		$12t_{CLCL}$		ns
		SM2 = 1; 4 clocks per cycle		$4t_{CLCL}$		
Output Data Setup to Clock Rising Edge	t_{QVXH}	SM2 = 0 12 clocks per cycle		$10t_{CLCL}$		ns
		SM2 = 1; 4 clocks per cycle		$3t_{CLCL}$		
Output Data Hold from Clock Rising	t_{XHQX}	SM2 = 0 12 clocks per cycle		$2t_{CLCL}$		ns
		SM2 = 1; 4 clocks per cycle		t_{CLCL}		
Input Data Hold After Clock Rising	t_{XHDX}	SM2 = 0; 12 clocks per cycle		t_{CLCL}		ns
		SM2 = 1; 4 clocks per cycle		t_{CLCL}		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0; 12 clocks per cycle		$11t_{CLCL}$		ns
		SM2 = 1 4 clocks per cycle		$2t_{CLCL}$		

EXPLANATION OF AC SYMBOLS

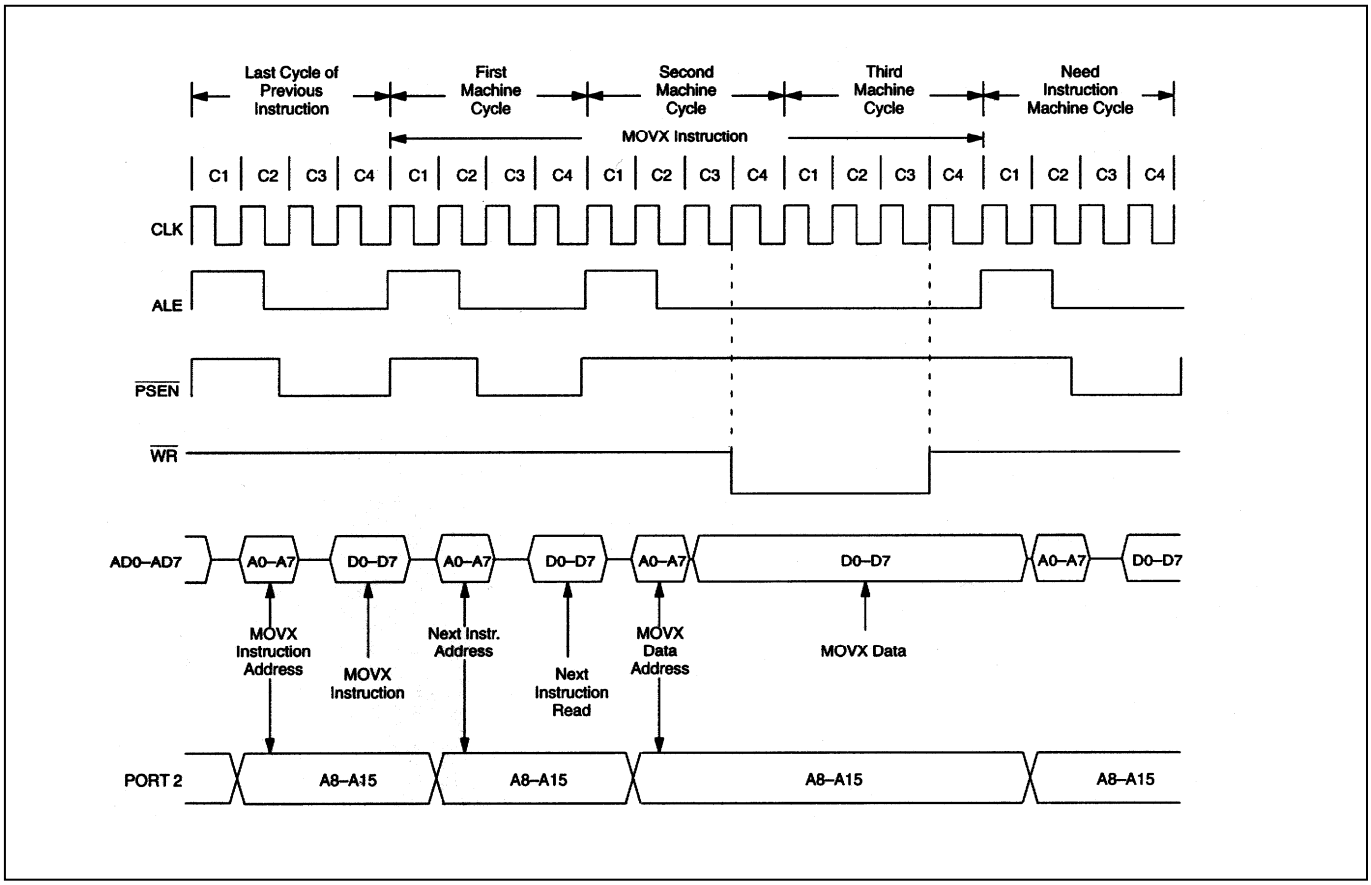
In an effort to remain compatible with the original 8051 family, this device specifies the same parameter as such devices, using the same symbols. For completeness, the following is an explanation of the symbols.

t	Time
A	Address
C	Clock
D	Input data
H	Logic level high
L	Logic level low
I	Instruction
P	$\overline{\text{PSEN}}$
Q	Output data
R	$\overline{\text{RD}}$ signal
V	Valid
W	$\overline{\text{WR}}$ signal
X	No longer a valid logic level
Z	Tri-state

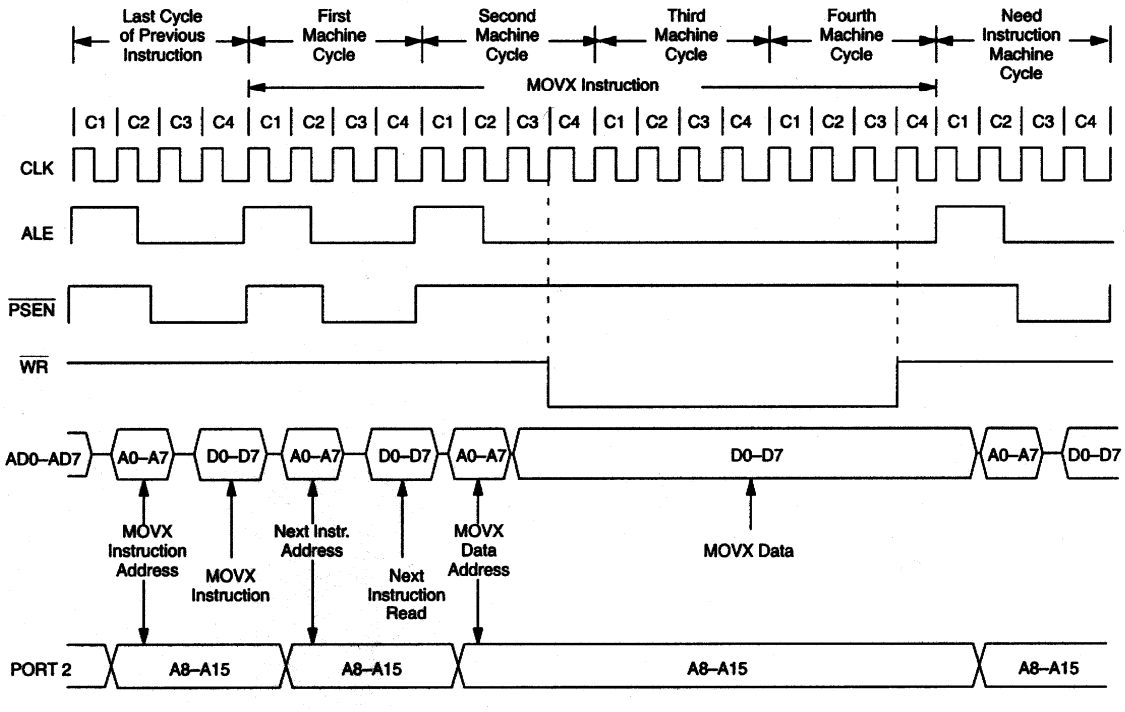
DATA MEMORY WRITE CYCLE



DATA MEMORY WRITE WITH STRETCH = 1

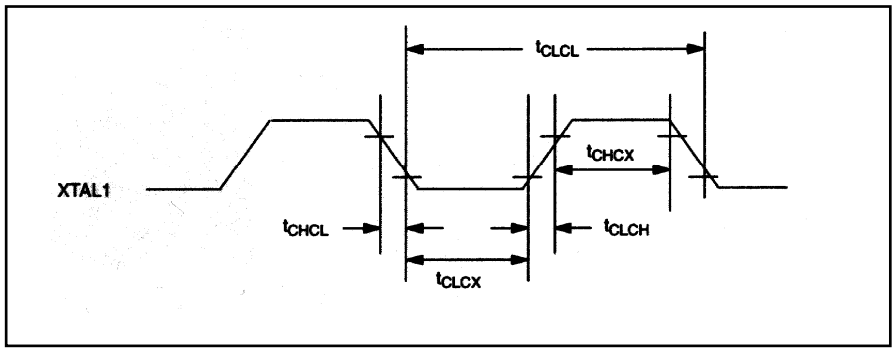


DATA MEMORY WRITE WITH STRETCH = 2

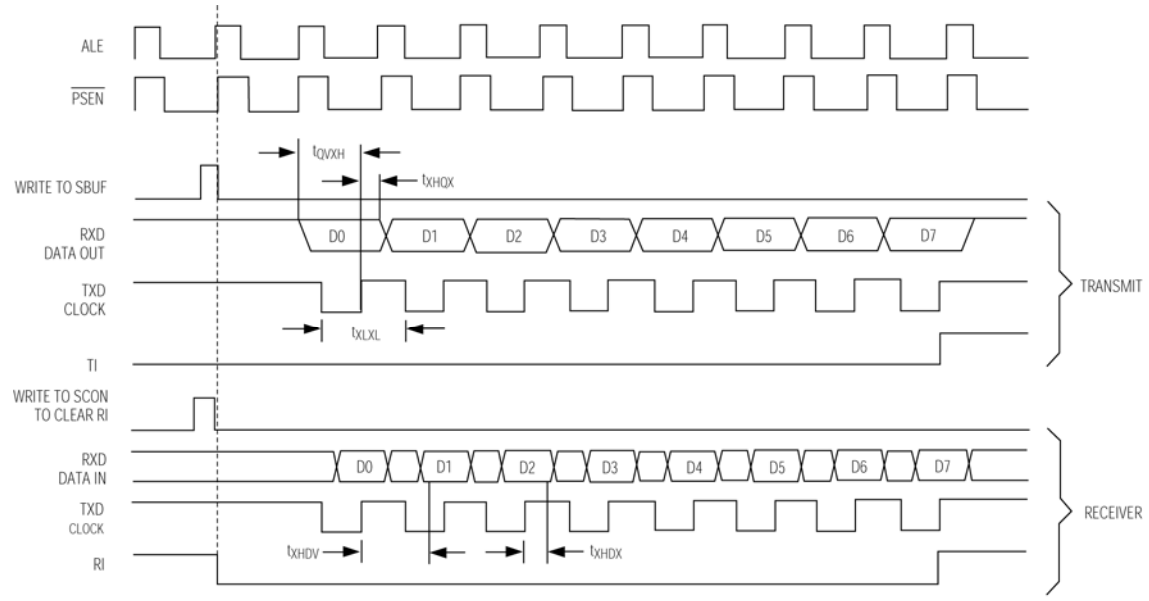


4-CYCLE DATA MEMORY WRITE
STRETCH VALUE = 2

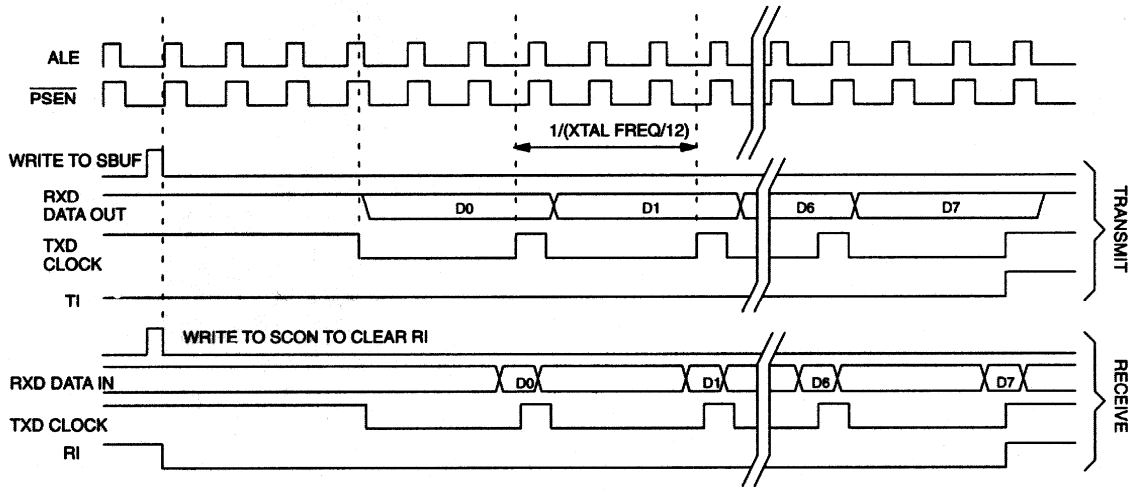
EXTERNAL CLOCK DRIVE



SERIAL PORT MODE 0 TIMING



SERIAL PORT 0 (SYNCHRONOUS MODE)
HIGH SPEED OPERATION SM2 = 1 ≥ TXD CLOCK = XTAL/4



SERIAL PORT 0 (SYNCHRONOUS MODE)
SM2 = 0 ≥ TXD CLOCK = XTAL/12

POWER-CYCLE TIMING