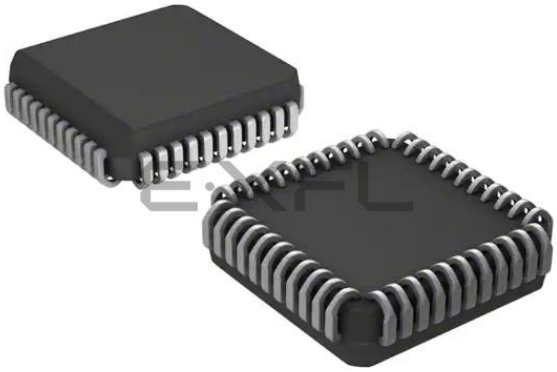
Analog Devices Inc./Maxim Integrated - DS80C320-QNL+ Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds80c320-qnl

DETAILED DESCRIPTION

The DS80C320/DS80C323 are fast 80C31/80C32-compatible microcontrollers. Wasted clock and memory cycles have been removed using a redesigned processor core. As a result, every 8051 instruction is executed between 1.5 and 3 times faster than the original for the same crystal speed. Typical applications see a speed improvement of 2.5 times using the same code and same crystal. The DS80C320 offers a maximum crystal rate of 33MHz, resulting in apparent execution speeds of 82.5MHz (approximately 2.5X).

The DS80C320/DS80C323 are pin compatible with all three packages of the standard 80C32 and offer the same timer/counters, serial port, and I/O ports. In short, the devices are extremely familiar to 8051 users, but provide the speed of a 16-bit processor.

The DS80C320 provides several extras in addition to greater speed. These include a second full hardware serial port, seven additional interrupts, programmable watchdog timer, power-fail interrupt and reset. The device also provides dual data pointers (DPTRs) to speed block data memory moves. It can also adjust the speed of off-chip data memory access to between two and nine machine cycles for flexibility in selecting memory and peripherals.

The DS80C320 operating voltage ranges from 4.25V to 5.5V, making it ideal as a high-performance upgrade to existing 5V systems. For applications in which power consumption is critical, the DS80C323 offers the same feature set as the DS80C320, but with 2.7V to 5.5V operation.

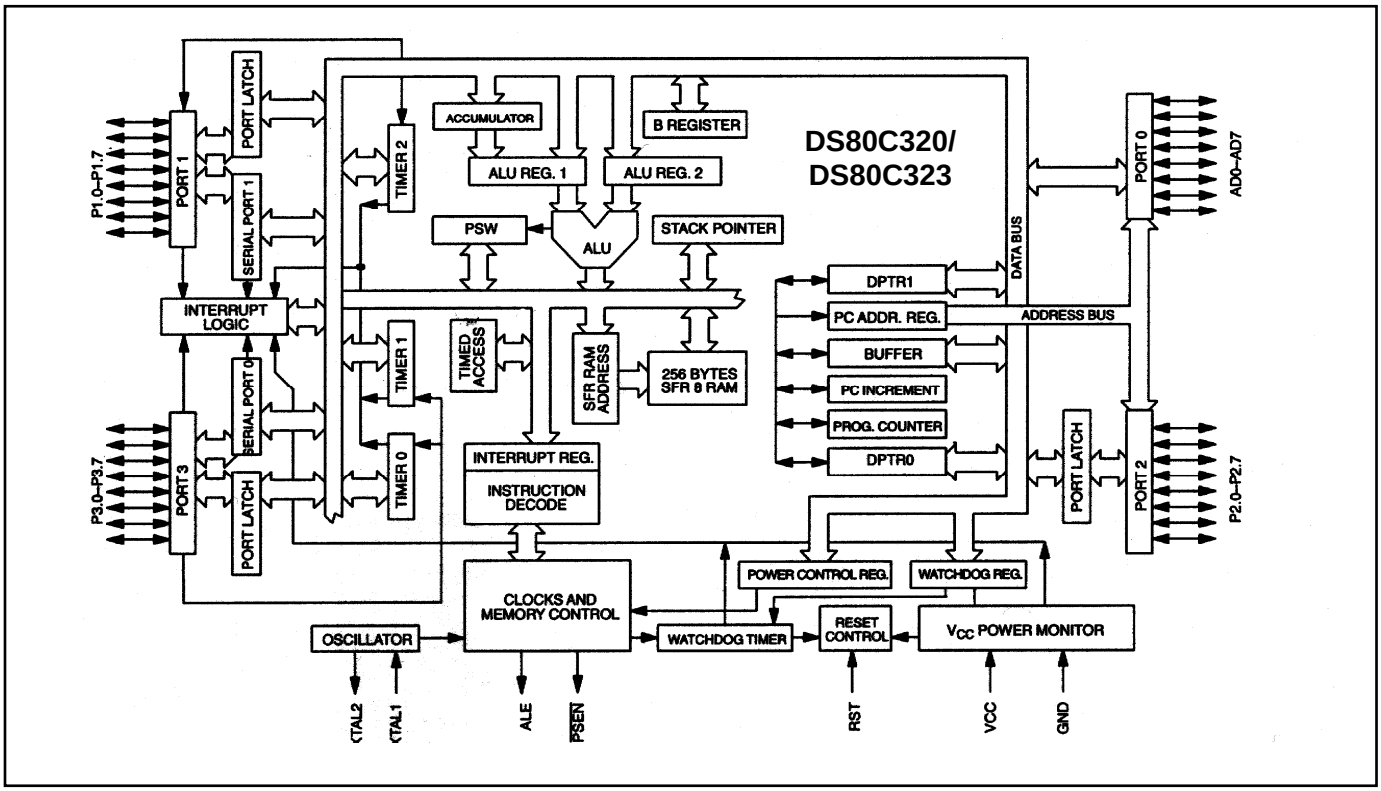
Designers must have two documents to fully use all the features of this device: this data sheet and the *High-Speed Microcontroller User's Guide*, available on our website at www.maxim-ic.com/microcontrollers. Data sheets contain pin descriptions, feature overviews, and electrical specifications, whereas our user's guides contain detailed information about device features and operation.

ORDERING INFORMATION

PART	Pb-FREE/RoHS-COMPLIANT	TEMP RANGE	MAX CLOCK SPEED (MHz)	PIN-PACKAGE
DS80C320-MCG	**DS80C320**-MCG+	0°C to +70°C	25	40 Plastic DIP
DS80C320-QCG	DS80C320-QCG+	0°C to +70°C	25	44 PLCC
DS80C320-ECG	DS80C320-ECG+	0°C to +70°C	25	44 TQFP
DS80C320-MNG	DS80C320-MNG+	-40°C to +85°C	25	40 Plastic DIP
DS80C320-QNG	DS80C320-QNG+	-40°C to +85°C	25	44 PLCC
DS80C320-ENG	DS80C320-ENG+	-40°C to +85°C	25	44 TQFP
DS80C320-MCL	DS80C320-MCL+	0°C to +70°C	33	40 Plastic DIP
DS80C320-QCL	DS80C320-QCL+	0°C to +70°C	33	44 PLCC
DS80C320-ECL	DS80C320-ECL+	0°C to +70°C	33	44 TQFP
DS80C320-MNL	DS80C320-MNL+	-40°C to +85°C	33	40 Plastic DIP
DS80C320-QNL	DS80C320-QNL+	-40°C to +85°C	33	44 PLCC
DS80C320-ENL	DS80C320-ENL+	-40°C to +85°C	33	44 TQFP
DS80C323-MCD	**DS80C323**-MCD+	0°C to +70°C	18	40 Plastic DIP
DS80C323-QCD	DS80C323-QCD+	0°C to +70°C	18	44 PLCC
DS80C323-ECD	DS80C323-ECD+	0°C to +70°C	18	44 TQFP
DS80C323-QND	DS80C323-QND+	-40°C to +85°C	18	44 PLCC
DS80C323-END	DS80C323-END+	-40°C to +85°C	18	44 TQFP

+ Denotes a lead(Pb)-free/RoHS-compliant device.

Figure 1. Block Diagram



PIN DESCRIPTION

PIN			NAME	FUNCTION
DIP	PLCC	TQFP		
40	44	38	V_{CC}	**+5V (+3V for DS80C323)**
20	22, 23	16, 17	GND	**Digital Circuit Ground**
9	10	4	RST	**Reset Input.** The RST input pin contains a Schmitt voltage input to recognize external active-high reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wired OR external reset sources. An RC is ***not*** required for power-up, as the device provides this function internally.
18	20	14	XTAL2	**Crystal Oscillator Pins.** XTAL1 and XTAL2 provide support for parallel-resonant, AT-cut crystals. XTAL1 acts also as an input in the event that an external clock source is used in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
19	21	15	XTAL1	
29	32	26	$\overline{\text{PSEN}}$	**Program Store-Enable Output, Active Low.** This signal is commonly connected to external ROM memory as a chip enable. $\overline{\text{PSEN}}$ provides an active-low pulse width of 2.25 XTAL1 cycles with a period of four XTAL1 cycles. $\overline{\text{PSEN}}$ is driven high when data memory (RAM) is being accessed through the bus and during a reset condition.

PIN DESCRIPTION (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>TQFP</th></tr>
<tr><td>30</td><td>33</td><td>27</td><td>ALE</td><td>Address Latch-Enable Output. This pin functions as a clock to latch the external address LSB from the multiplexed address/data bus. This signal is commonly connected to the latch enable of an external 373 family transparent latch. ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. ALE is forced high when the device is in a reset condition.</td></tr>
<tr><td>39</td><td>43</td><td>37</td><td>AD0</td><td rowspan="8">Port 0, Input/Output. Port 0 is the multiplexed address/data bus. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls, the port transitions to a bidirectional data bus. This bus is used to read external ROM and read/write external RAM memory or peripherals. The Port 0 has no true port latch and cannot be written directly by software. The reset condition of Port 0 is high. No pullup resistors are needed.</td></tr>
<tr><td>38</td><td>42</td><td>36</td><td>AD1</td></tr>
<tr><td>37</td><td>41</td><td>35</td><td>AD2</td></tr>
<tr><td>36</td><td>40</td><td>34</td><td>AD3</td></tr>
<tr><td>35</td><td>39</td><td>33</td><td>AD4</td></tr>
<tr><td>34</td><td>38</td><td>32</td><td>AD5</td></tr>
<tr><td>33</td><td>37</td><td>31</td><td>AD6</td></tr>
<tr><td>32</td><td>36</td><td>30</td><td>AD7</td></tr>
<tr><td>1–8</td><td>2–9</td><td>40–44, 1–3</td><td>P1.0–P1.7</td><td>Port 1, I/O. Port 1 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for Timer 2 I/O, new External Interrupts, and new Serial Port 1. The reset condition of Port 1 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the device will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port once again becomes the output high (and input) state. The alternate modes of Port 1 are outlined as follows:
<table>
<tr><th colspan="3">PIN</th><th rowspan="2">PORT</th><th rowspan="2">ALTERNATE</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>TQFP</th></tr>
<tr><td>1</td><td>2</td><td>40</td><td>P1.0</td><td>T2</td><td>External I/O for Timer/Counter 2</td></tr>
<tr><td>2</td><td>3</td><td>41</td><td>P1.1</td><td>T2EX</td><td>Timer/Counter 2 Capture/Reload Trigger</td></tr>
<tr><td>3</td><td>4</td><td>42</td><td>P1.2</td><td>RXD1</td><td>Serial Port 1 Input</td></tr>
<tr><td>4</td><td>5</td><td>43</td><td>P1.3</td><td>TXD1</td><td>Serial Port 1 Output</td></tr>
<tr><td>5</td><td>6</td><td>44</td><td>P1.4</td><td>INT2</td><td>External Interrupt 2 (Positive-Edge Detect)</td></tr>
<tr><td>6</td><td>7</td><td>1</td><td>P1.5</td><td>$\overline{\text{INT3}}$</td><td>External Interrupt 3 (Negative-Edge Detect)</td></tr>
<tr><td>7</td><td>8</td><td>2</td><td>P1.6</td><td>INT4</td><td>External Interrupt 4 (Positive-Edge Detect)</td></tr>
<tr><td>8</td><td>9</td><td>3</td><td>P1.7</td><td>$\overline{\text{INT5}}$</td><td>External Interrupt 5 (Negative-Edge Detect)</td></tr>
</table>
</td></tr>
</table>

PIN DESCRIPTION (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>TQFP</th></tr>
<tr><td>21</td><td>24</td><td>18</td><td>A8 (P2.0)</td><td rowspan="8">Port 2, Output. Port 2 serves as the MSB for external addressing. P2.7 is A15 and P2.0 is A8. The device will automatically place the MSB of an address on P2 for external ROM and RAM access. Although Port 2 can be accessed like an ordinary I/O port, the value stored on the Port 2 latch will never be seen on the pins (due to memory access). Therefore, writing to Port 2 in software is only useful for the instructions MOVX A, @Ri or MOVX @Ri, A. These instructions use the Port 2 internal latch to supply the external address MSB. In this case, the Port 2 latch value will be supplied as the address information.</td></tr>
<tr><td>22</td><td>25</td><td>19</td><td>A9 (P2.1)</td></tr>
<tr><td>23</td><td>26</td><td>20</td><td>A10 (P2.2)</td></tr>
<tr><td>24</td><td>27</td><td>21</td><td>A11 (P2.3)</td></tr>
<tr><td>25</td><td>28</td><td>22</td><td>A12 (P2.4)</td></tr>
<tr><td>26</td><td>29</td><td>23</td><td>A13 (P2.5)</td></tr>
<tr><td>27</td><td>30</td><td>24</td><td>A14 (P2.6)</td></tr>
<tr><td>28</td><td>31</td><td>25</td><td>A15 (P2.7)</td></tr>
<tr><td>10–17</td><td>11, 13–19</td><td>5, 7–13</td><td>P3.0–P3.7</td><td>Port 3, Input/Output. Port 3 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for External Interrupts, Serial Port 0, Timer 0 & 1 Inputs, $\overline{RD}$ and $\overline{WR}$ strobes. The reset condition of Port 3 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the device will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port once again becomes both the output high and input state. The alternate modes of Port 3 are outlined below:
<table>
<tr><th colspan="3">PIN</th><th rowspan="2">PORT</th><th rowspan="2">ALTERNATE</th><th rowspan="2">MODE</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>TQFP</th></tr>
<tr><td>10</td><td>11</td><td>5</td><td>P3.0</td><td>RXD0</td><td>Serial Port 0 Input</td></tr>
<tr><td>11</td><td>13</td><td>7</td><td>P3.1</td><td>TXD0</td><td>Serial Port 0 Output</td></tr>
<tr><td>12</td><td>14</td><td>8</td><td>P3.2</td><td>$\overline{INT0}$</td><td>External Interrupt 0</td></tr>
<tr><td>13</td><td>15</td><td>9</td><td>P3.3</td><td>$\overline{INT1}$</td><td>External Interrupt 1</td></tr>
<tr><td>14</td><td>16</td><td>10</td><td>P3.4</td><td>T0</td><td>Timer 0 External Input</td></tr>
<tr><td>15</td><td>17</td><td>11</td><td>P3.5</td><td>T1</td><td>Timer 1 External Input</td></tr>
<tr><td>16</td><td>18</td><td>12</td><td>P3.6</td><td>$\overline{WR}$</td><td>External Data Memory Write Strobe</td></tr>
<tr><td>17</td><td>19</td><td>13</td><td>P3.7</td><td>$\overline{RD}$</td><td>External Data Memory Read Strobe</td></tr>
</table></td></tr>
<tr><td>31</td><td>35</td><td>29</td><td>$\overline{EA}$</td><td>External Access, Active-Low Input. This pin must be connected to ground for proper operation.</td></tr>
<tr><td>—</td><td>12, 34, 1*</td><td>6, 28, 39*</td><td>N.C.</td><td>No Connection (Reserved). These pins should not be connected. They are reserved for use with future devices in this family.
*These pins are reserved for additional ground pins on future products.</td></tr>
</table>

STRETCH MEMORY CYCLE

The DS80C320/DS80C323 allow the application software to adjust the speed of data memory access. The microcontroller is capable of performing the MOVX in as little as two instruction cycles. However, this value can be stretched as needed so that both fast memory and slow memory or peripherals can be accessed with no glue logic. Even in high-speed systems, it may not be necessary or desirable to perform data memory access at full speed. In addition, there are a variety of memory-mapped peripherals such as LCD displays or UARTs that are not fast.

The Stretch MOVX is controlled by the Clock Control Register at SFR location 8Eh as described below. This allows the user to select a stretch value between 0 and 7. A Stretch of 0 will result in a two-machine cycle MOVX. A Stretch of 7 will result in a MOVX of nine machine cycles. Software can dynamically change this value depending on the particular memory or peripheral.

On reset, the Stretch value will default to 1, resulting in a three-cycle MOVX. Therefore, RAM access will not be performed at full speed. This is a convenience to existing designs that may not have fast RAM in place. When maximum speed is desired, the software should select a Stretch value of 0. When using very slow RAM or peripherals, a larger stretch value can be selected. Note that this affects data memory only and the only way to slow program memory (ROM) access is to use a slower crystal.

Using a Stretch value between 1 and 7 causes the microcontroller to stretch the read/write strobe and all related timing. This results in a wider read/write strobe allowing more time for memory/peripherals to respond. The timing of the variable speed MOVX is shown in the *Electrical Specifications* section. Note that full speed access is not the reset default case. Table 2 shows the resulting strobe widths for each Stretch value. The memory stretch is implemented using the Clock Control special-function register at SFR location 8Eh. The stretch value is selected using bits CKCON.2–0. In the table, these bits are referred to as M2 through M0. The first stretch (default) allows the use of common 120ns or 150ns RAMs without dramatically lengthening the memory access.

Table 2. Data Memory Cycle Stretch Values

CKCON.2–0			MEMORY CYCLES	$\overline{RD}$ or $\overline{WR}$ STROBE WIDTH IN CLOCKS	STROBE WIDTH TIME AT 25MHz (ns)
MD2	MD1	MD0			
0	0	0	2	2	80
0	0	1	3 (default)	4	160
0	1	0	4	8	320
0	1	1	5	12	480
1	0	0	6	16	640
1	0	1	7	20	800
1	1	0	8	24	960
1	1	1	9	28	1120

DUAL DATA POINTER

Data memory block moves can be accelerated using the Dual Data Pointer (DPTR). The standard 8032 DPTR is a 16-bit value that is used to address off-chip data RAM or peripherals. In the DS80C320/DS80C323, the standard 16-bit data pointer is called DPTR0 and is located at SFR addresses 82h and 83h. These are the standard locations. The new DPTR is located at SFR 84h and 85h and is called DPTR1. The DPTR Select bit (DPS) chooses the active pointer and is located at the LSB of the SFR location 86h. No other bits in register 86h have any effect and are set to 0. The user switches between data pointers by toggling the LSB of register 86h. The increment (INC) instruction is the fastest way to accomplish this. All DPTR-related instructions use the currently selected DPTR for any activity. Therefore only one instruction is required to switch from a source to a destination address. Using the Dual-Data Pointer saves code from needing to save source and destination addresses when doing a block move. Once loaded, the software simply switches between DPTR and 1. The relevant register locations are as follows.

DPL	82h	Low byte original DPTR
DPH	83h	High byte original DPTR
DPL1	84h	Low byte new DPTR
DPH1	85h	High byte new DPTR
DPS	86h	DPTR Select (LSB)

Sample code listed below illustrates the saving from using the dual DPTR. The example program was original code written for an 8051 and requires a total of 1869 DS80C320/DS80C323 machine cycles. This takes 299µs to execute at 25MHz. The new code using the Dual DPTR requires only 1097 machine cycles taking 175.5µs. The Dual DPTR saves 772 machine cycles or 123.5µs for a 64-byte block move. Since each pass through the loop saves 12 machine cycles when compared to the single DPTR approach, larger blocks gain more efficiency using this feature.

64-Byte Block Move without Dual Data Pointer

```
; SH and SL are high and low byte source address.
; DH and DL are high and low byte of destination address.
                                                                    # CYCLES
MOV     R5, #64d            ; NUMBER OF BYTES TO MOVE               2
MOV     DPTR, #SHSL         ; LOAD SOURCE ADDRESS                   3
MOV     R1, #SL             ; SAVE LOW BYTE OF SOURCE               2
MOV     R2, #SH             ; SAVE HIGH BYTE OF SOURCE              2
MOV     R3, #DL             ; SAVE LOW BYTE OF DESTINATION          2
MOV     R4, #DH             ; SAVE HIGH BYTE OF DESTINATION         2

MOVE:
; THIS LOOP IS PERFORMED THE NUMBER OF TIMES LOADED INTO R5, IN THIS EXAMPLE 64

MOVX    A, @DPTR            ; READ SOURCE DATA BYTE                 2
MOV     R1, DPL             ; SAVE NEW SOURCE POINTER               2
MOV     R2, DPH             ;                                       2
MOV     DPL, R3             ; LOAD NEW DESTINATION                  2
MOV     DPH, R4             ;                                       2
MOVX    @DPTR, A            ; WRITE DATA TO DESTINATION             2
INC     DPTR                ; NEXT DESTINATION ADDRESS              3
MOV     R3, DPL             ; SAVE NEW DESTINATION POINTER          2
MOV     R4, DPH             ;                                       2
MOV     DPL, R1             ; GET NEW SOURCE POINTER                2
MOV     DPH, R2             ;                                       2
INC     DPTR                ; NEXT SOURCE ADDRESS                   3
DJNZ    R5, MOVE            ; FINISHED WITH TABLE?                  3
```

64-Byte Block Move with Dual Data Pointer

```
; SH and SL are high and low byte source address.
; DH and DL are high and low byte of destination address.
; DPS is the data pointer select. Reset condition is DPS=0, DPTR0 is selected.
                                                                    # CYCLES
EQU     DPS, #86h           ; TELL ASSEMBLER ABOUT DPS

MOV     R5, #64             ; NUMBER OF BYTES TO MOVE               2
MOV     DPTR, #DHDL         ; LOAD DESTINATION ADDRESS              3
INC     DPS                 ; CHANGE ACTIVE DPTR                    2
MOV     DPTR, #SHSL         ; LOAD SOURCE ADDRESS                   2

MOVE:
; THIS LOOP IS PERFORMED THE NUMBER OF TIMES LOADED INTO R5, IN THIS EXAMPLE 64

MOVX    A, @DPTR            ; READ SOURCE DATA BYTE                 2
INC     DPS                 ; CHANGE DPTR TO DESTINATION            2
MOVX    @DPTR, A            ; WRITE DATA TO DESTINATION             2
INC     DPTR                ; NEXT DESTINATION ADDRESS              3
INC     DPS                 ; CHANGE DATA POINTER TO SOURCE         2
INC     DPTR                ; NEXT SOURCE ADDRESS                   3
DJNZ    R5, MOVE            ; FINISHED WITH TABLE?                  3
```

PERIPHERAL OVERVIEW

Peripherals in the DS80C320/DS80C323 are accessed using the SFRs. The devices provide several of the most commonly needed peripheral functions in microcomputer-based systems. These functions are new to the 80C32 family and include a second serial port, power-fail reset, power-fail interrupt, and a programmable watchdog timer. These are briefly described in the following paragraphs. More details are available in the *High-Speed Microcontroller User's Guide*.

SERIAL PORTS

The DS80C320/DS80C323 provide a serial port (UART) that is identical to the 80C32. Many applications require serial communication with multiple devices. Therefore, a second hardware serial port is provided that is a full duplicate of the standard one. It optionally uses pins P1.2 (RXD1) and P1.3 (TXD1). This port has duplicate control functions included in new SFR locations. The second serial port operates in a comparable manner with the first. Both can operate simultaneously but can be at different baud rates.

The second serial port has similar control registers (SCON1 at C0h, SBUF1 at C1h) to the original. One difference is that for timer-based baud rates, the original serial port can use Timer 1 or Timer 2 to generate baud rates. This is selected via SFR bits. The new serial port can only use Timer 1.

TIMER-RATE CONTROL

One important difference exists between the DS80C320/DS80C323 and 80C32 regarding timers. The original 80C32 used a 12 clock-per-cycle scheme for timers and consequently for some serial baud rates (depending on the mode). The DS80C320/DS80C323 architecture normally runs using 4 clocks per cycle. However, in the area of timers, it will default to a 12 clock-per-cycle scheme on a reset. This allows existing code with real-time dependencies such as baud rates to operate properly. If an application needs higher speed timers or serial baud rates, the timers can be set to run at the 4-clock rate.

The Clock Control register (CKCON - 8Eh) determines these timer speeds. When the relevant CKCON bit is a logic 1, the device uses 4 clocks per cycle to generate timer speeds. When the control bit is set to a 0, the device uses 12 clocks for timer speeds. The reset condition is a 0. CKCON.5 selects the speed of Timer 2. CKCON.4 selects Timer 1 and CKCON.3 selects Timer 0. Note that unless a user desires very fast timing, it is unnecessary to alter these bits. Note that the timer controls are independent.

POWER-FAIL RESET

The DS80C320/DS80C323 incorporate a precision bandgap voltage reference to determine when V_{CC} is out of tolerance. While powering up, internal circuits will hold the device in a reset state until V_{CC} rises above the V_{RST} reset threshold. Once V_{CC} is above this level, the oscillator will begin running. An internal reset circuit will then count 65,536 clocks to allow time for power and the oscillator to stabilize. The microcontroller will then exit the reset condition. No external components are needed to generate a power on reset. During power-down or during a severe power glitch, as V_{CC} falls below V_{RST}, the microcontroller will also generate its own reset. It will hold the reset condition as long as power remains below the threshold. This reset will occur automatically, needing no action from the user or from the software. See the *Electrical Specifications* section for the exact value of V_{RST}.

POWER-FAIL INTERRUPT

The same reference that generates a precision reset threshold can also generate an optional early warning Power-fail Interrupt (PFI). When enabled by the application software, this interrupt always has the highest priority. On detecting that the V_{CC} has dropped below V_{PFW} and that the PFI is enabled, the processor will vector to ROM address 0033h. The PFI enable is located in the Watchdog Control SFR (WDCON to D8h). Setting WDCON.5 to logic 1 will enable the PFI. The application software can also read a flag at WDCON.4. This bit is set when a PFI condition has occurred. The flag is independent of the interrupt enable and software must manually clear it.

WATCHDOG TIMER

For applications that cannot afford to run out of control, the DS80C320/DS80C323 incorporate a programmable watchdog timer circuit. The watchdog timer circuit resets the microcontroller if software fails to reset the watchdog before the selected time interval has elapsed. The user selects one of four timeout values. After enabling the watchdog, software must reset the timer prior to expiration of the interval, or the CPU will be reset. Both the Watchdog Enable and the Watchdog Reset bits are protected by a "Timed Access" circuit. This prevents accidentally clearing the watchdog. Timeout values are precise since they are related to the crystal frequency as shown in Table 3. For reference, the time periods at 25MHz are also shown.

The watchdog timer also provides a useful option for systems that may not require a reset. If enabled, then 512 clocks before giving a reset, the watchdog will give an interrupt. The interrupt can also serve as a convenient time-base generator, or be used to wake-up the processor from Idle mode. The watchdog function is controlled in the Clock Control (CKCON to 8Eh), Watchdog Control (WDCON to D8h), and Extended Interrupt Enable (EIE to E8h) SFRs. CKCON.7 and CKCON.6 are called WD1 and WD0, respectively, and are used to select the watchdog timeout period as shown in Table 3.

Table 3. Watchdog Timeout Values

WD1	WD0	INTERRUPT TIMEOUT	TIME (at 25MHz)	RESET TIMEOUT	TIME (at 25MHz)
0	0	2^{17} clocks	5.243ms	2^{17} + 512 clocks	5.263ms
0	1	2^{20} clocks	41.94ms	2^{20} + 512 clocks	41.96ms
1	0	2^{23} clocks	335.54ms	2^{23} + 512 clocks	335.56ms
1	1	2^{26} clocks	2684.35ms	2^{26} + 512 clocks	2684.38ms

As Table 3 shows, the watchdog timer uses the crystal frequency as a time base. A user selects one of four counter values to determine the timeout. These clock counter lengths are 2^{17} = 131,072 clocks; 2^{20} = 1,048,576; 2^{23} = 8,388,608 clocks; or 2^{26} = 67,108,864 clocks. The times shown in Table 4 are with

POWER MANAGEMENT

The DS80C320/DS80C323 provide the standard Idle and power-down (Stop) modes that are available on the standard 80C32. However, the device has enhancements that make these modes more useful, and allow more power saving.

The Idle mode is invoked by setting the LSB of the Power Control register (PCON to 87h). Idle will leave internal clocks, serial port and timer running. No memory access will be performed so power is dramatically reduced. Since clocks are running, the Idle power consumption is related to crystal frequency. It should be approximately one-half the operational power. The CPU can exit the Idle state with any interrupt or a reset.

The power-down or Stop mode is invoked by setting the PCON.1 bit. Stop mode is a lower power state than Idle since it turns off all internal clocking. The I_{CC} of a standard Stop mode is approximately 1 µA but is specified in the *Electrical Specifications* section. The CPU will exit Stop mode from an external interrupt or a reset condition.

Note that internally generated interrupts (timer, serial port, watchdog) are not useful in Idle or Stop since they require clocking activity.

IDLE MODE ENHANCEMENTS

A simple enhancement to Idle mode makes it substantially more useful. The innovation involves not the Idle mode itself, but the watchdog timer. As mentioned above, the Watchdog Timer provides an optional interrupt capability. This interrupt can provide a periodic interval timer to bring the DS80C320/DS80C323 out of Idle mode. This can be useful even if the Watchdog is not normally used. By enabling the Watchdog Timer and its interrupt prior to invoking Idle, a user can periodically come out of Idle perform an operation, then return to Idle until the next operation. This will lower the overall power consumption. When using the Watchdog Interrupt to cancel the Idle state, make sure to restart the Watchdog Timer or it will cause a reset.

STOP MODE ENHANCEMENTS

The DS80C320/DS80C323 provide two enhancements to the Stop mode. As documented above, the device provides a bandgap reference to determine Power-fail Interrupt and Reset thresholds. The default state is that the bandgap reference is off when Stop mode is invoked. This allows the extremely low power state mentioned above. A user can optionally choose to have the bandgap enabled during Stop mode. This means that PFI and power-fail reset will be activated and are valid means for leaving Stop mode.

In Stop mode with the bandgap on, I_{CC} will be approximately 50µA compared with 1µA with the bandgap off. If a user does not require a Power-fail Reset or Interrupt while in Stop mode, the bandgap can remain turned off. Note that only the most power sensitive applications should turn off the bandgap, as this results in an uncontrolled power-down condition.

The control of the bandgap reference is located in the Extended Interrupt Flag register (EXIF to 91h). Setting BGS (EXIF.0) to a 1 will leave the bandgap reference enabled during Stop mode. The default or reset condition is with the bit at a logic 0. This results in the bandgap being turned off during Stop mode. Note that this bit has no control of the reference during full power or Idle modes. Be aware that the DS80C320 and DS80C323 require that the reset watchdog timer bit (RWT;WDCON.0) be set

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground……..-0.3V to +6.0V
Operating Temperature Range……-40°C to +85°C
Storage Temperature Range……..-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS—DS80C320

(V_{CC} = 4.5V to 5.5V, T_A = -40°C to +85°C.)

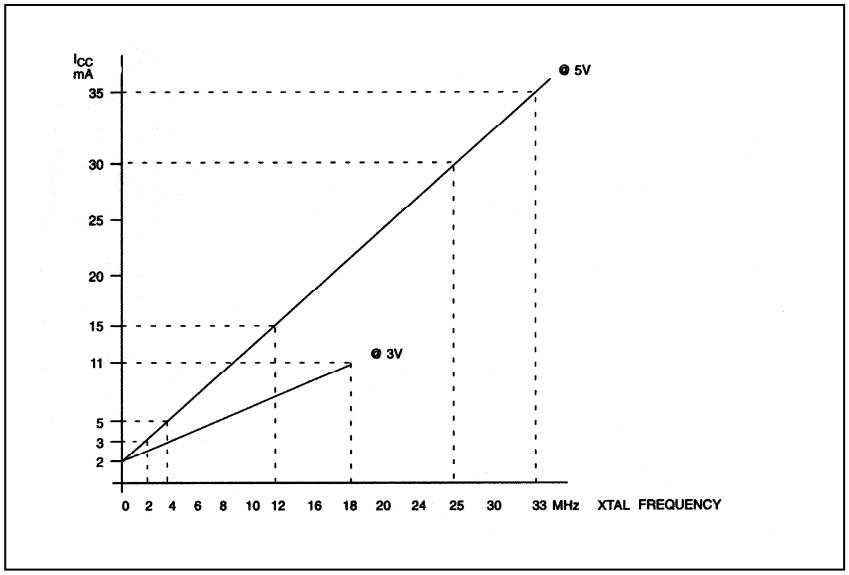
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Power-Fail Warning Voltage	V_{PFW}	4.25	4.38	4.55	V	1
Minimum Operating Voltage	V_{RST}	4.0	4.1	4.25	V	1, 12
Supply Current Active Mode at 25MHz	I_{CC}		30	45	mA	2
Supply Current Idle Mode at 25MHz	I_{IDLE}		15	25	mA	3
Supply Current Active Mode at 33MHz	I_{CC}		35		mA	2
Supply Current Idle Mode at 33MHz	I_{IDLE}		20		mA	3
Supply Current Stop Mode, Bandgap Reference Disabled	I_{STOP}		0.01	1	µA	4
Supply Current Stop Mode, Bandgap Reference Enabled	I_{SPBG}		50	80	µA	4, 10
Input Low Level	V_{IL}	-0.3		+0.8	V	1
Input High Level (Except XTAL1 and RST)	V_{IH1}	2.0		V_{CC} + 0.3	V	1
Input High Level XTAL1 and RST	V_{IH2}	3.5		V_{CC} + 0.3	V	1
Output-Low Voltage Ports 1, 3 at I_{OL} = 1.6mA	V_{OL1}			0.45	V	1
Output-Low Voltage Ports 0, 2, ALE, $\overline{PSEN}$ at I_{OL} = 3.2mA	V_{OL2}			0.45	V	1, 5
Output-High Voltage Ports 1, 3, ALE, $\overline{PSEN}$ at I_{OH} = -50µA	V_{OH1}	2.4			V	1, 6
Output High Voltage Ports 1, 3 at I_{OH} = -1.5mA	V_{OH2}	2.4			V	1, 7
Output-High Voltage Ports 0, 2, ALE, $\overline{PSEN}$ at I_{OH} = -8mA	V_{OH3}	2.4			V	1, 5
Input Low Current Ports 1, 3 at 0.45V	I_{IL}			-55	µA	11
Transition Current from 1 to 0 Ports 1, 3 at 2V	I_{TL}			-650	µA	8
Input Leakage Port 0, Bus Mode	I_L	-300		+300	µA	9
RST Pulldown Resistance	R_{RST}	50		170	kΩ	

NOTES FOR DS80C320 DC ELECTRICAL CHARACTERISTICS

All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested.

1. All voltages are referenced to ground.
2. Active current is measured with a 25MHz clock source driving XTAL1, V_{CC} = RST = 5.5V, all other pins disconnected.
3. Idle mode current is measured with a 25MHz clock source driving XTAL1, V_{CC} = 5.5V, RST at ground, all other pins disconnected.
4. Stop mode current measured with XTAL1 and RST grounded, V_{CC} = 5.5V, all other pins disconnected.
5. When addressing external memory. This specification only applies to the first clock cycle following transition.
6. RST = V_{CC}. This condition mimics operation of pins in I/O mode.
7. During a 0-to-1 transition, a one-shot drives the ports hard for two clock cycles. This measurement reflects port in transition mode.
8. Ports 1 and 3 source transition current when being pulled down externally. It reaches its maximum at approximately 2V.
9. $0.45<V_{IN}<V_{CC}$. Not a high-impedance input. This port is a weak address holding latch because Port 0 is dedicated as an address bus on the DS80C320. Peak current occurs near the input transition point of the latch, approximately 2V.
10. Over the industrial temperature range, this specification has a maximum value of 200µA.
11. This is the current required from an external circuit to hold a logic low level on an I/O pin while the corresponding port latch bit is set to 1. This is only the current required to *hold* the low level; transitions from 1 to 0 on an I/O pin will also have to overcome the transition current.
12. Device operating range is 4.5V to 5.5V; however, device is tested to 4.0V to ensure proper operation at minimum V_{RST}.

TYPICAL I_{CC} vs. FREQUENCY



AC CHARACTERISTICS—DS80C320

PARAMETER		SYMBOL	33MHz		VARIABLE CLOCK		UNITS
			MIN	MAX	MIN	MAX	
Oscillator Frequency	External Oscillator	$1/t_{CLCL}$	0	33	0	33	MHz
	External Crystal		1	33	1	33	
ALE Pulse Width		t_{LHLL}	34		$1.5t_{CLCL}$-11		ns
Port 0 Address Valid to ALE Low		t_{AVLL}	4		$0.5t_{CLCL}$-11		ns
Address Hold After ALE Low		t_{LLAX1}	2	(Note 5)	$0.25t_{CLCL}$-5	(Note 5)	ns
Address Hold After ALE Low for MOVX $\overline{WR}$		t_{LLAX2}	6		$0.5t_{CLCL}$-9		ns
ALE Low to Valid Instruction In		t_{LLIV}		49		$2.5t_{CLCL}$-27	ns
ALE Low to $\overline{PSEN}$ Low		t_{LLPL}	0.5		$0.25t_{CLCL}$-7		ns
$\overline{PSEN}$ Pulse Width		t_{PLPH}	61		$2.25t_{CLCL}$-7		ns
$\overline{PSEN}$ Low to Valid Instruction In		t_{PLIV}		48		$2.25t_{CLCL}$-21	ns
Input Instruction Hold After $\overline{PSEN}$		t_{PXIX}	0		0		ns
Input Instruction Float After $\overline{PSEN}$		t_{PXIZ}		25		t_{CLCL}-5	ns
Port 0 Address to Valid Instruction In		t_{AVIV1}		64		$3t_{CLCL}$-27	ns
Port 2 Address to Valid Instruction In		t_{AVIV2}		73		$3.5t_{CLCL}$-33	ns
$\overline{PSEN}$ Low to Address Float		t_{PLAZ}		(Note 5)		(Note 5)	ns

NOTES FOR DS80C320 AC ELECTRICAL CHARACTERISTICS

All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested. AC electrical characteristics assume 50% duty cycle for the oscillator, oscillator frequency > 16MHz, and are not 100% tested, but are guaranteed by design.

1. All signals rated over operating temperature at 33MHz.
2. All signals characterized with load capacitance of 80pF except Port 0, ALE, $\overline{PSEN}$, $\overline{RD}$ and $\overline{WR}$ at 100pF. Note that loading should be approximately equal for valid timing.
3. Interfacing to memory devices with float times (turn off times) over 30ns may cause contention. This will not damage the parts but will cause an increase in operating current.
4. Specifications assume a 50% duty cycle for the oscillator. Port 2 timing will change with the duty cycle variations.
5. Address is held in a weak latch until over driven by external memory.

MOVX CHARACTERISTICS—DS80C320

PARAMETER	SYMBOL	VARIABLE CLOCK		UNITS	STRETCH
		MIN	MAX		
$\overline{RD}$ Pulse Width	t_{RLRH}	$2t_{CLCL}$-11		ns	t_{MCS}=0
		t_{MCS}-11			t_{MCS}>0
$\overline{WR}$ Pulse Width	t_{WLWH}	$2t_{CLCL}$-11		ns	t_{MCS}=0
		t_{MCS}-11			t_{MCS}>0
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2t_{CLCL}$-25	ns	t_{MCS}=0
			t_{MCS}-25		t_{MCS}>0
Data Hold After Read	t_{RHDX}	0		ns	
Data Float After Read	t_{RHDZ}		t_{CLCL}-5	ns	t_{MCS}=0
			$2t_{CLCL}$-5		t_{MCS}>0
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL}$-27	ns	t_{MCS}=0
			$1.5t_{CLCL}$-28+t_{MCS}		t_{MCS}>0
Port 0 Address to Valid Data In	t_{AVDV1}		$3t_{CLCL}$-27	ns	t_{MCS}=0
			$2t_{CLCL}$-31+t_{MCS}		t_{MCS}>0
Port 2 Address to Valid Data In	t_{AVDV2}		$3.5t_{CLCL}$-32	ns	t_{MCS}=0
			$2.5t_{CLCL}$-34+t_{MCS}		t_{MCS}>0
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL}$-8	$0.5t_{CLCL}$+6	ns	t_{MCS}=0
		$1.5t_{CLCL}$-7	$1.5t_{CLCL}$+8		t_{MCS}>0
Port 0 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	t_{CLCL}-11		ns	t_{MCS}=0
		$2t_{CLCL}$-10			t_{MCS}>0
Port 2 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL}$-9		ns	t_{MCS}=0
		$2.5t_{CLCL}$-13			t_{MCS}>0
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-9		ns	t_{MCS}=0
		t_{CLCL}-10			t_{MCS}>0
Data Hold After Write	t_{WHQX}	t_{CLCL}-12		ns	t_{MCS}=0
		$2t_{CLCL}$-7			t_{MCS}>0
$\overline{RD}$ Low to Address Float	t_{RLAZ}		(Note 5)	ns	
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{WHLH}	0	10	ns	t_{MCS}=0
		t_{CLCL}-5	t_{CLCL}+11		t_{MCS}>0

Note: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.

M2	M1	M0	MOVX CYCLES	t_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles (default)	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Clock High Time	t_{CHCX}	10			ns
Clock Low Time	t_{CLCX}	10			ns
Clock Rise Time	t_{CLCH}			5	ns
Clock Fall Time	t_{CHCL}			5	ns

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

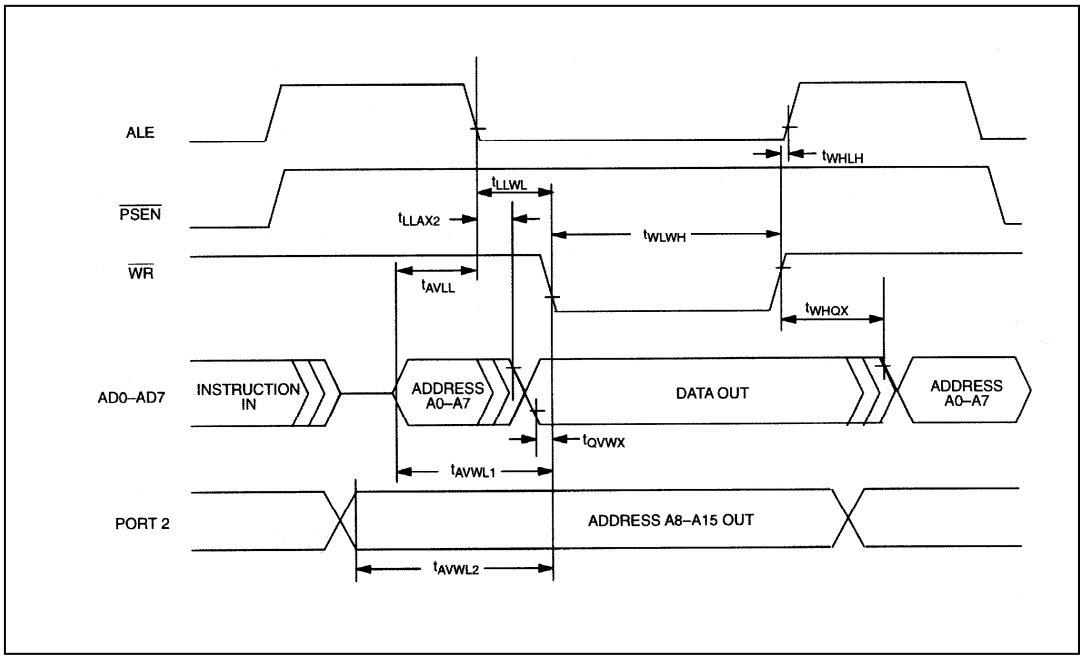
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Port Clock Cycle Time	t_{XLXL}	SM2 = 0; 12 clocks per cycle		$12t_{CLCL}$		ns
		SM2 = 1; 4 clocks per cycle		$4t_{CLCL}$		
Output Data Setup to Clock Rising Edge	t_{QVXH}	SM2 = 0 12 clocks per cycle		$10t_{CLCL}$		ns
		SM2 = 1; 4 clocks per cycle		$3t_{CLCL}$		
Output Data Hold from Clock Rising	t_{XHQX}	SM2 = 0 12 clocks per cycle		$2t_{CLCL}$		ns
		SM2 = 1; 4 clocks per cycle		t_{CLCL}		
Input Data Hold After Clock Rising	t_{XHDX}	SM2 = 0; 12 clocks per cycle		t_{CLCL}		ns
		SM2 = 1; 4 clocks per cycle		t_{CLCL}		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0; 12 clocks per cycle		$11t_{CLCL}$		ns
		SM2 = 1 4 clocks per cycle		$2t_{CLCL}$		

EXPLANATION OF AC SYMBOLS

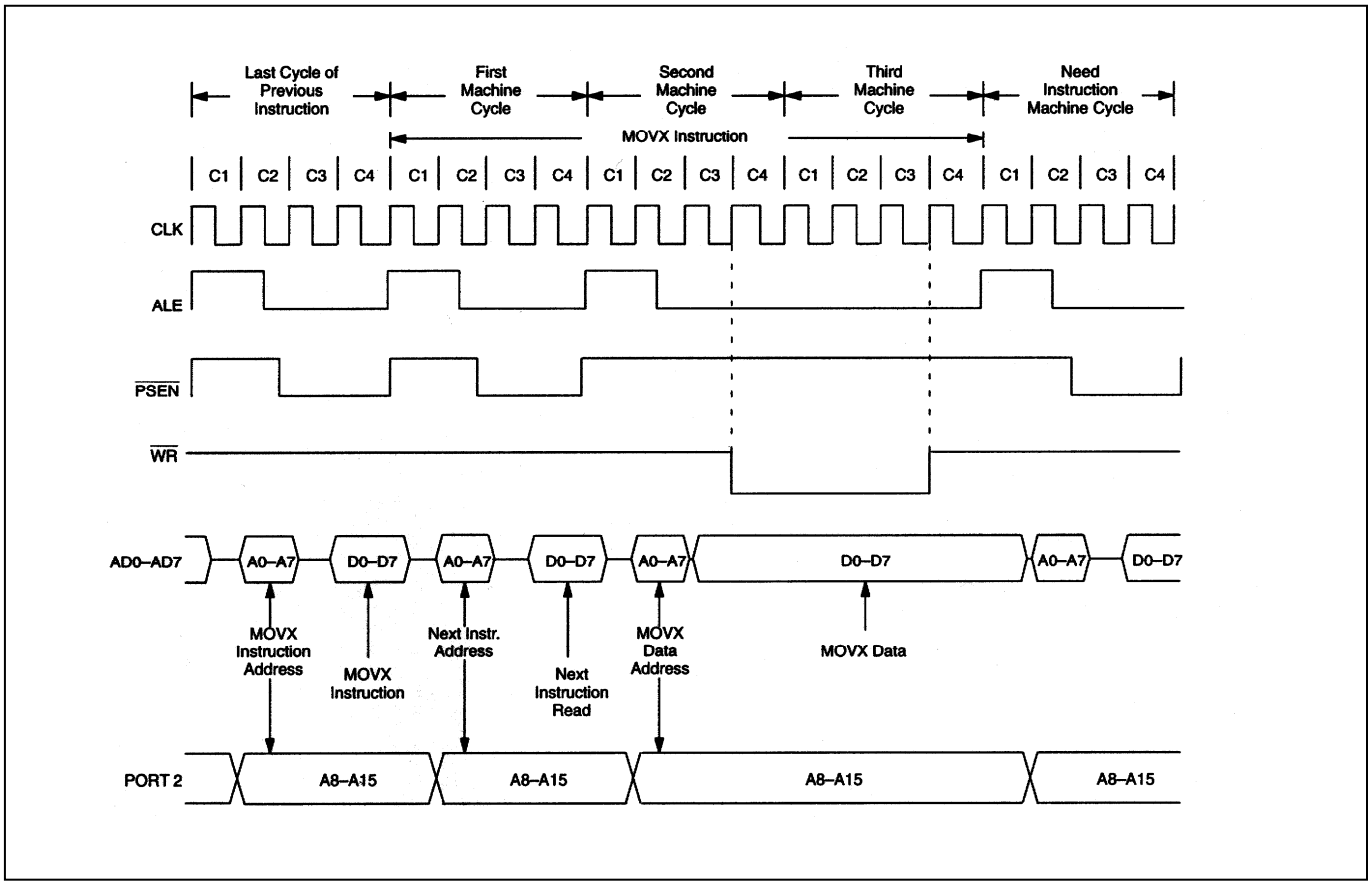
In an effort to remain compatible with the original 8051 family, this device specifies the same parameter as such devices, using the same symbols. For completeness, the following is an explanation of the symbols.

t	Time
A	Address
C	Clock
D	Input data
H	Logic level high
L	Logic level low
I	Instruction
P	$\overline{\text{PSEN}}$
Q	Output data
R	$\overline{\text{RD}}$ signal
V	Valid
W	$\overline{\text{WR}}$ signal
X	No longer a valid logic level
Z	Tri-state

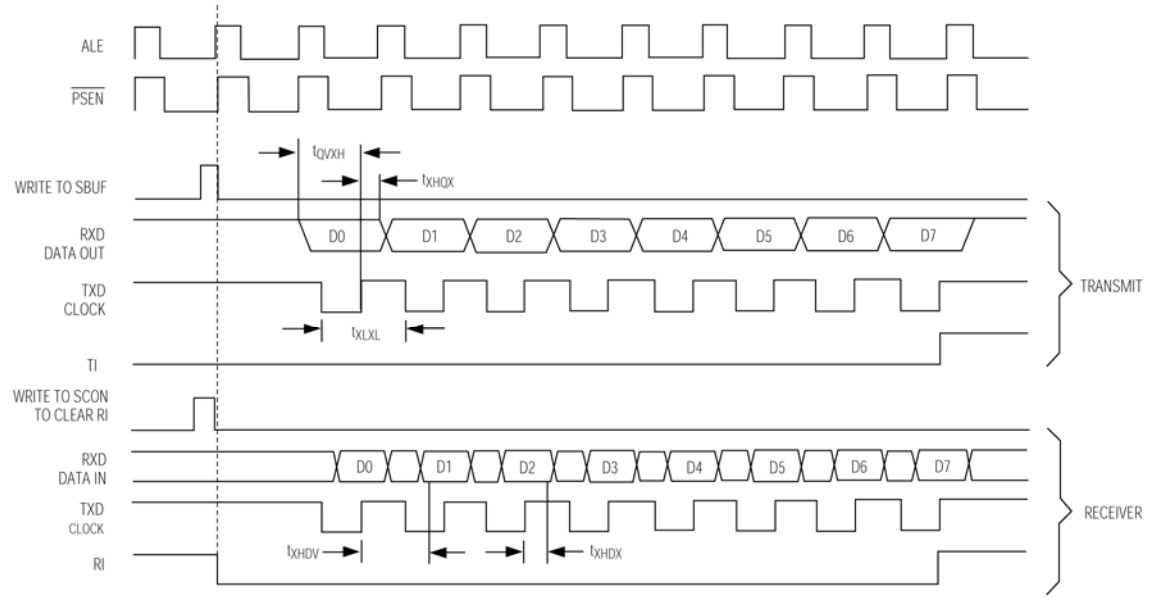
DATA MEMORY WRITE CYCLE



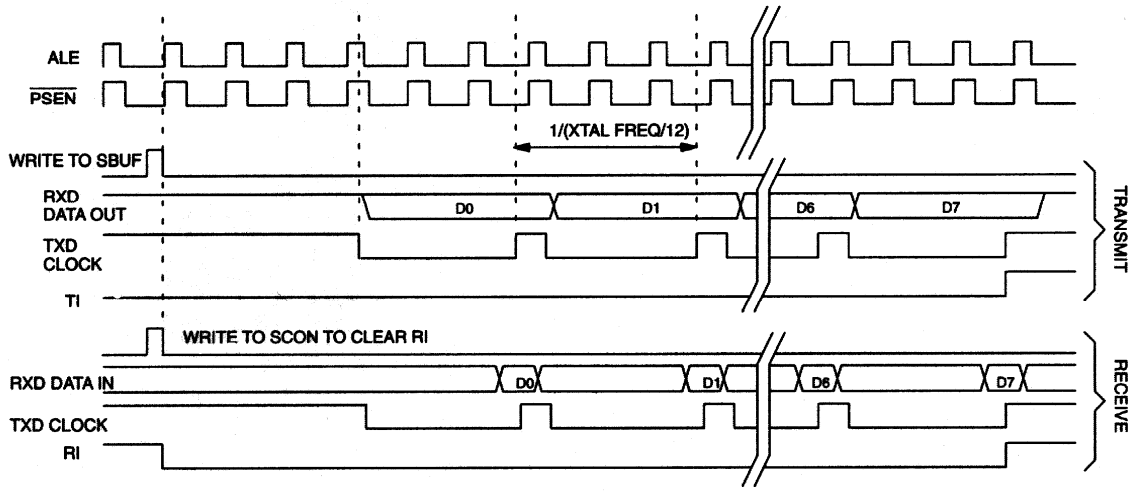
DATA MEMORY WRITE WITH STRETCH = 1



SERIAL PORT MODE 0 TIMING

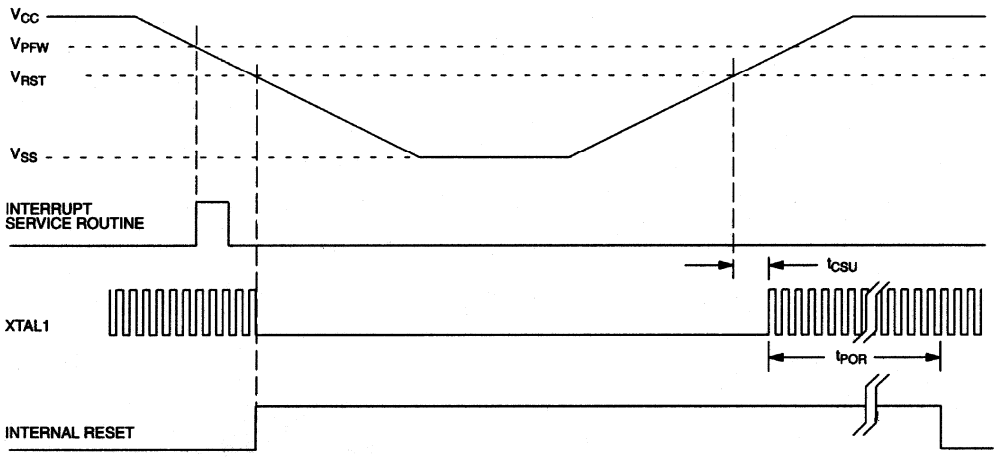


SERIAL PORT 0 (SYNCHRONOUS MODE)
HIGH SPEED OPERATION SM2 = 1 ≥ TXD CLOCK = XTAL/4



SERIAL PORT 0 (SYNCHRONOUS MODE)
SM2 = 0 ≥ TXD CLOCK = XTAL/12

POWER-CYCLE TIMING



PACKAGE INFORMATION

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
44 TQFP	C44+2	**21-0293**
44 MQFP	M44+10	**21-0269**
44 MQFP	M44+5	**21-0826**
40 PDIP	P40+1	**21-0044**
44 PLCC	Q44+1	**21-0049**

DATA SHEET REVISION SUMMARY

The following represent the key differences between the 101006 and 070505 version of the DS80C320/DS80C323 data sheet. Please review this summary carefully.

1. Deleted DS80C323-MND from Ordering Information table (page 2). Device was never manufactured.

The following represent the key differences between the 070505 and 051804 version of the DS80C320/DS80C323 data sheet. Please review this summary carefully.

2. Added Pb-free/RoHS-compliant part numbers to Ordering Information table.
3. Deleted the "A" from the IPC/JEDEC J-STD-020 specification in the Absolute Maximum Ratings.

The following represent the key differences between the 051804 and the 112299 version of the DS80C320/DS80C323 data sheet. Please review this summary carefully.

1. Removed "Preliminary" status as a result of final characterization.
2. Added industrial temperature DS80C323 devices to ordering information.
3. Updated soldering temperature specification to reflect JEDEC standards.
4. Updated the following DS80C323 AC timing parameters with final characterization data: t_{LHLL}, t_{LLAX1}, t_{LLAX2}, t_{LLAX2}, t_{LLIV}, t_{LLPL}, t_{PLIV}, t_{AVIV1}, t_{RLDV}, t_{RHDZ}, t_{LLDV}, t_{AVDV1}, t_{AVDV2}, t_{LLWL}, t_{AVWL1}, t_{AVWL2}, t_{QVWX}, t_{WHQX}, t_{WHLH}.
5. Updated the following DS80C320 AC timing parameters with final characterization data: t_{WHQX}, t_{LHLL}, t_{LLAX2}, tLLDV, t_{AVDV1}, t_{LLWL}, t_{AVWL1}, t_{AVWL2}.
6. Added note advising the need to reset watchdog timer before setting the Stop bit.
7. Added note clarifying drive strength of P0, P2, ALE, $\overline{PSEN}$.
8. Obsoleted DS80C320 25MHz AC timing tables; merged into 33MHz AC timing tables.
9. Corrected Serial Port Mode 0 Timing diagrams to show correct order of D6, D7.

The following represent the key differences between the 041896 and the 052799 version of the DS80C320 data sheet. Please review this summary carefully.

1. Corrected V_{CC} pin description to show DS80C323 operation at +3V.
2. Corrected Timed Access description to show three-cycle window.
3. Modified absolute Maximum Ratings for any pin relative to around, V_{CC} relative to ground.
4. Changed minimum oscillator frequency to 1MHz when using external crystal.
5. Clarified that t_{POR} begins when XTAL1 reaches V_{IH2}.

The following represent the key differences between the 103196 and the 041896 version of the DS80C320 data sheet. Please review this summary carefully.

1. Updated DS80C320 25MHz AC Characteristics.

The following represent the key differences between the 041895 and the 031096 version of the DS80C320 data sheet. Please review this summary carefully.

1. Remove Port 0, Port 2 from V_{OH1} specification (PCN B60802).
2. V_{OH1} test specification clarified (RST = V_{CC}).
3. Add t_{AVWL2} marking to External Memory Read Cycle figure.
4. Correct TQFP drawing to read 44-pin TQFP.
5. Rotate page 1 TQFP illustration to match assembly specifications.

The following represent the key differences between the 031096 and the 052296 version of the DS80C320 data sheet. Please review this summary carefully.

1. Added *Data Sheet Revision Summary* section.

The following represent the key differences between 05/23/96 and 05/22/96 version of the DS80C320 data sheet and between 05/23/96 and 03/27/95 version of the DS80C323 data sheet. Please review this summary carefully.

DS80C320:

1. Add DS80C323 Characteristics.
2. Change DS80C320 V_{PFW} specification from 4.5V to 4.55V (PCN E62802).
3. Update DS80C320 33MHz AC Characteristics.

DS80C323:

1. Delete Data Sheet. Contents moved to DS80C320/DS80C323.

DATA SHEET REVISION SUMMARY (continued)

The following represent the key differences between the 05/22/96 and the 10/21/97 version of the DS80C320 data sheet. Please review this summary carefully.

DS80C320

1. Added note to clarify I_{IL} specification.
2. Added note to clarify AC timing conditions.
3. Corrected erroneous t_{QVXL} label on figure "Serial Port Mode 0 Timing" to read t_{QVXH}.
4. Added note to prevent accidental corruption of Watchdog Timer count while changing counter length.

DS80C323

1. Added note to clarify I_{IL} specification.
2. Remove port 2 from V_{OH1} specification, add port 3.
3. I_{OH} for V_{OH3} specification changed from -3mA to -2mA.
4. Added note to clarify AC timing conditions.

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