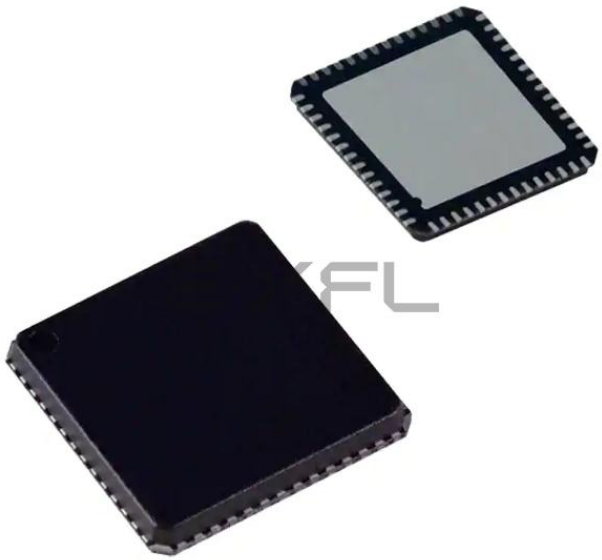

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| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 8052 |
| Core Size | 8-Bit |
| Speed | 12.58MHz |
| Connectivity | EBI/EMI, I²C, SPI, UART/USART |
| Peripherals | POR, PSM, Temp Sensor, WDT |
| Number of I/O | 34 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 640 x 8 |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.25V |
| Data Converters | A/D 3x16b, 4x24b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 56-VFQFN Exposed Pad, CSP |
| Supplier Device Package | 56-LFCSP-VQ (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/aduc824bcpz |

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- AN-644: Frequency Measurement Using Timer 2 on a MicroConverter ® (uC013)
- AN-645: Interfacing an HD44780 Character LCD to a MicroConverter ® (uC014)
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- UG-041: ADuC8xx Evaluation Kit Getting Started User Guide

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- Integrated Route Taken to Pulse Oximetry

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| Parameter | ADuC824BS | Test Conditions/Comments | Unit |
|---|---|---|---|
| TRANSDUCER BURNOUT CURRENT SOURCES | | | |
| AIN+ Current | –100 | AIN+ is the Selected Positive Input to the Primary ADC | nA typ |
| AIN– Current | +100 | AIN– is the Selected Negative Input to the Auxiliary ADC | nA typ |
| Initial Tolerance @ 25°C Drift | ±10 | | % typ |
| Drift | 0.03 | | %/°C typ |
| EXCITATION CURRENT SOURCES | | | |
| Output Current | –200 | Available from Each Current Source | µA typ |
| Initial Tolerance @ 25°C | ±10 | | % typ |
| Drift | 200 | | ppm/°C typ |
| Initial Current Matching @ 25°C | ±1 | Matching Between Both Current Sources | % typ |
| Drift Matching | 20 | | ppm/°C typ |
| Line Regulation ($AV_{DD}$) | 1 | $AV_{DD}$ = 5 V + 5% | µA/V typ |
| Load Regulation | 0.1 | | µA/V typ |
| Output Compliance | $AV_{DD}$ – 0.6<br>AGND | | V max<br>min |
| LOGIC INPUTS | | | |
| All Inputs Except SCLOCK, RESET, and XTAL1 | | | |
| $V_{INL}$, Input Low Voltage | 0.8 | $DV_{DD}$ = 5 V | V max |
| | 0.4 | $DV_{DD}$ = 3 V | V max |
| $V_{INH}$, Input High Voltage | 2.0 | | V min |
| SCLOCK and RESET Only (Schmitt-Triggered Inputs)[2] | | | |
| $V_{T+}$ | 1.3/3 | $DV_{DD}$ = 5 V | V min/V max |
| | 0.95/2.5 | $DV_{DD}$ = 3 V | V min/V max |
| $V_{T-}$ | 0.8/1.4 | $DV_{DD}$ = 5 V | V min/V max |
| | 0.4/1.1 | $DV_{DD}$ = 3 V | V min/V max |
| $V_{T+} - V_{T-}$ | 0.3/0.85 | $DV_{DD}$ = 5 V | V min/V max |
| | 0.3/0.85 | $DV_{DD}$ = 3 V | V min/V max |
| Input Currents | | | |
| Port 0, P1.2–P1.7, $\overline{EA}$ | ±10 | $V_{IN}$ = 0 V or $V_{DD}$ | µA max |
| SCLOCK, SDATA/MOSI, MISO, $\overline{SS}$[12] | –10 min, –40 max | $V_{IN}$ = 0 V, $DV_{DD}$ = 5 V, Internal Pull-Up | µA min/µA max |
| | ±10 | $V_{IN}$ = $V_{DD}$, $DV_{DD}$ = 5 V | µA max |
| RESET | ±10 | $V_{IN}$ = 0 V, $DV_{DD}$ = 5 V | µA max |
| | 35 min, 105 max | $V_{IN}$ = $V_{DD}$, $DV_{DD}$ = 5 V, Internal Pull-Down | µA min/µA max |
| P1.0, P1.1, Ports 2 and 3 | ±10 | $V_{IN}$ = $V_{DD}$, $DV_{DD}$ = 5 V | µA max |
| | –180 | $V_{IN}$ = 2 V, $DV_{DD}$ = 5 V | µA min |
| | –660 | | µA max |
| | –20 | $V_{IN}$ = 450 mV, $DV_{DD}$ = 5 V | µA min |
| | –75 | | µA max |
| Input Capacitance | 5 | All Digital Inputs | pF typ |
| CRYSTAL OSCILLATOR (XTAL1 AND XTAL2) | | | |
| Logic Inputs, XTAL1 Only | | | |
| $V_{INL}$, Input Low Voltage | 0.8 | $DV_{DD}$ = 5 V | V max |
| | 0.4 | $DV_{DD}$ = 3 V | V max |
| $V_{INH}$, Input High Voltage | 3.5 | $DV_{DD}$ = 5 V | V min |
| | 2.5 | $DV_{DD}$ = 3 V | V min |
| XTAL1 Input Capacitance | 18 | | pF typ |
| XTAL2 Output Capacitance | 18 | | pF typ |

| Parameter | | Min | Typ | Max | Unit | Figure |
|---|---|---|---|---|---|---|
| SPI MASTER MODE TIMING (CPHA = 0) | | | | | | |
| $t_{SL}$ | SCLOCK Low Pulsewidth* | | 630 | | ns | 9 |
| $t_{SH}$ | SCLOCK High Pulsewidth* | | 630 | | ns | 9 |
| $t_{DAV}$ | Data Output Valid after SCLOCK Edge | | | 50 | ns | 9 |
| $t_{DOSU}$ | Data Output Setup before SCLOCK Edge | | | 150 | ns | 9 |
| $t_{DSU}$ | Data Input Setup Time before SCLOCK Edge | 100 | | | ns | 9 |
| $t_{DHD}$ | Data Input Hold Time after SCLOCK Edge | 100 | | | ns | 9 |
| $t_{DF}$ | Data Output Fall Time | | 10 | 25 | ns | 9 |
| $t_{DR}$ | Data Output Rise Time | | 10 | 25 | ns | 9 |
| $t_{SR}$ | SCLOCK Rise Time | | 10 | 25 | ns | 9 |
| $t_{SF}$ | SCLOCK Fall Time | | 10 | 25 | ns | 9 |

*Characterized under the following conditions:
a. Core clock divider bits CD2, CD1, and CD0 bits in PLLCON SFR set to 0, 1, and 1 respectively, i.e., core clock frequency = 1.57 MHz and
b. SPI bit-rate selection bits SPR1 and SPR0 bits in SPICON SFR set to 0 and 0 respectively.

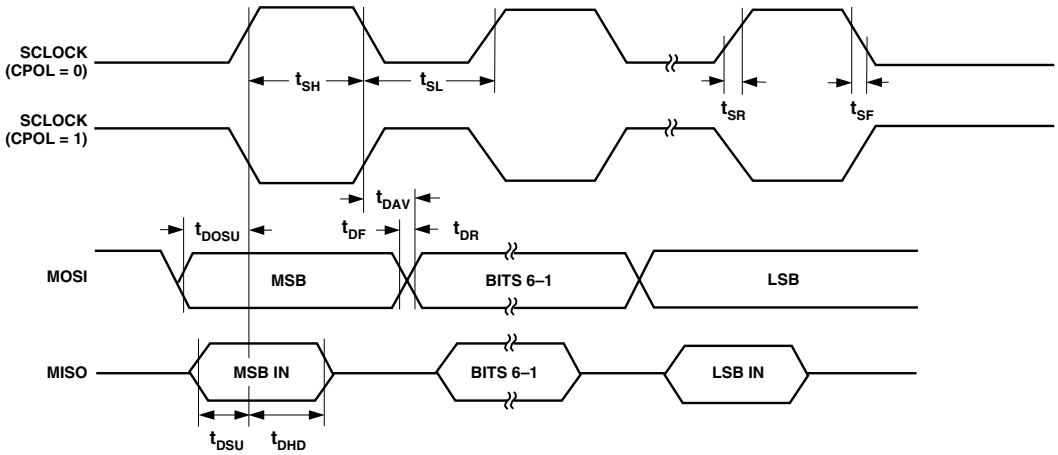


*Figure 9. SPI Master Mode Timing (CPHA = 0)*

| Parameter | | Min | Typ | Max | Unit | Figure |
|---|---|---|---|---|---|---|
| SPI SLAVE MODE TIMING (CPHA = 0) | | | | | | |
| $t_{SS}$ | $\overline{SS}$ to SCLOCK Edge | 0 | | | ns | 11 |
| $t_{SL}$ | SCLOCK Low Pulsewidth | | 330 | | ns | 11 |
| $t_{SH}$ | SCLOCK High Pulsewidth | | 330 | | ns | 11 |
| $t_{DAV}$ | Data Output Valid after SCLOCK Edge | | | 50 | ns | 11 |
| $t_{DSU}$ | Data Input Setup Time before SCLOCK Edge | 100 | | | ns | 11 |
| $t_{DHD}$ | Data Input Hold Time after SCLOCK Edge | 100 | | | ns | 11 |
| $t_{DF}$ | Data Output Fall Time | | 10 | 25 | ns | 11 |
| $t_{DR}$ | Data Output Rise Time | | 10 | 25 | ns | 11 |
| $t_{SR}$ | SCLOCK Rise Time | | 10 | 25 | ns | 11 |
| $t_{SF}$ | SCLOCK Fall Time | | 10 | 25 | ns | 11 |
| $t_{SSR}$ | $\overline{SS}$ to SCLOCK Edge | | | 50 | ns | 11 |
| $t_{DOSS}$ | Data Output Valid after $\overline{SS}$ Edge | | | 20 | ns | 11 |
| $t_{SFS}$ | $\overline{SS}$ High after SCLOCK Edge | 0 | | | ns | 11 |

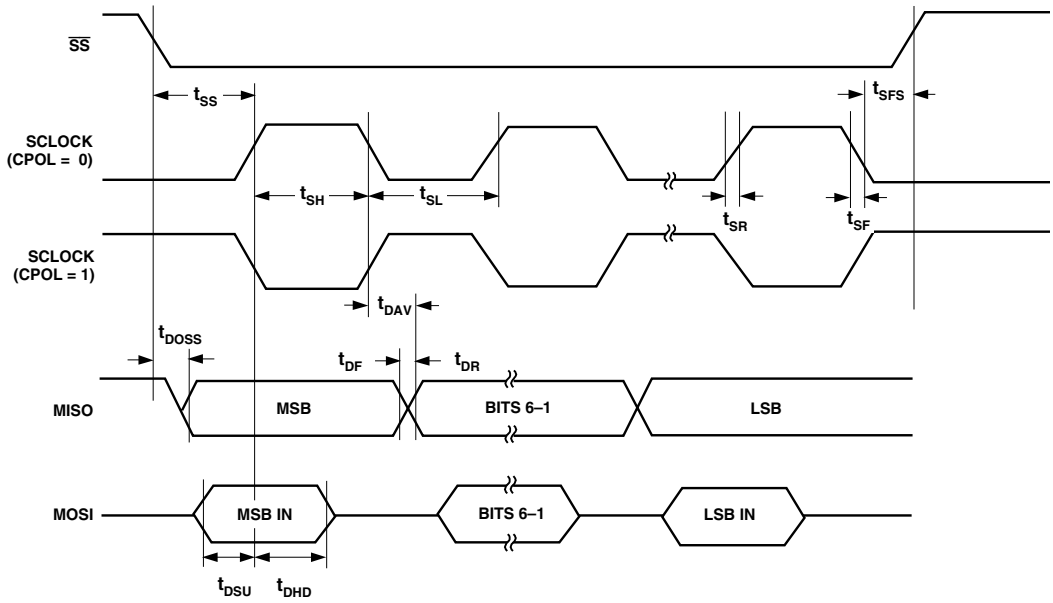


*Figure 11. SPI Slave Mode Timing (CPHA = 0)*

**ADCMODE (ADC Mode Register)**
Used to control the operational mode of both ADCs.

| | |
|---|---|
| SFR Address | D1H |
| Power-On Default Value | 00H |
| Bit Addressable | No |

| — | — | ADC0EN | ADC1EN | — | MD2 | MD1 | MD0 |
|---|---|---|---|---|---|---|---|

**Table IV. ADCMODE SFR Bit Designations**

| Bit | Name | Description |
|---|---|---|
| 7 | — | Reserved for Future Use |
| 6 | — | Reserved for Future Use |
| 5 | ADC0EN | Primary ADC Enable<br>*Set* by the user to enable the Primary ADC and place it in the mode selected in MD2–MD0 below<br>*Cleared* by the user to place the Primary ADC in power-down mode. |
| 4 | ADC1EN | Auxiliary ADC Enable<br>*Set* by the user to enable the Auxiliary ADC and place it in the mode selected in MD2–MD0 below<br>*Cleared* by the user to place the Auxiliary ADC in power-down mode. |
| 3 | — | Reserved for Future Use |
| 2 | MD2 | Primary and Auxiliary ADC Mode bits. |
| 1 | MD1 | These bits select the operational mode of the enabled ADC as follows: |
| 0 | MD0 | MD2 MD1 MD0<br>0 0 0 Power-Down Mode (Power-On Default)<br>0 0 1 Idle Mode<br>In Idle Mode the ADC filter and modulator are held in a reset state although the modulator clocks are still provided.<br>0 1 0 Single Conversion Mode<br>In Single Conversion Mode, a single conversion is performed on the enabled ADC. On completion of the conversion, the ADC data registers (ADC0H/M/L and/or ADC1H/L) are updated, the relevant flags in the ADCSTAT SFR are written, and power-down is re-entered with the MD2–MD0 accordingly being written to 000.<br>0 1 1 Continuous Conversion<br>In continuous conversion mode the ADC data registers are regularly updated at the selected update rate (see SF register)<br>1 0 0 Internal Zero-Scale Calibration<br>Internal short is automatically connected to the enabled ADC(s)<br>1 0 1 Internal Full-Scale Calibration<br>Internal or External $V_{REF}$ (as determined by XREF0 and XREF1 bits in ADC0/1CON) is automatically connected to the ADC input for this calibration.<br>1 1 0 System Zero-Scale Calibration<br>User should connect system zero-scale input to the ADC input pins as selected by CH1/CH0 and ACH1/ACH0 bits in the ADC0/1CON register.<br>1 1 1 System Full-Scale Calibration<br>User should connect system full-scale input to the ADC input pins as selected by CH1/CH0 and ACH1/ACH0 bits in the ADC0/1CON register. |

NOTES
1. Any change to the MD bits will immediately reset both ADCs. A write to the MD2–0 bits with no change is also treated as a reset. (See exception to this in Note 3 below.)
2. If ADC0CON is written when AD0EN = 1, or if AD0EN is changed from 0 to 1, then both ADCs are also immediately reset. In other words, the Primary ADC is given priority over the Auxiliary ADC and any change requested on the primary ADC is immediately responded to.
3. On the other hand, if ADC1CON is written or if ADC1EN is changed from 0 to 1, only the Auxiliary ADC is reset. For example, if the Primary ADC is continuously converting when the Auxiliary ADC change or enable occurs, the primary ADC continues undisturbed. Rather than allow the Auxiliary ADC to operate with a phase difference from the primary ADC, the Auxiliary ADC will fall into step with the outputs of the primary ADC. The result is that the first conversion time for the Auxiliary ADC will be delayed up to three outputs while the Auxiliary ADC update rate is synchronized to the Primary ADC.
4. Once ADCMODE has been written with a calibration mode, the RDY0/1 bits (ADCSTAT) are immediately reset and the calibration commences. On completion, the appropriate calibration registers are written, the relevant bits in ADCSTAT are written, and the MD2–0 bits are reset to 000 to indicate the ADC is back in power-down mode.
5. Any calibration request of the Auxiliary ADC while the temperature sensor is selected will fail to complete. Although the RDY1 bit will be set at the end of the calibration cycle, no update of the calibration SFRs will take place and the ERR1 bit will be set.
6. Calibrations are performed at maximum SF (see SF SFR) value guaranteeing optimum calibration operation.

**ADC0CON (Primary ADC Control Register)**

Used to configure the Primary ADC for range, channel selection, external Ref enable, and unipolar or bipolar coding.

| | |
|---|---|
| SFR Address | D2H |
| Power-On Default Value | 07H |
| Bit Addressable | No |

| — | XREF0 | CH1 | CH0 | UNI0 | RN2 | RN1 | RN0 |
|---|---|---|---|---|---|---|---|

**Table V. ADC0CON SFR Bit Designations**

| Bit | Name | Description |
|---|---|---|
| 7 | — | Reserved for Future Use |
| 6 | XREF0 | Primary ADC External Reference Select Bit<br>*Set* by user to enable the Primary ADC to use the external reference via REFIN(+)/REFIN(–).<br>*Cleared* by user to enable the Primary ADC to use the internal bandgap reference ($V_{REF}$ = 1.25 V). |
| 5 | CH1 | Primary ADC Channel Selection Bits |
| 4 | CH0 | Written by the user to select the differential input pairs used by the Primary ADC as follows:<br>CH1 CH0 Positive Input Negative Input<br>0 0 AIN1 AIN2<br>0 1 AIN3 AIN4<br>1 0 AIN2 AIN2 (Internal Short)<br>1 1 AIN3 AIN2 |
| 3 | UNI0 | Primary ADC Unipolar Bit.<br>*Set* by user to enable unipolar coding, i.e., zero differential input will result in 000000 hex output.<br>*Cleared* by user to enable bipolar coding, zero differential input will result in 800000 hex output. |
| 2 | RN2 | Primary ADC Range Bits |
| 1 | RN1 | Written by the user to select the Primary ADC input range as follows: |
| 0 | RN0 | RN2 RN1 RN0 Selected Primary ADC Input Range ($V_{REF}$ = 2.5 V)<br>0 0 0 ±20 mV<br>0 0 1 ±40 mV<br>0 1 0 ±80 mV<br>0 1 1 ±160 mV<br>1 0 0 ±320 mV<br>1 0 1 ±640 mV<br>1 1 0 ±1.28 V<br>1 1 1 ±2.56 V |

**ADC1CON (Auxiliary ADC Control Register)**
Used to configure the Auxiliary ADC for channel selection, external Ref enable and unipolar or bipolar coding. It should be noted that the Auxiliary ADC only operates on a fixed input range of $\pm V_{REF}$.

SFR Address D3H
Power-On Default Value 00H
Bit Addressable No

| — | XREF1 | ACH1 | ACH0 | UNI1 | — | — | — |
|---|---|---|---|---|---|---|---|

**Table VI. ADC1CON SFR Bit Designations**

| Bit | Name | Description |
|---|---|---|
| 7 | — | Reserved for Future Use |
| 6 | XREF1 | Auxiliary ADC External Reference Bit<br>*Set* by user to enable the Auxiliary ADC to use the external reference via REFIN(+)/REFIN(–).<br>*Cleared* by user to enable the Auxiliary ADC to use the internal bandgap reference. |
| 5 | ACH1 | Auxiliary ADC Channel Selection Bits |
| 4 | ACH0 | Written by the user to select the single-ended input pins used to drive the Auxiliary ADC as follows:<br>ACH1 ACH0 Positive Input Negative Input<br>0 0 AIN3 AGND<br>0 1 AIN4 AGND<br>1 0 Temp Sensor* AGND (Temp. Sensor routed to the ADC input)<br>1 1 AIN5 AGND |
| 3 | UNI1 | Auxiliary ADC Unipolar Bit<br>*Set* by user to enable unipolar coding, i.e., zero input will result in 0000 hex output.<br>*Cleared* by user to enable bipolar coding, zero input will result in 8000 hex output. |
| 2 | — | Reserved for Future Use |
| 1 | — | Reserved for Future Use |
| 0 | — | Reserved for Future Use |

*NOTES
1. When the temperature sensor is selected, user code must select internal reference via XREF1 bit above and clear the UNI1 bit (ADC1CON.3) to select bipolar coding.
2. The temperature sensor is factory calibrated to yield conversion results 8000H at 0°C.
3. A +1°C change in temperature will result in a +1 LSB change in the ADC1H register ADC conversion result.

**SF (Sinc Filter Register)**
The number in this register sets the decimation factor and thus the output update rate for the Primary and Auxiliary ADCs. This SFR cannot be written by user software while either ADC is active. The update rate applies to both Primary and Auxiliary ADCs and is calculated as follows:

$$f_{ADC} = \frac{1}{3} \times \frac{1}{8.SF} \times f_{MOD}$$

Where: $f_{ADC}$ = ADC Output Update Rate
$f_{MOD}$ = Modulator Clock Frequency = 32.768 kHz
$SF$ = Decimal Value of SF Register

The allowable range for SF is 0Dhex to FFhex. Examples of SF values and corresponding conversion update rate ($f_{ADC}$) and conversion time ($t_{ADC}$) are shown in Table VII, the power-on default value for the SF register is 45hex, resulting in a default ADC update rate of just under 20 Hz. Both ADC inputs are chopped to minimize offset errors, which means that the settling time for a single conversion or the time to a first conversion result in continuous conversion mode is $2 \times t_{ADC}$. As mentioned earlier, all calibration cycles will be carried out automatically with a maximum, i.e., FFhex, SF value to ensure optimum calibration performance. Once a calibration cycle has completed, the value in the SF register will be that programmed by user software.

**Table VII. SF SFR Bit Designations**

| SF(dec) | SF(hex) | $f_{ADC}$(Hz) | $t_{ADC}$(ms) |
|---|---|---|---|
| 13 | 0D | 105.3 | 9.52 |
| 69 | 45 | 19.79 | 50.34 |
| 255 | FF | 5.35 | 186.77 |

The absolute input voltage range on the auxiliary ADC is restricted to between AGND – 30 mV to AVDD + 30 mV. The slightly negative absolute input voltage limit does allow the possibility of monitoring small signal bipolar signals using the single-ended auxiliary ADC front end.

**Programmable Gain Amplifier**

The output from the buffer on the primary ADC is applied to the input of the on-chip programmable gain amplifier (PGA). The PGA can be programmed through eight different unipolar input ranges and bipolar ranges. The PGA gain range is programmed via the range bits in the ADC0CON SFR. With the external reference select bit set in the ADC0CON SFR and an external 2.5 V reference, the unipolar ranges are 0 mV to 20 mV, 0 mV to 40 mV, 0 mV to 80 mV, 0 mV to 160 mV, 0 mV to 320 mV, 0 mV to 640 mV, 0 V to 1.28 V, and 0 to 2.56 V, while the bipolar ranges are ±20 mV, ±40 mV, ±80 mV, ±160 mV, ±320 mV, ±640 mV, ±1.28 V, and ±2.56 V. These are the nominal ranges that should appear at the input to the on-chip PGA. An ADC range matching specification of 2 μV (typ) across all ranges means that calibration need only be carried out at a single gain range and does not have to be repeated when the PGA gain range is changed.

Typical matching across ranges is shown in Figure 20 below. Here, the primary ADC is configured in bipolar mode with an external 2.5 V reference, while just greater than 19 mV is forced on its inputs. The ADC continuously converts the DC input voltage at an update rate of 5.35 Hz, i.e., SF = FFhex. In total, 800 conversion results are gathered. The first 100 results are gathered with the primary ADC operating in the ±20 mV range. The ADC range is then switched to ±40 mV and 100 more conversion results are gathered, and so on until the last group of 100 samples are gathered with the ADC configured in the ±2.56 V range. From Figure 20, The variation in the sample mean through each range, i.e., the range matching, is seen to be of the order of 2 μV.

The auxiliary ADC does not incorporate a PGA and is configured for a fixed single input range of 0 to $V_{REF}$.

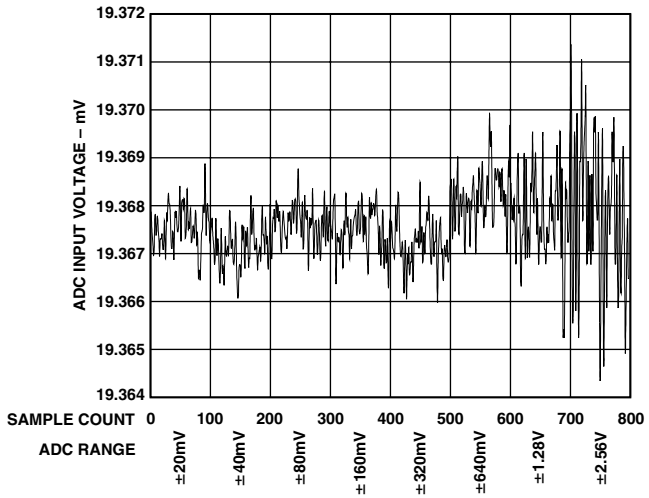


*Figure 20. Primary ADC Range Matching*

**Bipolar/Unipolar Inputs**

The analog inputs on the ADuC824 can accept either unipolar or bipolar input voltage ranges. Bipolar input ranges do not imply that the part can handle negative voltages with respect to system AGND.

Unipolar and bipolar signals on the AIN(+) input on the primary ADC are referenced to the voltage on the respective AIN(–) input. For example, if AIN(–) is 2.5 V and the primary ADC is configured for an analog input range of 0 mV to 20 mV, the input voltage range on the AIN(+) input is 2.5 V to 2.52 V. If AIN(–) is 2.5 V and the ADuC824 is configured for an analog input range of 1.28 V, the analog input range on the AIN(+) input is 1.22 V to 3.78 V (i.e., 2.5 V ± 1.28 V).

As mentioned earlier, the auxiliary ADC input is a single-ended input with respect to the system AGND. In this context a bipolar signal on the auxiliary ADC can only span 30 mV negative with respect to AGND before violating the voltage input limits for this ADC.

Bipolar or unipolar options are chosen by programming the Primary and Auxiliary Unipolar enable bits in the ADC0CON and ADC1CON SFRs respectively. This programs the relevant ADC for either unipolar or bipolar operation. Programming for either unipolar or bipolar operation does not change any of the input signal conditioning; it simply changes the data output coding and the points on the transfer function where calibrations occur. When an ADC is configured for unipolar operation, the output coding is natural (straight) binary with a zero differential input voltage resulting in a code of 000 . . . 000, a midscale voltage resulting in a code of 100 . . . 000, and a full-scale input voltage resulting in a code of 111 . . . 111. When an ADC is configured for bipolar operation, the coding is offset binary with a negative full-scale voltage resulting in a code of 000 . . . 000, a zero differential voltage resulting in a code of 100 . . . 000, and a positive full-scale voltage resulting in a code of 111 . . . 111.

**Burnout Currents**

The primary ADC on the ADuC824 contains two 100 nA constant current generators, one sourcing current from AVDD to AIN(+), and one sinking from AIN(–) to AGND. The currents are switched to the selected analog input pair. Both currents are either on or off, depending on the Burnout Current Enable (BO) bit in the ICON SFR (see Table VIII). These currents can be used to verify that an external transducer is still operational before attempting to take measurements on that channel. Once the burnout currents are turned on, they will flow in the external transducer circuit, and a measurement of the input voltage on the analog input channel can be taken. If the resultant voltage measured is full-scale, this indicates that the transducer has gone open-circuit. If the voltage measured is 0 V, it indicates that the transducer has short circuited. For normal operation, these burnout currents are turned off by writing a 0 to the BO bit in the ICON SFR. The current sources work over the normal absolute input voltage range specifications.

**ON-CHIP PLL**

The ADuC824 is intended for use with a 32.768 kHz watch crystal. A PLL locks onto a multiple (384) of this to provide a stable 12.582912 MHz clock for the system. The core can operate at this frequency or at binary submultiples of it to allow power saving in cases where maximum core performance is not required. The default core clock is the PLL clock divided by 8 or 1.572864 MHz. The ADC clocks are also derived from the PLL clock, with the modulator rate being the same as the crystal oscillator frequency. The above choice of frequencies ensures that the modulators and the core will be synchronous, regardless of the core clock rate. The PLL control register is PLLCON.

**PLLCON** **PLL Control Register**

| | |
|---|---|
| SFR Address | D7H |
| Power-On Default Value | 03H |
| Bit Addressable | No |

| OSC_PD | LOCK | — | $\overline{\text{LTEA}}$ | FINT | CD2 | CD1 | CD0 |
|---|---|---|---|---|---|---|---|

**Table XV. PLLCON SFR Bit Designations**

| Bit | Name | Description |
|---|---|---|
| 7 | OSC_PD | Oscillator Power-down Bit<br>*Set* by user to halt the 32 kHz oscillator in power-down mode.<br>*Cleared* by user to enable the 32 kHz oscillator in power-down mode.<br>This feature allows the TIC to continue counting even in power-down mode. |
| 6 | LOCK | PLL Lock Bit<br>This is a read only bit.<br>*Set* automatically at power-on to indicate the PLL loop is correctly tracking the crystal clock. If the external crystal becomes subsequently disconnected the PLL will rail and the core will halt.<br>*Cleared* automatically at power-on to indicate the PLL is not correctly tracking the crystal clock. This may be due to the absence of a crystal clock or an external crystal at power-on. In this mode, the PLL output can be 12.58 MHz ± 20%. |
| 5 | — | Reserved for future use; should be written with '0.' |
| 4 | $\overline{\text{LTEA}}$ | Reading this bit returns the state of the external $\overline{\text{EA}}$ pin latched at reset or power-on. |
| 3 | FINT | Fast Interrupt Response Bit<br>*Set* by user enabling the response to any interrupt to be executed at the fastest core clock frequency, regardless of the configuration of the CD2–0 bits (see below). Once user code has returned from an interrupt, the core resumes code execution at the core clock selected by the CD2–0 bits.<br>*Cleared* by user to disable the fast interrupt response feature. |
| 2 | CD2 | CPU (Core Clock) Divider Bits |
| 1 | CD1 | This number determines the frequency at which the microcontroller core will operate. |
| 0 | CD0 | CD2 CD1 CD0 Core Clock Frequency (MHz)<br>0 0 0 12.582912<br>0 0 1 6.291456<br>0 1 0 3.145728<br>0 1 1 1.572864 (Default Core Clock Frequency)<br>1 0 0 0.786432<br>1 0 1 0.393216<br>1 1 0 0.196608<br>1 1 1 0.098304 |

**TIME INTERVAL COUNTER (TIC)**

A time interval counter is provided on-chip for counting longer intervals than the standard 8051-compatible timers are capable of. The TIC is capable of timeout intervals ranging from 1/128th second to 255 hours. Furthermore, this counter is clocked by the crystal oscillator rather than the PLL and thus has the ability to remain active in power-down mode and time long power-down intervals. This has obvious applications for remote battery-powered sensors where regular widely spaced readings are required.

Six SFRs are associated with the time interval counter, TIMECON being its control register. Depending on the configuration of the IT0 and IT1 bits in TIMECON, the selected time counter register overflow will clock the interval counter. When this counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt if enabled (See IEIP2 SFR description under Interrupt System later in this data sheet.) If the ADuC824 is in power-down mode, again with TIC interrupt enabled, the TII bit will wake up the device and resume code execution by vectoring directly to the TIC interrupt service vector address at 0053 hex. The TIC-related SFRs are described in Table XVI. Note also that the timebase SFRs can be written initially with the current time, the TIC can then be controlled and accessed by user software. In effect, this facilitates the implementation of a real-time clock. A block diagram of the TIC is shown in Figure 32.

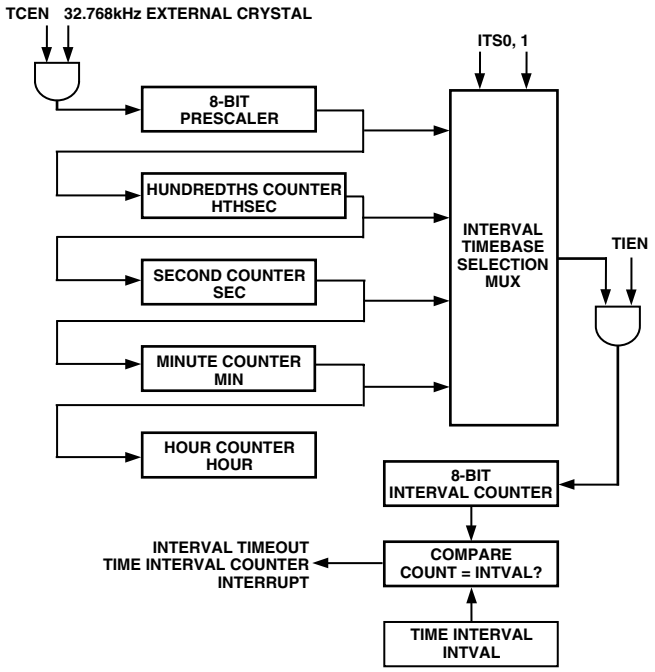


*Figure 32. TIC, Simplified Block Diagram*

**TIMECON** **TIC Control Register**
SFR Address A1H
Power-On Default Value 00H
Bit Addressable No

| — | — | ITS1 | ITS0 | STI | TII | TIEN | ICEN |
|---|---|---|---|---|---|---|---|

**Table XVI. TIMECON SFR Bit Designations**

| Bit | Name | Description |
|---|---|---|
| 7 | — | Reserved for Future Use |
| 6 | — | Reserved for Future Use. For future product code compatibility this bit should be written as a '1.' |
| 5 | ITS1 | Interval Timebase Selection Bits. |
| 4 | ITS0 | Written by user to determine the interval counter update rate.<br>ITS1 ITS0 Interval Timebase<br>0 0 1/128 Second<br>0 1 Seconds<br>1 0 Minutes<br>1 1 Hours |
| 3 | STI | Single Time Interval Bit<br>*Set* by user to generate a single interval timeout. If set, a timeout will clear the TIEN bit.<br>*Cleared* by user to allow the interval counter to be automatically reloaded and start counting again at each interval timeout. |
| 2 | TII | TIC Interrupt Bit<br>*Set* when the 8-bit Interval Counter matches the value in the INTVAL SFR.<br>*Cleared* by user software. |
| 1 | TIEN | Time Interval Enable Bit<br>*Set* by user to enable the 8-bit time interval counter.<br>*Cleared* by user to disable and clear the contents of the interval counter. |
| 0 | TCEN | Time Clock Enable Bit<br>*Set* by user to enable the time clock to the time interval counters.<br>*Cleared* by user to disable the clock to the time interval counters and clear the time interval SFRs. The time registers (HTHSEC, SEC, MIN and HOUR) can be written while TCEN is low. |

**SERIAL PERIPHERAL INTERFACE**

The ADuC824 integrates a complete hardware Serial Peripheral Interface (SPI) interface on-chip. SPI is an industry standard synchronous serial interface that allows eight bits of data to be synchronously transmitted and received simultaneously, i.e., full duplex. It should be noted that the SPI physical interface is shared with the $I^2C$ interface and therefore the user can only enable one or the other interface at any given time (see SPE in SPICON below). The system can be configured for Master or Slave operation and typically consists of four pins, namely:

**MISO (Master In, Slave Out Data I/O Pin), Pin#14**

The MISO (master in slave out) pin is configured as an input line in master mode and an output line in slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out). The data is transferred as byte wide (8-bit) serial data, MSB first.

**MOSI (Master Out, Slave In Pin), Pin#27**

The MOSI (master out slave in) pin is configured as an output line in master mode and an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte wide (8-bit) serial data, MSB first.

**SCLOCK (Serial Clock I/O Pin), Pin#26**

The master clock (SCLOCK) is used to synchronize the data being transmitted and received through the MOSI and MISO data lines. A single data bit is transmitted and received in each SCLOCK period. Therefore, a byte is transmitted/received after eight SCLOCK periods. The SCLOCK pin is configured as an output in master mode and as an input in slave mode. In master mode the bit-rate, polarity and phase of the clock are controlled by the CPOL, CPHA, SPR0 and SPR1 bits in the SPICON SFR (see Table XIX). In slave mode the SPICON register will have to be configured with the phase and polarity (CPHA and CPOL) of the expected input clock. In both master and slave mode the data is transmitted on one edge of the SCLOCK signal and sampled on the other. It is important therefore that the CPHA and CPOL are configured the same for the master and slave devices.

**$\overline{SS}$ (Slave Select Input Pin), Pin#13**

The Slave Select ($\overline{SS}$) input pin is only used when the ADuC824 is configured in slave mode to enable the SPI peripheral. This line is active low. Data is only received or transmitted in slave mode when the $\overline{SS}$ pin is low, allowing the ADuC824 to be used in single master, multislave SPI configurations. If CPHA = 1 then the $\overline{SS}$ input may be permanently pulled low. With CPHA = 0 then the $\overline{SS}$ input must be driven low before the first bit in a byte wide transmission or reception and return high again after the last bit in that byte wide transmission or reception. In SPI Slave Mode, the logic level on the external $\overline{SS}$ pin (Pin# 13), can be read via the SPR0 bit in the SPICON SFR.

The following SFR registers are used to control the SPI interface.

| **SPICON** | **SPI Control Register** |
|---|---|
| SFR Address | F8H |
| Power-On Default Value | 04H |
| Bit Addressable | Yes |

| ISPI | WCOL | SPE | SPIM | CPOL | CPHA | SPR1 | SPR0 |
|---|---|---|---|---|---|---|---|

**Table XIX. SPICON SFR Bit Designations**

| Bit | Name | Description |
|---|---|---|
| 7 | ISPI | SPI Interrupt Bit<br>*Set* by MicroConverter at the end of each SPI transfer.<br>*Cleared* directly by user code or indirectly by reading the SPIDAT SFR. |
| 6 | WCOL | Write Collision Error Bit<br>*Set* by MicroConverter if SPIDAT is written to while an SPI transfer is in progress.<br>*Cleared* by user code. |
| 5 | SPE | SPI Interface Enable Bit<br>*Set* by user to enable the SPI interface.<br>*Cleared* by user to enable the $I^2C$ interface. |
| 4 | SPIM | SPI Master/Slave Mode Select Bit<br>*Set* by user to enable Master Mode operation (SCLOCK is an output).<br>*Cleared* by user to enable Slave Mode operation (SCLOCK is an input). |
| 3 | CPOL* | Clock Polarity Select Bit<br>*Set* by user if SCLOCK idles high.<br>*Cleared* by user if SCLOCK idles low. |
| 2 | CPHA* | Clock Phase Select Bit<br>*Set* by user if leading SCLOCK edge is to transmit data.<br>*Cleared* by user if trailing SCLOCK edge is to transmit data. |
| 1 | SPR1 | SPI Bit-Rate Select Bits |
| 0 | SPR0 | These bits select the SCLOCK rate (bit-rate) in Master Mode as follows:<br>SPR1 SPR0 Selected Bit Rate — SPR1 SPR0 Selected Bit Rate<br>0 0 $f_{CORE}/2$ — 1 0 $f_{CORE}/8$<br>0 1 $f_{CORE}/4$ — 1 1 $f_{CORE}/16$<br>In SPI Slave Mode, i.e., SPIM = 0, the logic level on the external $\overline{SS}$ pin (Pin# 13), can be read via the SPR0 bit. |

*Bits should contain the same values for master and slave devices.

**TIMER/COUNTER 0 AND 1 OPERATING MODES**

The following paragraphs describe the operating modes for timer/counters 0 and 1. Unless otherwise noted, assume that these modes of operation are the same for timer 0 as for timer 1.

**Mode 0 (13-Bit Timer/Counter)**

Mode 0 configures an 8-bit timer/counter with a divide-by-32 prescaler. Figure 34 shows mode 0 operation.

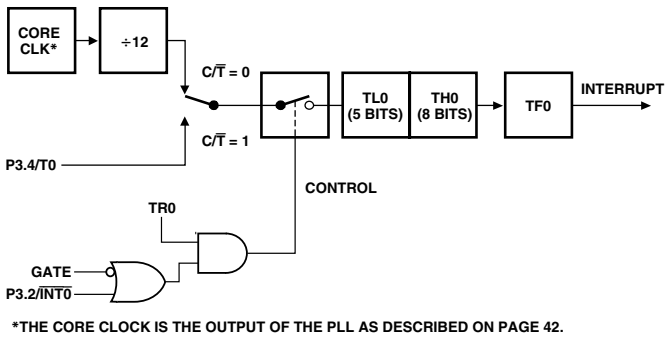


*Figure 34. Timer/Counter 0, Mode 0*

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer overflow flag TF0. The overflow flag, TF0, can then be used to request an interrupt. The counted input is enabled to the timer when TR0 = 1 and either Gate = 0 or $\overline{INT0}$ = 1. Setting Gate = 1 allows the timer to be controlled by external input $\overline{INT0}$, to facilitate pulsewidth measurements. TR0 is a control bit in the special function register TCON; Gate is in TMOD. The 13-bit register consists of all eight bits of TH0 and the lower five bits of TL0. The upper three bits of TL0 are indeterminate and should be ignored. Setting the run flag (TR0) does not clear the registers.

**Mode 1 (16-Bit Timer/Counter)**

Mode 1 is the same as Mode 0, except that the timer register is running with all 16 bits. Mode 1 is shown in Figure 35.

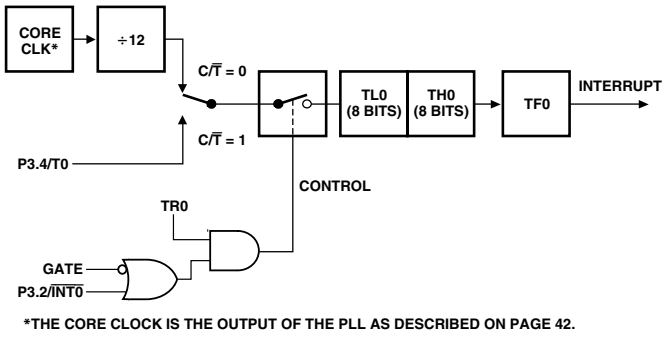


*Figure 35. Timer/Counter 0, Mode 1*

**Mode 2 (8-Bit Timer/Counter with Auto Reload)**

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reload, as shown in Figure 36. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is preset by software. The reload leaves TH0 unchanged.

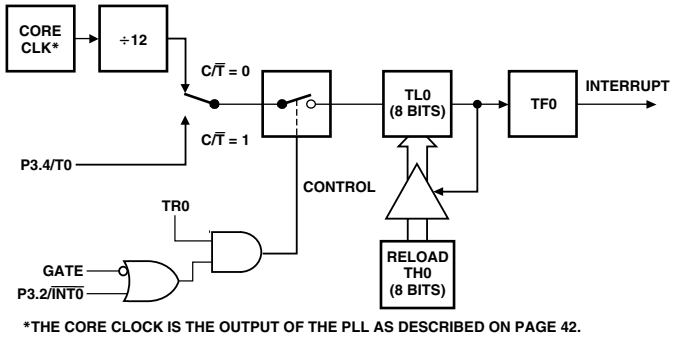


*Figure 36. Timer/Counter 0, Mode 2*

**Mode 3 (Two 8-Bit Timer/Counters)**

Mode 3 has different effects on timer 0 and timer 1. Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. This configuration is shown in Figure 37. TL0 uses the timer 0 control bits: C/T, Gate, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from timer 1. Thus, TH0 now controls the "timer 1" interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer or counter.

When timer 0 is in Mode 3, timer 1 can be turned on and off by switching it out of, and into, its own Mode 3, or can still be used by the serial interface as a *Baud Rate Generator*. In fact, it can be used, in any application not requiring an interrupt from timer 1 itself.

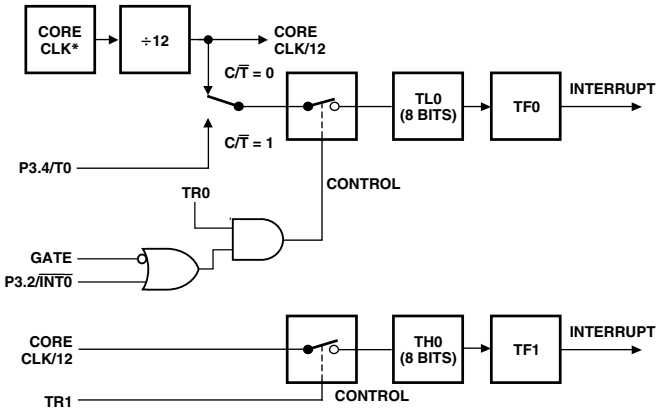


*Figure 37. Timer/Counter 0, Mode 3*

**T2CON** **Timer/Counter 2 Control Register**
SFR Address C8H
Power-On Default Value 00H
Bit Addressable Yes

| TF2 | EXF2 | RCLK | TCLK | EXEN2 | TR2 | CNT2 | CAP2 |
|---|---|---|---|---|---|---|---|

**Table XXV. T2CON SFR Bit Designations**

| Bit | Name | Description |
|---|---|---|
| 7 | TF2 | Timer 2 Overflow Flag<br>*Set* by hardware on a Timer 2 overflow. TF2 will not be set when either RCLK or TCLK = 1.<br>*Cleared* by user software. |
| 6 | EXF2 | Timer 2 External Flag<br>*Set* by hardware when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1.<br>*Cleared* by user user software. |
| 5 | RCLK | Receive Clock Enable Bit<br>*Set* by user to enable the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3.<br>*Cleared* by user to enable Timer 1 overflow to be used for the receive clock. |
| 4 | TCLK | Transmit Clock Enable Bit<br>*Set* by user to enable the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3.<br>*Cleared* by user to enable Timer 1 overflow to be used for the transmit clock. |
| 3 | EXEN2 | Timer 2 External Enable Flag<br>*Set* by user to enable a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port.<br>*Cleared* by user for Timer 2 to ignore events at T2EX. |
| 2 | TR2 | Timer 2 Start/Stop Control Bit<br>*Set* by user to start Timer 2.<br>*Cleared* by user to stop Timer 2. |
| 1 | CNT2 | Timer 2 Timer or Counter Function Select Bit<br>*Set* by user to select counter function (input from external T2 pin).<br>*Cleared* by user to select timer function (input from on-chip core clock). |
| 0 | CAP2 | Timer 2 Capture/Reload Select Bit<br>*Set* by user to enable captures on negative transitions at T2EX if EXEN2 = 1.<br>*Cleared* by user to enable auto-reloads with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to autoreload on Timer 2 overflow. |

**Timer/Counter 2 Data Registers**
Timer/Counter 2 also has two pairs of 8-bit data registers associated with it. These are used as both timer data registers and timer capture/reload registers.

**TH2 and TL2**
Timer 2, data high byte and low byte.
SFR Address = CDhex, CChex respectively.

**RCAP2H and RCAP2L**
Timer 2, Capture/Reload byte and low byte.
SFR Address = CBhex, CAhex respectively.

**Timer/Counter 2 Operating Modes**

The following paragraphs describe the operating modes for timer/counter 2. The operating modes are selected by bits in the T2CON SFR as shown in Table XXVI.

**Table XXVI. TIMECON SFR Bit Designations**

| RCLK (or) TCLK | CAP2 | TR2 | MODE |
|---|---|---|---|
| 0 | 0 | 1 | 16-Bit Autoreload |
| 0 | 1 | 1 | 16-Bit Capture |
| 1 | X | 1 | Baud Rate |
| X | X | 0 | OFF |

**16-Bit Autoreload Mode**

In 'Autoreload' mode, there are two options, which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then when Timer 2 rolls over it not only sets TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1, then Timer 2 still performs the above, but with the added feature that a 1-to-0 transition at external input T2EX will also trigger the 16-bit reload and set EXF2. The autoreload mode is illustrated in Figure 38.

**16-Bit Capture Mode**

In the 'Capture' mode, there are again two options, which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which, upon overflowing, sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, then Timer 2 still performs the above, but a l-to-0 transition on external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt. The Capture Mode is illustrated in Figure 39.

The baud rate generator mode is selected by RCLK = 1 and/or TCLK = 1.

In either case if Timer 2 is being used to generate the baud rate, the TF2 interrupt flag will not occur. Hence Timer 2 interrupts will not occur so they do not have to be disabled. In this mode the EXF2 flag, however, can still cause interrupts and this can be used as a third external interrupt.

Baud rate generation will be described as part of the UART serial port operation in the following pages.

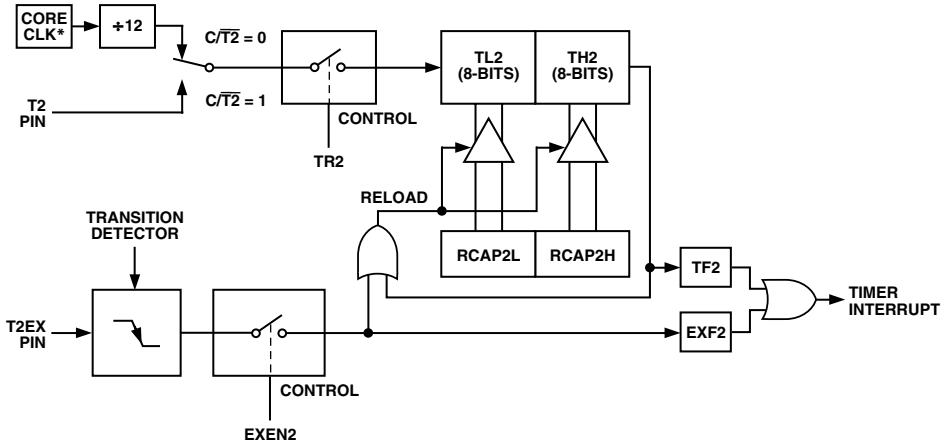


*Figure 38. Timer/Counter 2, 16-Bit Autoreload Mode*

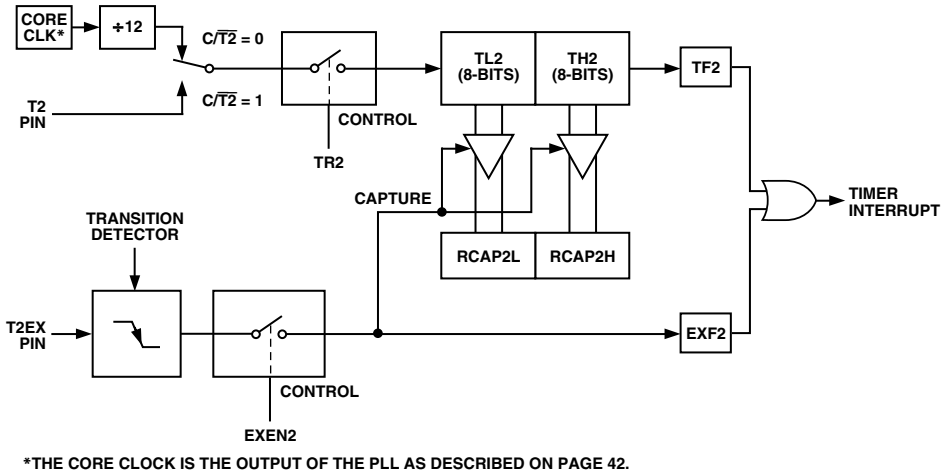


*Figure 39. Timer/Counter 2, 16-Bit Capture Mode*

**Mode 0: 8-Bit Shift Register Mode**

Mode 0 is selected by clearing both the SM0 and SM1 bits in the SFR SCON. Serial data enters and exits through RXD. TXD outputs the shift clock. Eight data bits are transmitted or received. Transmission is initiated by any instruction that writes to SBUF. The data is shifted out of the RXD line. The eight bits are transmitted with the least-significant bit (LSB) first, as shown in Figure 40.

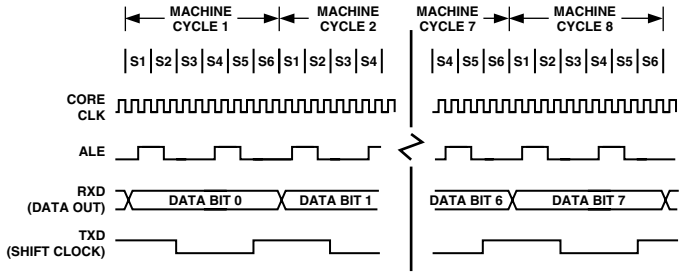


*Figure 40. UART Serial Port Transmission, Mode 0.*

Reception is initiated when the receive enable bit (REN) is 1 and the receive interrupt bit (RI) is 0. When RI is cleared the data is clocked into the RXD line and the clock pulses are output from the TXD line.

**Mode 1: 8-Bit UART, Variable Baud Rate**

Mode 1 is selected by clearing SM0 and setting SM1. Each data byte (LSB first) is preceded by a start bit(0) and followed by a stop bit(1). Therefore 10 bits are transmitted on TXD or received on RXD. The baud rate is set by the Timer 1 or Timer 2 overflow rate, or a combination of the two (one for transmission and the other for reception).

Transmission is initiated by writing to SBUF. The 'write to SBUF' signal also loads a 1 (stop bit) into the ninth bit position of the transmit shift register. The data is output bit by bit until the stop bit appears on TXD and the transmit interrupt flag (TI) is automatically set as shown in Figure 41.

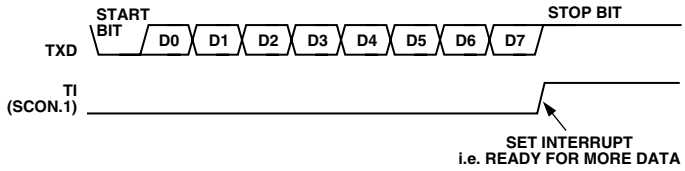


*Figure 41. UART Serial Port Transmission, Mode 0.*

Reception is initiated when a 1-to-0 transition is detected on RXD. Assuming a valid start bit was detected, character reception continues. The start bit is skipped and the eight data bits are clocked into the serial port shift register. When all eight bits have been clocked in, the following events occur:

The eight bits in the receive shift register are latched into SBUF

The ninth bit (Stop bit) is clocked into RB8 in SCON

The Receiver interrupt flag (RI) is set

if, and only if, the following conditions are met at the time the final shift pulse is generated:

RI = 0, and

Either SM2 = 0, or SM2 = 1 and the received stop bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set.

**Mode 2: 9-Bit UART with Fixed Baud Rate**

Mode 2 is selected by setting SM0 and clearing SM1. In this mode the UART operates in 9-bit mode with a fixed baud rate. The baud rate is fixed at Core_Clk/64 by default, although by setting the SMOD bit in PCON, the frequency can be doubled to Core_Clk/32. Eleven bits are transmitted or received, a start bit(0), eight data bits, a programmable ninth bit and a stop bit(1). The ninth bit is most often used as a parity bit, although it can be used for anything, including a ninth data bit if required.

To transmit, the eight data bits must be written into SBUF. The ninth bit must be written to TB8 in SCON. When transmission is initiated the eight data bits (from SBUF) are loaded onto the transmit shift register (LSB first). The contents of TB8 are loaded into the ninth bit position of the transmit shift register. The transmission will start at the next valid baud rate clock. The TI flag is set as soon as the stop bit appears on TXD.

Reception for Mode 2 is similar to that of Mode 1. The eight data bytes are input at RXD (LSB first) and loaded onto the receive shift register. When all eight bits have been clocked in, the following events occur:

The eight bits in the receive shift register are latched into SBUF

The ninth data bit is latched into RB8 in SCON

The Receiver interrupt flag (RI) is set

if, and only if, the following conditions are met at the time the final shift pulse is generated:

RI = 0, and

Either SM2 = 0, or SM2 = 1 and the received stop bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set.

**Mode 3: 9-Bit UART with Variable Baud Rate**

Mode 3 is selected by setting both SM0 and SM1. In this mode the 8051 UART serial port operates in 9-bit mode with a variable baud rate determined by either Timer 1 or Timer 2. The operation of the 9-bit UART is the same as for Mode 2 but the baud rate can be varied as for Mode 1.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

**UART Serial Port Baud Rate Generation**

***Mode 0 Baud Rate Generation***

The baud rate in Mode 0 is fixed:

Mode 0 Baud Rate = (Core Clock Frequency*/12)

*In these descriptions, Core Clock Frequency refers to the core clock frequency selected via the CD0–2 bits in the PLLCON SFR.

***Mode 2 Baud Rate Generation***

The baud rate in Mode 2 depends on the value of the SMOD bit in the PCON SFR. If SMOD = 0, the baud rate is 1/64 of the core clock. If SMOD = 1, the baud rate is 1/32 of the core clock:

Mode 2 Baud Rate = $(2^{SMOD}/64) \times$ (Core Clock Frequency)

***Mode 1 and 3 Baud Rate Generation***

The baud rates in Modes 1 and 3 are determined by the overflow rate in Timer 1 or Timer 2, or both (one for transmit and the other for receive).

**ADuC824 HARDWARE DESIGN CONSIDERATIONS**

This section outlines some of the key hardware design considerations that must be addressed when integrating the ADuC824 into any hardware system.

**Clock Oscillator**

As described earlier, the core clock frequency for the ADuC824 is generated from an on-chip PLL that locks onto a multiple (384 times) of 32.768 kHz. The latter is generated from an internal clock oscillator. To use the internal clock oscillator, connect a 32.768 kHz parallel resonant crystal between XTAL1 and XTAL2 pins (32 and 33) as shown in Figure 43.

As shown in the typical external crystal connection diagram in Figure 44, two internal 12 pF capacitors are provided on-chip. These are connected internally, directly to the XTAL1 and XTAL2 pins and the total input capacitances at both pins is detailed in the specification section of this data sheet. The value of the total load capacitance required for the external crystal should be the value recommended by the crystal manufacturer for use with that specific crystal. In many cases, because of the on-chip capacitors, additional external load capacitors will not be required.

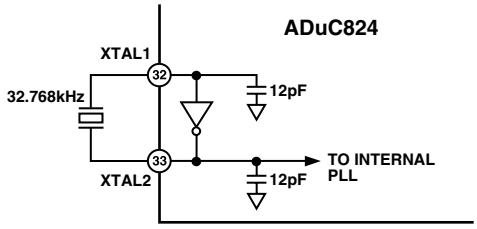


*Figure 43. External Parallel Resonant Crystal Connections*

**External Memory Interface**

In addition to its internal program and data memories, the ADuC824 can access up to 64 Kbytes of external program memory (ROM/PROM/etc.) and up to 16 Mbytes of external data memory (SRAM).

To select from which code space (internal or external program memory) to begin executing instructions, tie the $\overline{EA}$ (external access) pin high or low, respectively. When $\overline{EA}$ is high (pulled up to $V_{DD}$), user program execution will start at address 0 of the internal 8 Kbytes Flash/EE code space. When $\overline{EA}$ is low (tied to ground) user program execution will start at address 0 of the external code space. In either case, addresses above 1FFF hex (8K) are mapped to the external space.

Note that a second very important function of the $\overline{EA}$ pin is described in the Single Pin Emulation Mode section of this data sheet.

External program memory (if used) must be connected to the ADuC824 as illustrated in Figure 44. Note that 16 I/O lines (Ports 0 and 2) are dedicated to bus functions during external program memory fetches. Port 0 (P0) serves as a multiplexed address/data bus. It emits the low byte of the program counter (PCL) as an address, and then goes into a float state awaiting the arrival of the code byte from the program memory. During the time that the low byte of the program counter is valid on P0, the signal ALE (Address Latch Enable) clocks this byte into an address latch. Meanwhile, Port 2 (P2) emits the high byte of the program counter (PCH), then $\overline{PSEN}$ strobes the EPROM and the code byte is read into the ADuC824.

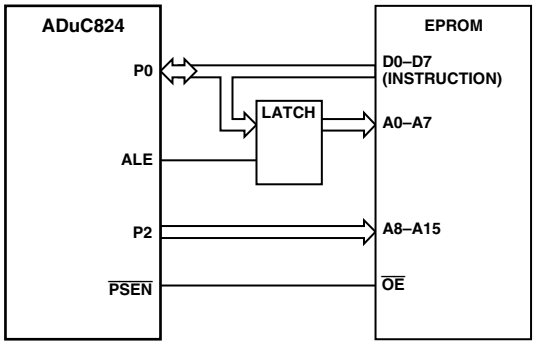


*Figure 44. External Program Memory Interface*

Note that program memory addresses are always 16 bits wide, even in cases where the actual amount of program memory used is less than 64 Kbytes. External program execution sacrifices two of the 8-bit ports (P0 and P2) to the function of addressing the program memory. While executing from external program memory, Ports 0 and 2 can be used simultaneously for read/write access to external data memory, but not for general-purpose I/O.

Though both external program memory and external data memory are accessed by some of the same pins, the two are completely independent of each other from a software point of view. For example, the chip can read/write external data memory while executing from external program memory.

Figure 45 shows a hardware configuration for accessing up to 64 Kbytes of external RAM. This interface is standard to any 8051 compatible MCU.

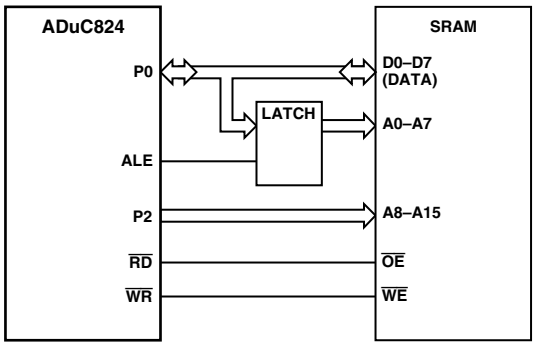


*Figure 45. External Data Memory Interface (64 K Address Space)*

If access to more than 64 Kbytes of RAM is desired, a feature unique to the ADuC824 allows addressing up to 16 Mbytes of external RAM simply by adding an additional latch as illustrated in Figure 46.

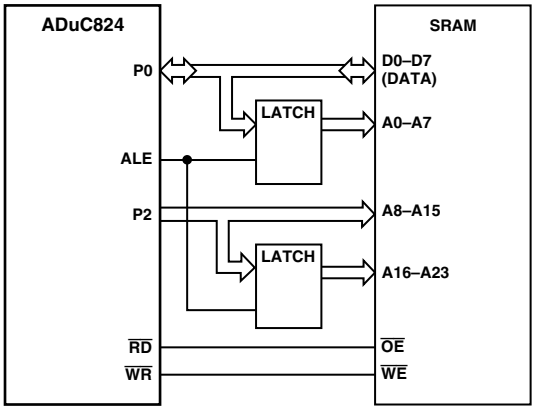


*Figure 46. External Data Memory Interface (16 MBytes Address Space)*

In either implementation, Port 0 (P0) serves as a multiplexed address/data bus. It emits the low byte of the data pointer (DPL) as an address, which is latched by a pulse of ALE prior to data being placed on the bus by the ADuC824 (write operation) or the SRAM (read operation). Port 2 (P2) provides the data pointer page byte (DPP) to be latched by ALE, followed by the data pointer high byte (DPH). If no latch is connected to P2, DPP is ignored by the SRAM, and the 8051 standard of 64 Kbyte external data memory access is maintained.

Detailed timing diagrams of external program and data memory read and write access can be found in the timing specification sections of this data sheet.

**Power-On Reset Operation**

External POR (power-on reset) circuitry must be implemented to drive the RESET pin of the ADuC824. The circuit must hold the RESET pin asserted (high) whenever the power supply ($DV_{DD}$) is below 2.5 V. Furthermore, $V_{DD}$ must remain above 2.5 V for at least 10 ms before the RESET signal is deasserted (low) by which time the power supply must have reached at least a 2.7 V level. The external POR circuit must be operational down to 1.2 V or less. The timing diagram of Figure 47 illustrates this functionality under three separate events: power-up, brownout, and power-down. Notice that when RESET is asserted (high) it tracks the voltage on $DV_{DD}$.

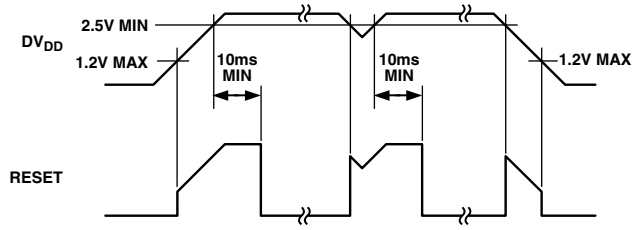


*Figure 47. External POR Timing*

The best way to implement an external POR function to meet the above requirements involves the use of a dedicated POR chip, such as the ADM809/ADM810 SOT-23 packaged PORs from Analog Devices. Recommended connection diagrams for both active-high ADM810 and active-low ADM809 PORs are shown in Figure 48 and Figure 49 respectively.

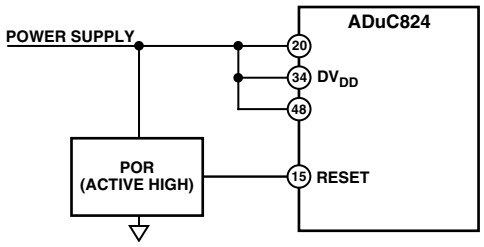


*Figure 48. External Active High POR Circuit*

Some active-low POR chips, such as the ADM809 can be used with a manual push-button as an additional reset source as illustrated by the dashed line connection in Figure 49.

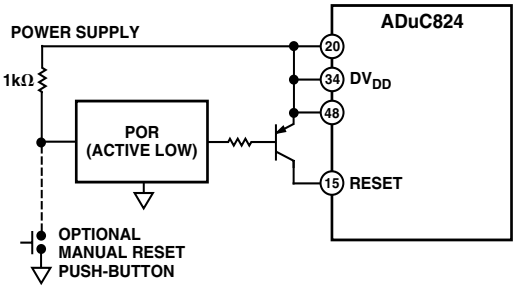


*Figure 49. External Active Low POR Circuit*

**Power Supplies**

The ADuC824's operational power supply voltage range is 2.7 V to 5.25 V. Although the guaranteed data sheet specifications are given only for power supplies within 2.7 V to 3.6 V or +5% of the nominal 5 V level, the chip will function equally well at any power supply level between 2.7 V and 5.25 V.

Separate analog and digital power supply pins ($AV_{DD}$ and $DV_{DD}$ respectively) allow $AV_{DD}$ to be kept relatively free of noisy digital signals often present on the system DVDD line. In this mode the part can also operate with split supplies; that is, using different voltage supply levels for each supply. For example, this means that the system can be designed to operate with a $DV_{DD}$ voltage level of 3 V while the $AV_{DD}$ level can be at 5 V or vice versa if required. A typical split supply configuration is show in Figure 50.

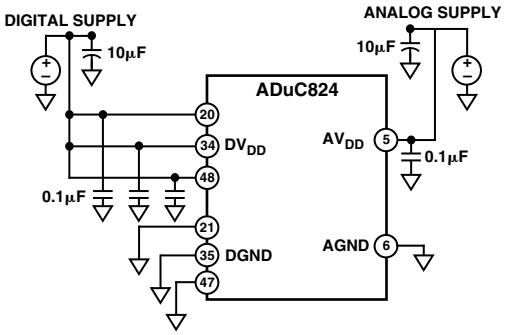


*Figure 50. External Dual Supply Connections*

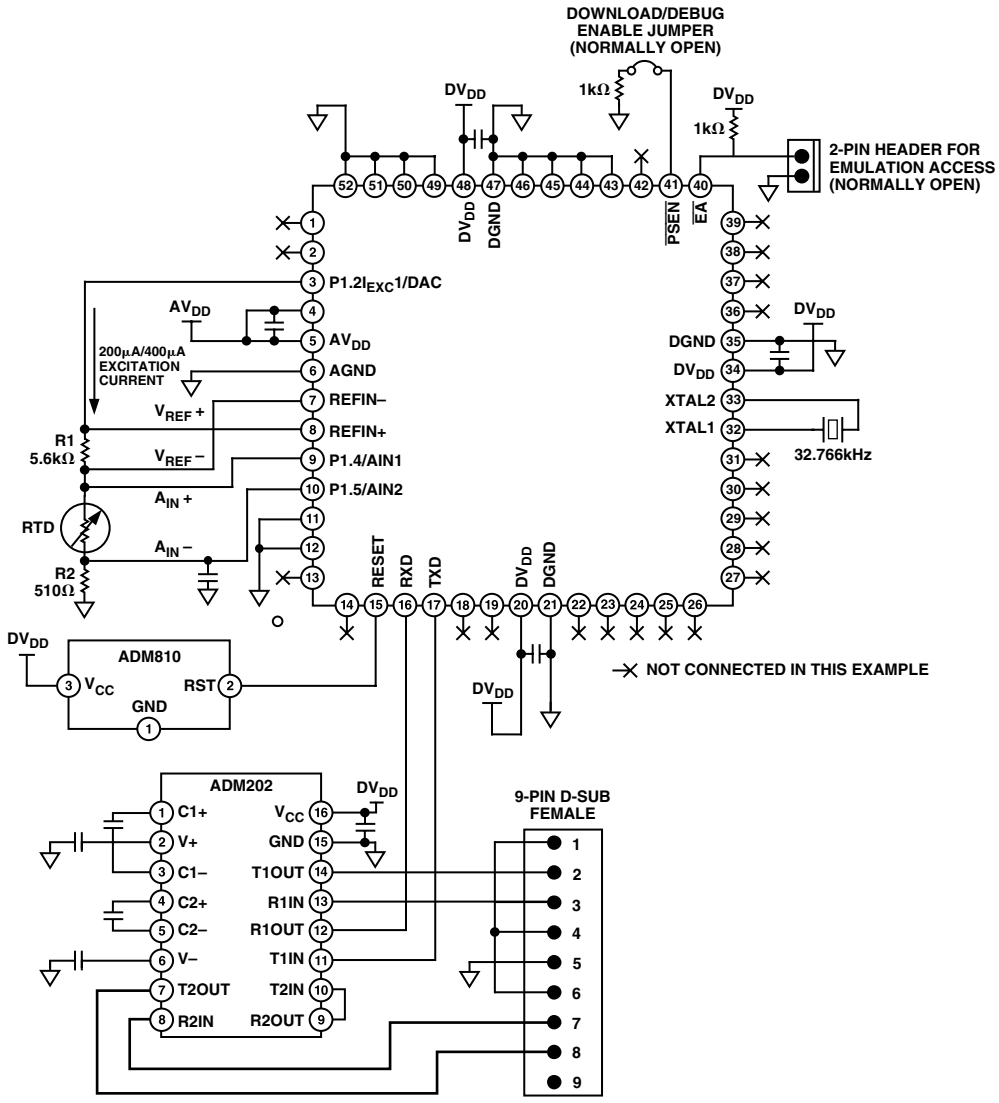


*Figure 53. Typical System Configuration*

comes with the single-pin emulator available from Accutron Limited (www.accutron.com), use a 2-pin 0.1-inch pitch "Friction Lock" header from Molex (www.molex.com) such as their part number 22-27-2021. Be sure to observe the polarity of this header. As represented in Figure 53, when the Friction Lock tab is at the right, the ground pin should be the lower of the two pins (when viewed from the top).

**Enhanced-Hooks Emulation Mode**

ADuC824 also supports enhanced-hooks emulation mode. An enhanced-hooks-based emulator is available from Metalink Corporation (www.metaice.com). No special hardware support for these emulators needs to be designed onto the board since these are "pod-style" emulators where users must replace the chip on their board with a header device that the emulator pod plugs into. The only hardware concern is then one of determining if adequate space is available for the emulator pod to fit into the system enclosure.

**Typical System Configuration**

A typical ADuC824 configuration is shown in Figure 53. It summarizes some of the hardware considerations discussed in the previous paragraphs.

Figure 53 also includes connections for a typical analog measurement application of the ADuC824, namely an interface to an RTD (Resistive Temperature Device). The arrangement shown is commonly referred to as a 4-wire RTD configuration.

Here, the on-chip excitation current sources are enabled to excite the sensor. An external differential reference voltage is generated by the current sourced through resistor R1. This current also flows directly through the RTD, which generates a differential voltage directly proportional to temperature. This differential voltage is routed directly to the positive and negative inputs of the primary ADC (AIN1, AIN2 respectively). A second external resistor, R2, is used to ensure that absolute analog input voltage on the negative input to the primary ADC stays within that specified for the ADuC824, i.e., AGND + 100 mV.

It should also be noted that variations in the excitation current do not affect the measurement system as the input voltage from the RTD and reference voltage across R1 vary ratiometrically with the excitation current. Resistor R1 must, however, have a low temperature coefficient to avoid errors in the reference voltage over temperature.