Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf13k22-e-ss

TABLE 1-1: DEVICE FEATURES FOR THE PI C18(L)F1XK22 (20-PIN DEVICES)

Features	PIC18F13K22	PIC18LF13K22	PIC18F14K22	PIC18LF14K22
Voltage Range (1.8 - 5.5V)	2.3-5.5V	1.8V-3.6V	2.3-5.5V	1.8V-3.6V
Program Memory (Bytes)	8K		16K	
Program Memory (Instructions)	4096		8192	
Data Memory (Bytes)	256		512	
Operating Frequency	DC – 64 MHz			
Interrupt Sources	30			
I/O Ports	Ports A, B, C			
Timers	4			
Enhanced Capture/ Compare/PWM Modules	1			
Serial Communications	MSSP, Enhanced USART			
10-Bit Analog-to-Digital Module	12 Input Channels			
Resets (and Delays)	POR, BOR, RESETInstruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST)			
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled			
Packages	20-Pin PDIP, SSOP, SOIC QFN (4x4x0.9mm)			

TABLE 3-2: REGISTER FILE SUMMARY (PIC18(L)F1XK22) (CONTINUED)

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
SPBRGH	EUSART Baud Rate Generator Register, High Byte								0000 0000	247, 182
SPBRG	EUSART Baud Rate Generator Register, Low Byte								0000 0000	247, 182
RCREG	EUSART Receive Register								0000 0000	247, 175
TXREG	EUSART Transmit Register								0000 0000	247, 172
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	247, 179
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	247, 180
EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000	247, 45, 54
EEDATA	EEPROM Data Register								0000 0000	247, 45, 54
EECON2	EEPROM Control Register 2 (not a physical register)								0000 0000	247, 45, 54
EECON1	EEPGD	CFGS	—	FREE	WRERR	WREN	WR	RD	xx-0 x000	247, 45, 54
IPR2	OSCFIP	C1IP	C2IP	EEIP	BCLIP	—	TMR3IP	—	1111 1-1-	248, 70
PIR2	OSCFIF	C1IF	C2IF	EEIF	BCLIF	—	TMR3IF	—	0000 0-0-	248, 66
PIE2	OSCFIE	C1IE	C2IE	EEIE	BCLIE	—	TMR3IE	—	0000 0-0-	248, 68
IPR1	—	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	-111 1111	248, 69
PIR1	—	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	248, 65
PIE1	—	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	248, 67
OSCTUNE	INTSRC	PLLEN	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0	0000 0000	248, 19
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	248, 84
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	1111 ----	248, 80
TRISA	—	—	TRISA5	TRISA4	—(3)	TRISA2	TRISA1	TRISA0	--11 1111	248, 75
LATC	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx xxxx	248, 85
LATB	LATB7	LATB6	LATB5	LATB4	—	—	—	—	xxxx ----	248, 80
LATA	—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0	--xx -xxx	248, 76
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	248, 84
PORTB	RB7	RB6	RB5	RB4	—	—	—	—	xxxx ----	248, 80
PORTA	—	—	RA5	RA4	RA3(2)	RA2	RA1	RA0	--xx xxxx	248, 75
ANSELH	—	—	—	—	ANS11	ANS10	ANS9	ANS8	---- 1111	248, 89
ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	248, 88
IOCB	IOCB7	IOCB6	IOCB5	IOCB4	—	—	—	—	0000 ----	248, 81
IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	248, 76
WPUB	WPUB7	WPUB6	WPUB5	WPUB4	—	—	—	—	1111 ----	248, 81
WPUA	—	—	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	--11 1111	245, 76
SLRCON	—	—	—	—	—	SLRC	SLRB	SLRA	---- -111	248, 90
SSPMSK	MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0	1111 1111	248, 146
CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	248, 216
CM2CON1	MC1OUT	MC2OUT	C1RSEL	C2RSEL	C1HYS	C2HYS	C1SYNC	C2SYNC	0000 0000	248, 220
CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0	0000 0000	248, 217
SRCON1	SRSPE	SRSCKE	SRSC2E	SRSC1E	SRRPE	SRRCKE	SRRC2E	SRRC1E	0000 0000	248, 230
SRCON0	SRLEN	SRCLK2	SRCLK1	SRCLK0	SRQEN	SRNQEN	SRPS	SRPR	0000 0000	248, 229

Legend: x = unknown, u = unchanged, —= unimplemented, q = value depends on condition

Note 1: The SBOREN bit is only available when the BOREN<1:0> Configuration bits = 01; otherwise it is disabled and reads as '0'. See Section 22.4 "Brown-out Reset (BOR)" .

2: The RA3 bit is only available when Master Clear Reset is disabled (MCLRE Configuration bit = 0). Otherwise, RA3 reads as '0'. This bit is read-only.

3: Unimplemented, read as '1'.