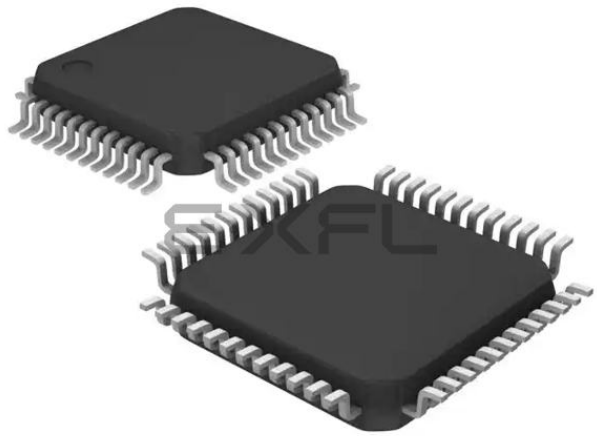


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	45MHz
Connectivity	I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	39
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1224fbd48-101-1

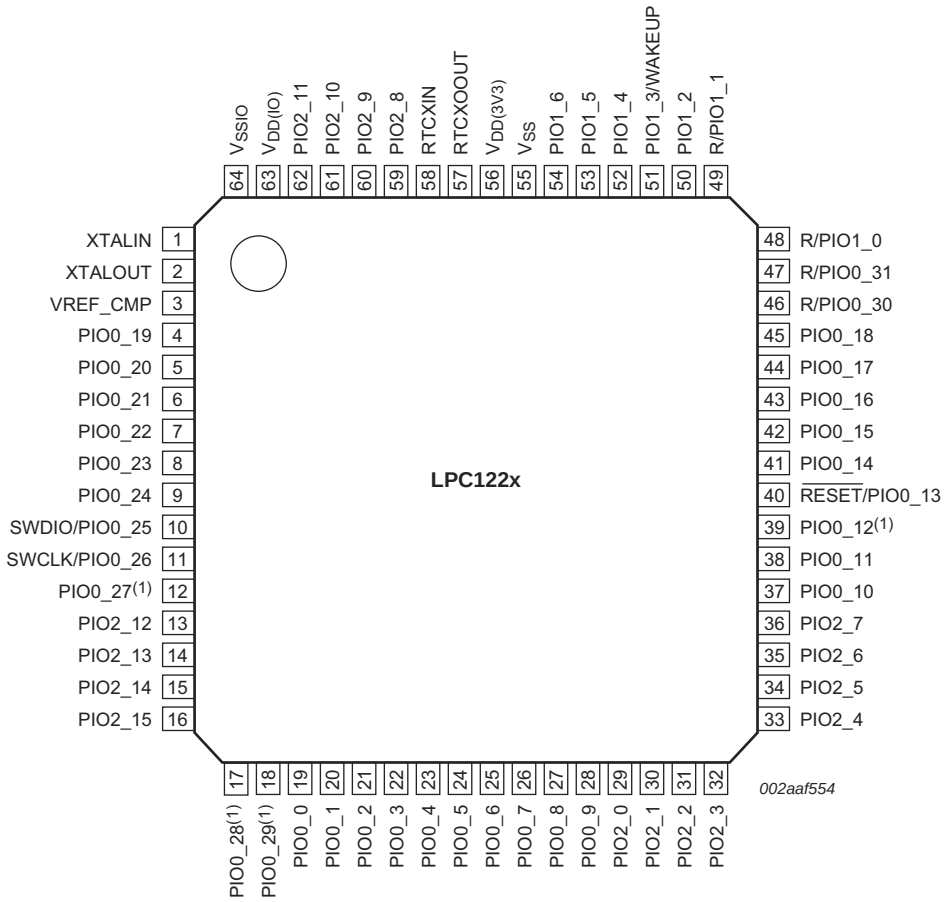
4.1 Ordering options

Table 2. Ordering options for LPC122x

Type number	Flash	Total SRAM	UART	I^2C/ FM+	SSP/ SPI	ADC channels	GPIO	Package
LPC1227								
LPC1227FBD64/301	128 kB	8 kB	2	1	1	8	55	LQFP64
LPC1227FBD48/301	128 kB	8 kB	2	1	1	8	39	LQFP48
LPC1226								
LPC1226FBD64/301	96 kB	8 kB	2	1	1	8	55	LQFP64
LPC1226FBD48/301	96 kB	8 kB	2	1	1	8	39	LQFP48
LPC1225								
LPC1225FBD64/321	80 kB	8 kB	2	1	1	8	55	LQFP64
LPC1225FBD64/301	64 kB	8 kB	2	1	1	8	55	LQFP64
LPC1225FBD48/321	80 kB	8 kB	2	1	1	8	39	LQFP48
LPC1225FBD48/301	64 kB	8 kB	2	1	1	8	39	LQFP48
LPC1224								
LPC1224FBD64/121	48 kB	4 kB	2	1	1	8	55	LQFP64
LPC1224FBD64/101	32 kB	4 kB	2	1	1	8	55	LQFP64
LPC1224FBD48/121	48 kB	4 kB	2	1	1	8	39	LQFP48
LPC1224FBD48/101	32 kB	4 kB	2	1	1	8	39	LQFP48

6. Pinning information

6.1 Pinning



(1) High-current output driver.

Remark: For a full listing of all functions for each pin see Table 3.

Fig 2. Pin configuration LQFP64 package

Table 3. LPC122x pin description *…continued*

Symbol	Pin LQFP48	Pin LQFP64		Start logic input	Type	Reset state [1]	Description
PIO1_5/AD7/ CT16B1_CAP0/ CT16B1_MAT0	41	53	[6] [3]	no	I/O	I; PU	**PIO1_5 —** General purpose digital input/output pin.
					I	-	**AD7 —** A/D converter, input 7.
					I	-	**CT16B1_CAP0 —** Capture input, channel 0 for 16-bit timer 1.
					O	-	**CT16B1_MAT0 —** Match output, channel 0 for 16-bit timer 1.
PIO1_6/ CT16B1_CAP1/ CT16B1_MAT1	42	54	[2] [3]	no	I/O	I; PU	**PIO1_6 —** General purpose digital input/output pin.
					I	-	**CT16B1_CAP1 —** Capture input, channel 1 for 16-bit timer 1.
					O	-	**CT16B1_MAT1 —** Match output, channel 1 for 16-bit timer 1.
PIO2_0 to PIO2_15					I/O		**Port 2 —** Port 2 is a 32-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block. Pins PIO2_16 through PIO2_31 are not available.
PIO2_0/ CT16B0_CAP0/ CT16B0_MAT0/ $\overline{\text{RTS0}}$	-	29	[2] [3]	no	I/O	I; PU	**PIO2_0 —** General purpose digital input/output pin.
					I	-	**CT16B0_CAP0 —** Capture input, channel 0 for 16-bit timer 0.
					O	-	**CT16B0_MAT0 —** Match output, channel 0 for 16-bit timer 0.
					O	-	**$\overline{\text{RTS0}}$ —** Request To Send output for UART0.
PIO2_1/ CT16B0_CAP1/ CT16B0_MAT1/RXD0	-	30	[2] [3]	no	I/O	I; PU	**PIO2_1 —** General purpose digital input/output pin.
					I	-	**CT16B0_CAP1 —** Capture input, channel 1 for 16-bit timer 0.
					O	-	**CT16B0_MAT1 —** Match output, channel 1 for 16-bit timer 0.
					I	-	**RXD0 —** Receiver input for UART0.
PIO2_2/ CT16B1_CAP0/ CT16B1_MAT0/TXD0	-	31	[2] [3]	no	I/O	I; PU	**PIO2_2 —** General purpose digital input/output pin.
					I	-	**CT16B1_CAP0 —** Capture input, channel 0 for 16-bit timer 1.
					O	-	**CT16B1_MAT0 —** Match output, channel 0 for 16-bit timer 1.
					O	-	**TXD0 —** Transmitter output for UART0.
PIO2_3/ CT16B1_CAP1/ CT16B1_MAT1/$\overline{\text{DTR0}}$	-	32	[2] [3]	no	I/O	I; PU	**PIO2_3 —** General purpose digital input/output pin.
					I	-	**CT16B1_CAP1 —** Capture input, channel 1 for 16-bit timer 1.
					O	-	**CT16B1_MAT1 —** Match output, channel 1 for 16-bit timer 1.
					O	-	**$\overline{\text{DTR0}}$ —** Data Terminal Ready output for UART0.
PIO2_4/ CT32B0_CAP0/ CT32B0_MAT0/$\overline{\text{CTS0}}$	-	33	[2] [3]	no	I/O	I; PU	**PIO2_4 —** General purpose digital input/output pin.
					I	-	**CT32B0_CAP0 —** Capture input, channel 0 for 32-bit timer 0.
					O	-	**CT32B0_MAT0 —** Match output, channel 0 for 32-bit timer 0.
					I	-	**$\overline{\text{CTS0}}$ —** Clear To Send input for UART0.
PIO2_5/ CT32B0_CAP1/ CT32B0_MAT1/$\overline{\text{RI0}}$	-	34	[2] [3]	no	I/O	I; PU	**PIO2_5 —** General purpose digital input/output pin.
					I	-	**CT32B0_CAP1 —** Capture input, channel 1 for 32-bit timer 0.
					O	-	**CT32B0_MAT1 —** Match output, channel 1 for 32-bit timer 0.
					I	-	**$\overline{\text{RI0}}$ —** Ring Indicator input for UART0.

Table 3. LPC122x pin description *…continued*

Symbol	Pin LQFP48	Pin LQFP64		Start logic input	Type	Reset state [1]	Description
PIO2_6/ CT32B0_CAP2/ CT32B0_MAT2/DCD0	-	35	[2] [3]	no	I/O	I; PU	**PIO2_6 —** General purpose digital input/output pin.
					I	-	**CT32B0_CAP2 —** Capture input, channel 2 for 32-bit timer 0.
					O	-	**CT32B0_MAT2 —** Match output, channel 2 for 32-bit timer 0.
					I	-	**DCD0 —** Data Carrier Detect input for UART0.
PIO2_7/ CT32B0_CAP3/ CT32B0_MAT3/DSR0	-	36	[2] [3]	no	I/O	I; PU	**PIO2_7 —** General purpose digital input/output pin.
					I	-	**CT32B0_CAP3 —** Capture input, channel 3 for 32-bit timer 0.
					O	-	**CT32B0_MAT3 —** Match output, channel 3 for 32-bit timer 0.
					I	-	**DSR0 —** Data Set Ready input for UART0.
PIO2_8/ CT32B1_CAP0/ CT32B1_MAT0	-	59	[2] [3]	no	I/O	I; PU	**PIO2_8 —** General purpose digital input/output pin.
					I	-	**CT32B1_CAP0 —** Capture input, channel 0 for 32-bit timer 1.
					O	-	**CT32B1_MAT0 —** Match output, channel 0 for 32-bit timer 1.
PIO2_9/ CT32B1_CAP1/ CT32B1_MAT1	-	60	[2] [3]	no	I/O	I; PU	**PIO2_9 —** General purpose digital input/output pin.
					I	-	**CT32B1_CAP1 —** Capture input, channel 1 for 32-bit timer 1.
					O	-	**CT32B1_MAT1 —** Match output, channel 1 for 32-bit timer 1.
PIO2_10/ CT32B1_CAP2/ CT32B1_MAT2/TXD1	-	61	[2] [3]	no	I/O	I; PU	**PIO2_10 —** General purpose digital input/output pin.
					I	-	**CT32B1_CAP2 —** Capture input, channel 2 for 32-bit timer 1.
					O	-	**CT32B1_MAT2 —** Match output, channel 2 for 32-bit timer 1.
					O	-	**TXD1 —** Transmitter output for UART1.
PIO2_11/ CT32B1_CAP3/ CT32B1_MAT3/RXD1	-	62	[2] [3]	no	I/O	I; PU	**PIO2_11 —** General purpose digital input/output pin.
					I	-	**CT32B1_CAP3 —** Capture input, channel 3 for 32-bit timer 1.
					O	-	**CT32B1_MAT3 —** Match output, channel 3 for 32-bit timer 1.
					I	-	**RXD1 —** Receiver input for UART1.
PIO2_12/RXD1	-	13	[2] [3]	no	I/O	I; PU	**PIO2_12 —** General purpose digital input/output pin.
					I	-	**RXD1 —** Receiver input for UART1.
PIO2_13/TXD1	-	14	[2] [3]	no	I/O	I; PU	**PIO2_13 —** General purpose digital input/output pin.
					O	-	**TXD1 —** Transmitter output for UART1.
PIO2_14	-	15	[2] [3]	no	I/O	I; PU	**PIO2_14 —** General purpose digital input/output pin.
PIO2_15	-	16	[2] [3]	no	I/O	I; PU	**PIO2_15 —** General purpose digital input/output pin.
RTCXIN	46	58	[10]	-	I	-	Input to the 32 kHz oscillator circuit.
RTCXOUT	45	57	[10]	-	O	-	Output from the 32 kHz oscillator amplifier.
XTALIN	1	1		-	I	-	Input to the system oscillator circuit and internal clock generator circuits.
XTALOUT	2	2		-	O	-	Output from the system oscillator amplifier.
VREF_CMP	3	3		-	I	-	Reference voltage for comparator.

Table 3. LPC122x pin description *…continued*

Symbol	Pin LQFP48	Pin LQFP64	Start logic input	Type	Reset state [1]	Description
$V_{DD(IO)}$	47	63	-	I	-	Input/output supply voltage.
$V_{DD(3V3)}$	44	56	-	I	-	3.3 V supply voltage to the internal regulator and the ADC. Also used as the ADC reference voltage.
V_{SSIO}	48	64	-	I	-	Ground.
V_{SS}	43	55	-	I	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled.

[2] 3.3 V tolerant, digital I/O pin; default: pull-up enabled, no hysteresis.

[3] If set to output, this normal-drive pin is in low mode by default.

[4] I^2C-bus pins; 5 V tolerant; open-drain; default: no pull-up/pull-down; no hysteresis.

[5] 3.3 V tolerant, digital I/O pin with $\overline{\text{RESET}}$ function; default: pull-up enabled, no hysteresis. An external pull-up resistor is required on this pin for the Deep power-down mode.

[6] 3.3 V tolerant, digital I/O pin with analog function; default: pull-up enabled, no hysteresis.

[7] If set to output, this normal-drive pin is in high mode by default.

[8] 3.3 V tolerant, digital I/O pin with analog function and WAKEUP function; default: pull-up enabled, no hysteresis.

[9] 3.3 V tolerant, high-drive digital I/O pin; default: pull-up enabled, no hysteresis.

[10] If the RTC is not used, RTCXIN and RTCXOUT can be left floating.

To enable a peripheral function, find the corresponding port pin, or select a port pin if the function is multiplexed, and program the port pin's IOCONFIG register to enable that function. The primary SWD functions and $\overline{\text{RESET}}$ are the default functions on their pins after reset.

Table 4. Pin multiplexing

Peripheral	Function	Type	Available on ports:		
Analog comparators	ROSC	I/O	PIO0_29	-	-
	ACMP0_I0	I	PIO0_19	-	-
	ACMP0_I1	I	PIO0_20	-	-
	ACMP0_I2	I	PIO0_21	-	-
	ACMP0_I3	I	PIO0_22	-	-
	ACMP0_O	O	PIO0_27	-	-
	ACMP1_I0	I	PIO0_23	-	-
	ACMP1_I1	I	PIO0_24	-	-
	ACMP1_I2	I	PIO0_25	-	-
	ACMP1_I3	I	PIO0_26	-	-
	ACMP1_O	O	PIO0_28	-	-

- In the LPC122x, the NVIC supports 32 vectored interrupts. In addition, up to 12 of the individual GPIO inputs are NVIC-vector capable.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation.
- Non-maskable Interrupt (NMI) can be programmed to use any of the peripheral interrupts. The NMI is not available on an external pin.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any GPIO pin (total of up to 55 pins) regardless of the selected function, can be programmed to generate an interrupt on a level, a rising edge or falling edge, or both.

7.6 IOCONFIG block

The IOCONFIG block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.6.1 Features

- Programmable pull-up resistor.
- Programmable digital glitch filter.
- Programmable input inverter.
- Programmable drive current.
- Programmable open-drain mode.

7.7 Micro DMA controller

The micro DMA controller enables memory-to-memory, memory-to-peripheral, and peripheral-to-memory data transfers. The supported peripherals are: UART0 (transmit and receive), UART1 (transmit and receive), SSP/SPI (transmit and receive), ADC, RTC, 32-bit counter/timer 0 (match output channels 0 and 1), 32-bit counter/timer 1 (match output channels 0 and 1), 16-bit counter/timer 0 (match output channel 0), 16-bit counter/timer 1 (match output channel 0), comparator 0, comparator 1, GPIO0 to GPIO2.

7.7.1 Features

- Single AHB-Lite master for transferring data using a 32-bit address bus and 32-bit data bus.
- 21 DMA channels.
- Handshake signals and priority level programmable for each channel.
- Each priority level arbitrates using a fixed priority that is determined by the DMA channel number.

- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- The I^2C-bus controller supports multiple address recognition and a bus monitor mode.

7.13 10-bit ADC

The LPC122x contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

7.13.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to $V_{DD(3V3)}$.
- 10-bit conversion time of 257 kHz.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or counter/timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

7.14 Comparator block

The comparator block consists of two analog comparators.

7.14.1 Features

- Up to six selectable external sources per comparator; fully configurable on either positive or negative comparator input channels.
- BOD 0.9 V internal reference voltage selectable on both comparators; configurable on either positive or negative comparator input channels.
- 32-stage voltage ladder internal reference voltage selectable on both comparators; configurable on either positive or negative comparator input channels.
- Voltage ladder source voltage is selectable from an external pin or an internal 3.3 V voltage rail if external power source is not available.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Relaxation oscillator circuitry output for a feedback 555-style timer application.
- Common interrupt connected to NVIC.
- Comparator outputs selectable as synchronous or asynchronous.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL. The ARM processor clock frequency is referred to as CCLK elsewhere in this document.

7.18.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 7.8 kHz and 1.7 MHz. The frequency spread over processing and temperature is ±40 %.

7.18.2 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.18.3 Clock output

The LPC122x features a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.18.4 Wake-up process

The LPC122x begin operation at power-up and when awakened from Deep power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

7.18.5 Power control

The LPC122x support a variety of power control features. There are three special modes of processor power reduction: Sleep mode, Deep-sleep mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.18.5.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.18.5.2 Deep-sleep mode

In Deep-sleep mode, the chip is in Sleep mode, and in addition all analog blocks are shut down. As an exception, the user has the option to keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection. Deep-sleep mode allows for additional power savings.

The GPIO pins PIO0_0 to PIO0_11 (up to 12 pins total) and the RTC match interrupt can serve as a wake-up input to the start logic to wake up the chip from Deep-sleep mode.

Unless the watchdog oscillator is selected to run in Deep-sleep mode, the clock source should be switched to IRC before entering Deep-sleep mode, because the IRC can be switched on and off glitch-free.

7.18.5.3 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip with the exception of the Real Time Clock, the four general-purpose registers, and the WAKEUP pin. The LPC122x can wake up from Deep power-down mode via the WAKEUP pin or the RTC match interrupt.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. The $\overline{\text{RESET}}$ pin must also be held HIGH to prevent it from floating while in Deep power-down mode.

7.19 System control

7.19.1 Start logic

The start logic connects external pins to corresponding interrupts in the NVIC. Each pin shown in Table 3 as input to the start logic has an individual interrupt in the NVIC interrupt vector table. The start logic pins can serve as external interrupt pins when the chip is running. In addition, an input signal on the start logic pins can wake up the chip from Deep-sleep mode when all clocks are shut down.

The start logic must be configured in the system configuration block and in the NVIC before being used.

7.19.2 Reset

Reset has four sources on the LPC122x: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

An external pull-up resistor is required on the $\overline{\text{RESET}}$ pin if Deep power-down mode is used.

7.19.3 Brownout detection

The LPC122x includes four levels for monitoring the voltage on the $V_{DD(3V3)}$ pin. If this voltage falls below one of the four selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register. An additional threshold level can be selected to cause a forced reset of the chip.

7.19.4 Code security (Code Read Protection - CRP)

This feature of the LPC122x allows user to enable different levels of security in the system so that access to the on-chip flash and use of the SWD and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of Code Read Protection:

1. CRP1 disables access to chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_12 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_12 for valid user code can be disabled.

7.19.5 APB interface

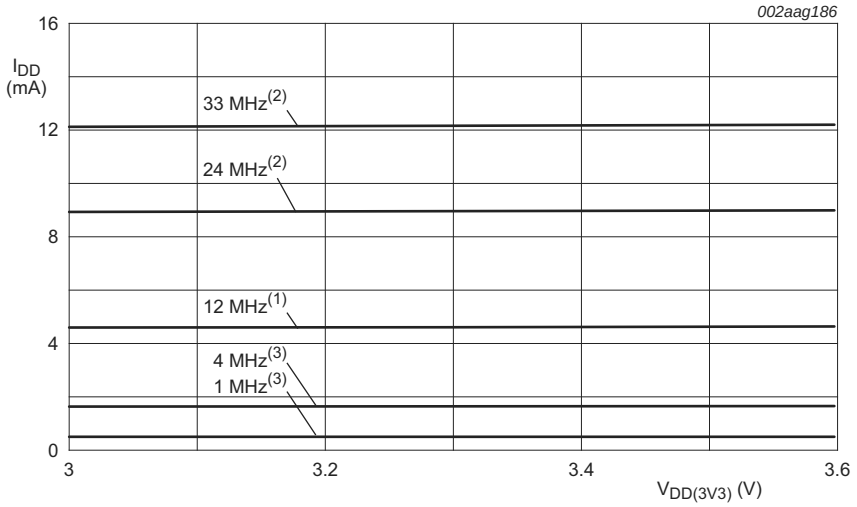
The APB peripherals are located on one APB bus.

7.19.6 AHB-Lite

The AHB-Lite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the Boot ROM.

7.19.7 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs.



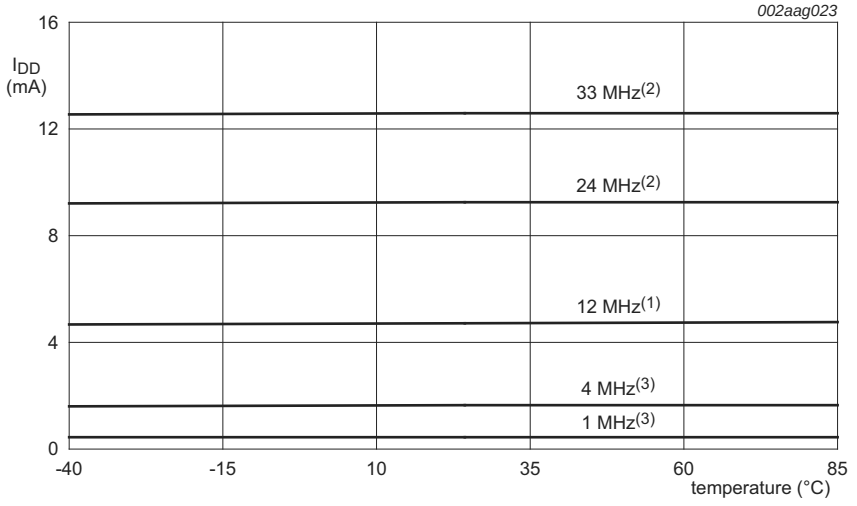
Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

(3) System oscillator enabled; IRC and system PLL disabled.

Fig 6. Active mode: Typical supply current I_{DD} versus supply voltage $V_{DD(3V3)}$ for different system clock frequencies (all peripherals disabled)



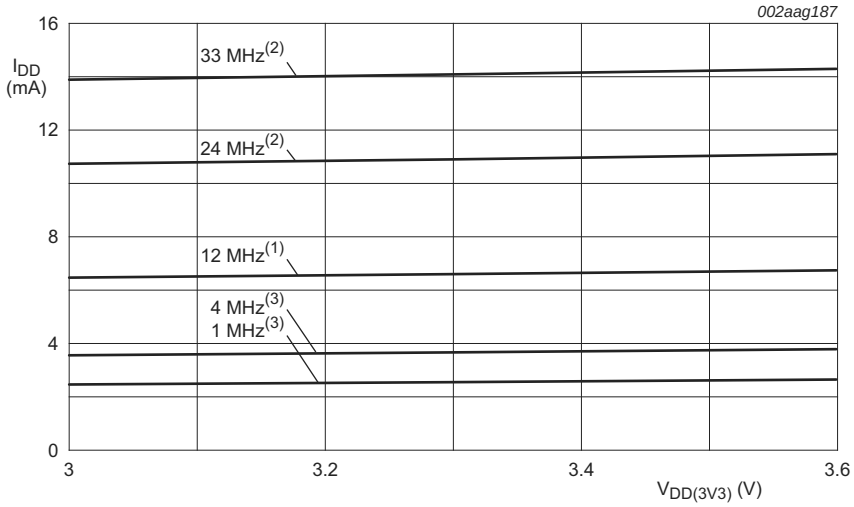
Conditions: $V_{DD(3V3)}$ = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

(3) System oscillator enabled; IRC and system PLL disabled.

Fig 7. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (peripherals disabled)



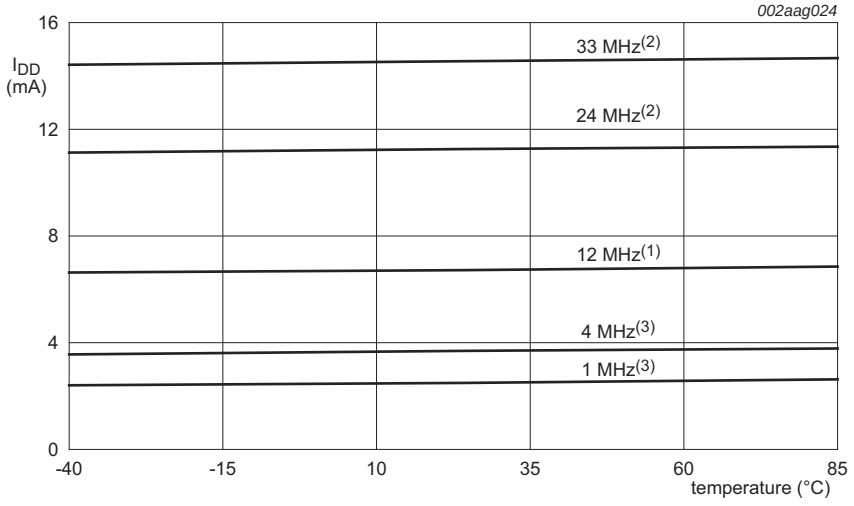
Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals enabled in the SYSAHBCLKCTRL register.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

(3) System oscillator enabled with external clock input; IRC and system PLL disabled.

Fig 8. Active mode: Typical supply current I_{DD} versus supply voltage $V_{DD(3V3)}$ for different system clock frequencies (all peripherals enabled)



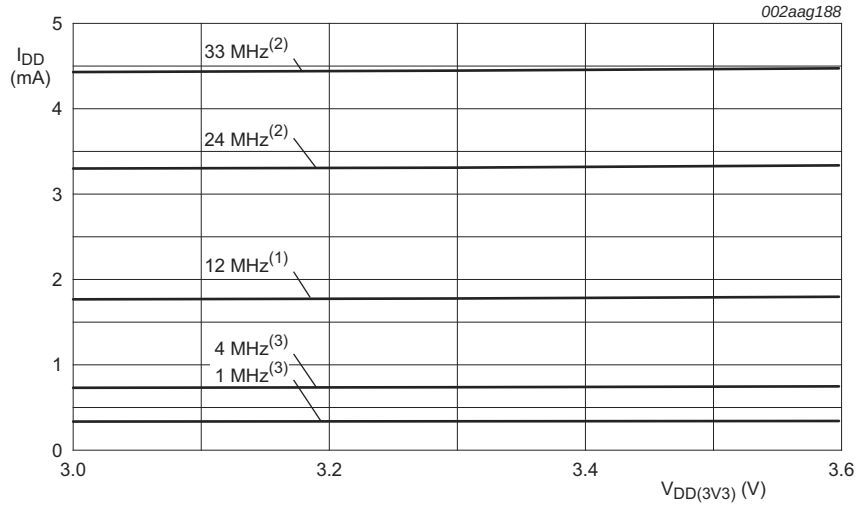
Conditions: $V_{DD(3V3)}$ = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals enabled in the SYSAHBCLKCTRL register.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

(3) System oscillator enabled with external clock input; IRC and system PLL disabled.

Fig 9. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (peripherals enabled)



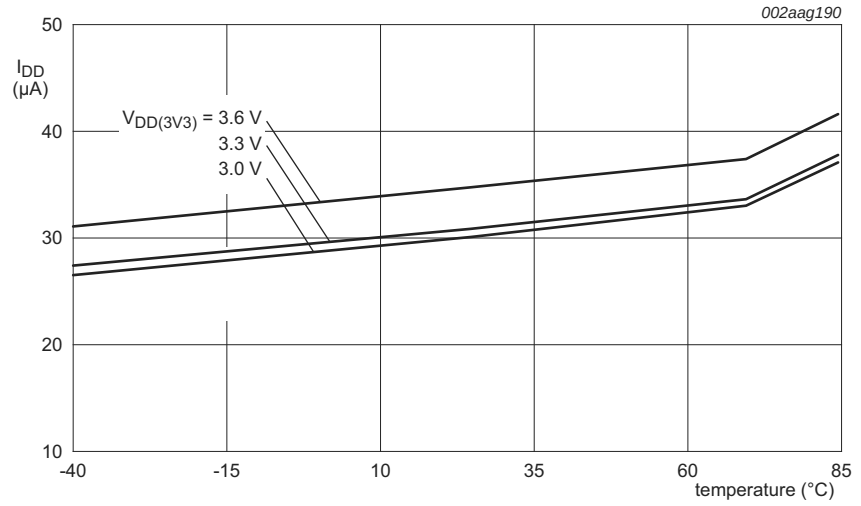
Conditions: $V_{DD(3V3)}$ = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

(3) System oscillator enabled with external clock input; IRC and system PLL disabled.

Fig 10. Sleep mode: Typical supply current I_{DD} versus supply voltage $V_{DD(3V3)}$ for different system clock frequencies



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register

Fig 11. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages $V_{DD(3V3)}$

10.5 BOD static characteristics

Table 10. BOD static characteristics[1]
T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1				
		assertion	-	2.25	-	V
		de-assertion	-	2.39	-	V
		interrupt level 2				
		assertion	-	2.54	-	V
		de-assertion	-	2.67	-	V
		interrupt level 3				
		assertion	-	2.83	-	V
		de-assertion	-	2.93	-	V
		reset level 1				
		assertion	-	2.04	-	V
		de-assertion	-	2.18	-	V
		reset level 2				
		assertion	-	2.34	-	V
		de-assertion	-	2.47	-	V
		reset level 3				
		assertion	-	2.62	-	V
		de-assertion	-	2.76	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC122x user manual*.

11. Dynamic characteristics

11.1 Power-up ramp conditions

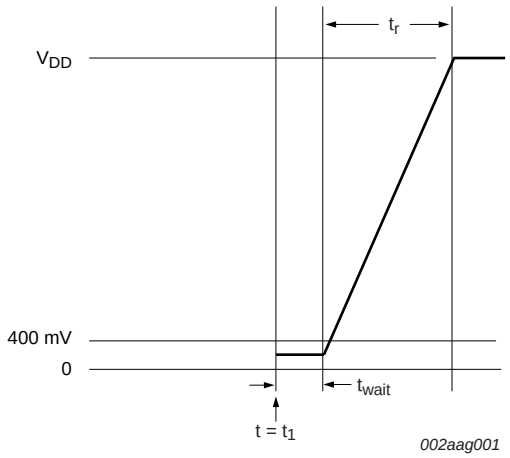
Table 11. Power-up characteristics

T_{amb} = –40 °C to +85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	at t = t_1: 0 < $V_I \leq$ 400 mV	[1]	0	-	500	ms
t_{wait}	wait time		[1][2]	12	-	-	µs
V_I	input voltage	at t = t_1 on pin V_{DD}		0	-	400	mV

[1] See Figure 20.

[2] The wait time specifies the time the power supply must be at levels below 400 mV before ramping up.



Condition: 0 < $V_I \leq$ 400 mV at start of power-up (t = t_1)

Fig 20. Power-up ramp

11.4 Internal oscillators

Table 14. Dynamic characteristic: internal oscillators
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12	12.12	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

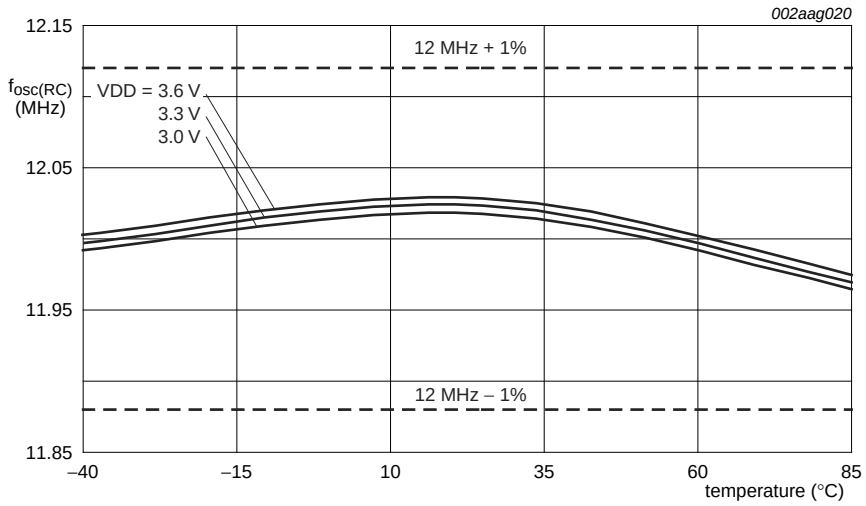


Fig 22. Internal RC oscillator frequency versus temperature

Table 15. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	7.8	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	1700	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +85 °C) is ±40 %.

[3] See the *LPC122x user manual*.

12.3 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for the LPC1227FBD64/301 in Table 17.

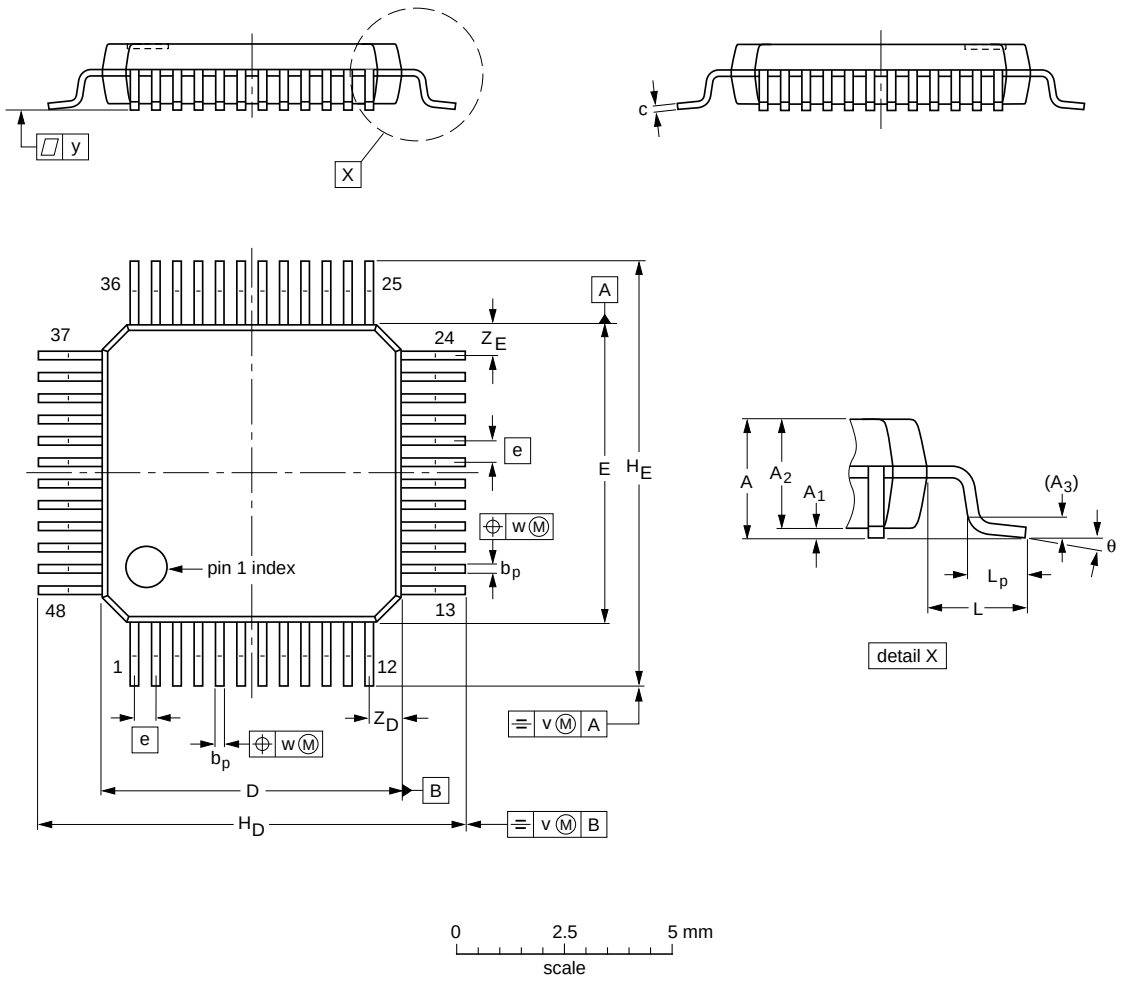
Table 17. ElectroMagnetic Compatibility (EMC) for part LPC1227FBD64/301 (TEM-cell method)

V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =			Unit
		12 MHz	24 MHz	33 MHz	
Input clock: IRC (12 MHz)					
maximum peak level	150 kHz - 30 MHz	−4.2	−3.8	−6.4	dBμV
	30 MHz - 150 MHz	7.3	5.4	9	dBμV
	150 MHz - 1 GHz	16.4	20.1	23.4	dBμV
IEC level[1]	-	M	L	L	-
Input clock: crystal oscillator (12 MHz)					
maximum peak level	150 kHz - 30 MHz	−4.8	−4	−6.6	dBμV
	30 MHz - 150 MHz	6.9	5.6	10	dBμV
	150 MHz - 1 GHz	16.3	20.3	22.3	dBμV
IEC level[1]	-	M	L	L	-

[1] IEC levels refer to *Appendix D in the IEC61967-2 Specification*.

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

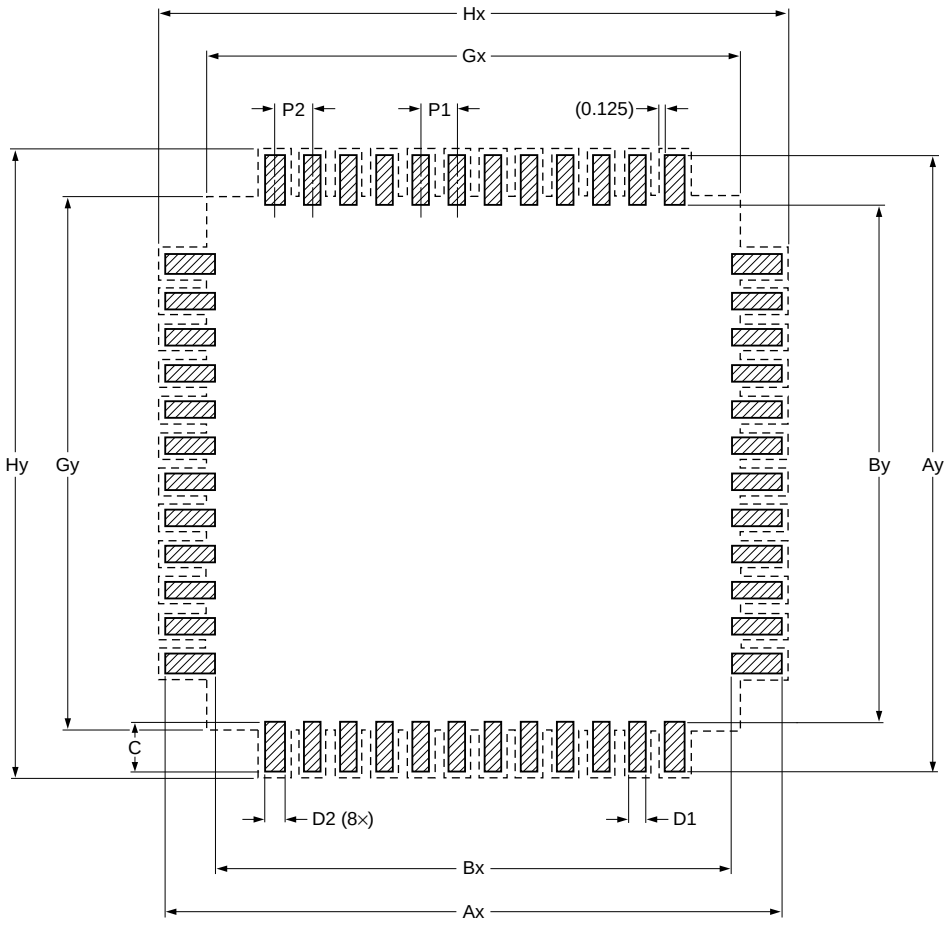
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 26. Package outline SOT313-2 (LQFP48)

14. Soldering

Footprint information for reflow soldering of LQFP48 package **SOT313-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	10.350	10.350	7.350	7.350	1.500	0.280	0.500	7.500	7.500	10.650	10.650

sot313-2_fr

Fig 27. Reflow soldering of the LQFP48 package

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 26 August 2011
Document identifier: LPC122X