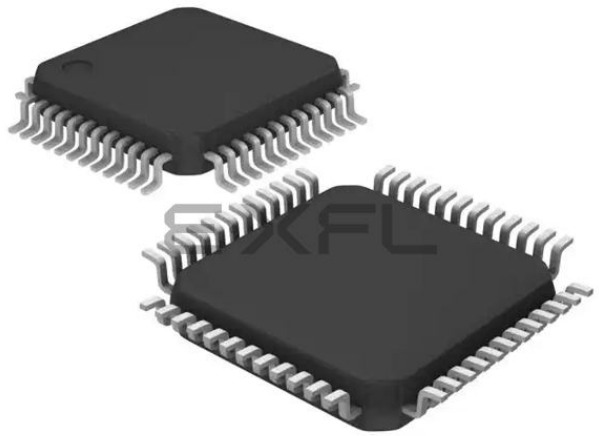

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 45MHz |
| Connectivity | I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, WDT |
| Number of I/O | 39 |
| Program Memory Size | 48KB (48K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1224fbd48-121-1 |

# 5. Block diagram

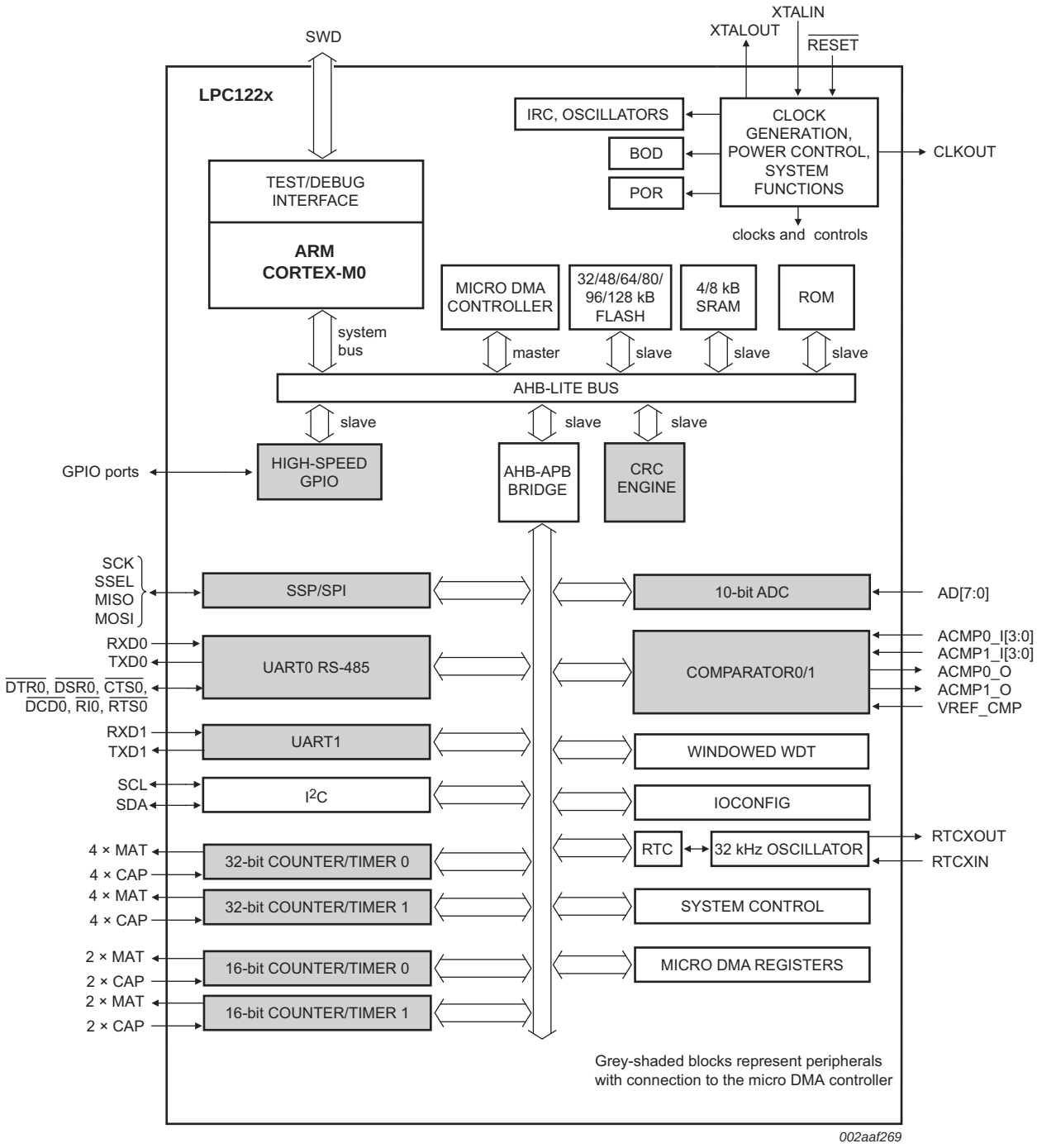



**Fig 1. LPC122x block diagram**

## 6.2 Pin description

All pins except the supply pins can have more than one function as shown in Table 3. The pin function is selected through the pin's IOCON register in the IOCONFIG block. The multiplexed functions (see Table 4) include the counter/timer inputs and outputs, the UART receive, transmit, and control functions, and the serial wire debug functions.

For each pin, the default function is listed first together with the pin's reset state.

**Table 3. LPC122x pin description**

| Symbol | Pin LQFP48 | Pin LQFP64 | | Start logic input | Type | Reset state [1] | Description |
|---|---|---|---|---|---|---|---|
| PIO0_0 to PIO0_31 | | | | | I/O | | **Port 0 —** Port 0 is a 32-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block. |
| PIO0_0/$\overline{\text{RTS0}}$ | 15 | 19 | [2] [3] | yes | I/O | I; PU | **PIO0_0 —** General purpose digital input/output pin. |
| | | | | | O | - | **$\overline{\text{RTS0}}$ —** Request To Send output for UART0. |
| PIO0_1/RXD0/ CT32B0_CAP0/ CT32B0_MAT0 | 16 | 20 | [2] [3] | yes | I/O | I; PU | **PIO0_1 —** General purpose digital input/output pin. |
| | | | | | I | - | **RXD0 —** Receiver input for UART0. |
| | | | | | I | - | **CT32B0_CAP0 —** Capture input, channel 0 for 32-bit timer 0. |
| | | | | | O | - | **CT32B0_MAT0 —** Match output, channel 0 for 32-bit timer 0. |
| PIO0_2/TXD0/ CT32B0_CAP1/ CT32B0_MAT1 | 17 | 21 | [2] [3] | yes | I/O | I; PU | **PIO0_2 —** General purpose digital input/output pin. |
| | | | | | O | - | **TXD0 —** Transmitter output for UART0. |
| | | | | | I | - | **CT32B0_CAP1 —** Capture input, channel 1 for 32-bit timer 0. |
| | | | | | O | - | **CT32B0_MAT1 —** Match output, channel 1 for 32-bit timer 0. |
| PIO0_3/$\overline{\text{DTR0}}$/ CT32B0_CAP2/ CT32B0_MAT2 | 18 | 22 | [2] [3] | yes | I/O | I; PU | **PIO0_3 —** General purpose digital input/output pin. |
| | | | | | O | - | **$\overline{\text{DTR0}}$ —** Data Terminal Ready output for UART0. |
| | | | | | I | - | **CT32B0_CAP2 —** Capture input, channel 2 for 32-bit timer 0. |
| | | | | | O | - | **CT32B0_MAT2 —** Match output, channel 2 for 32-bit timer 0. |
| PIO0_4/$\overline{\text{DSR0}}$/ CT32B0_CAP3/ CT32B0_MAT3 | 19 | 23 | [2] [3] | yes | I/O | I; PU | **PIO0_4 —** General purpose digital input/output pin. |
| | | | | | I | - | **$\overline{\text{DSR0}}$ —** Data Set Ready input for UART0. |
| | | | | | I | - | **CT32B0_CAP3 —** Capture input, channel 3 for 32-bit timer 0. |
| | | | | | O | - | **CT32B0_MAT3 —** Match output, channel 3 for 32-bit timer 0. |
| PIO0_5/$\overline{\text{DCD0}}$ | 20 | 24 | [2] [3] | yes | I/O | I; PU | **PIO0_5 —** General purpose digital input/output pin. |
| | | | | | I | - | **$\overline{\text{DCD0}}$ —** Data Carrier Detect input for UART0. |
| PIO0_6/$\overline{\text{RI0}}$/ CT32B1_CAP0/ CT32B1_MAT0 | 21 | 25 | [2] [3] | yes | I/O | I; PU | **PIO0_6 —** General purpose digital input/output pin. |
| | | | | | I | - | **$\overline{\text{RI0}}$ —** Ring Indicator input for UART0. |
| | | | | | I | - | **CT32B1_CAP0 —** Capture input, channel 0 for 32-bit timer 1. |
| | | | | | O | - | **CT32B1_MAT0 —** Match output, channel 0 for 32-bit timer 1. |

**Table 3. LPC122x pin description** *…continued*

| Symbol | Pin LQFP48 | Pin LQFP64 | | Start logic input | Type | Reset state [1] | Description |
|---|---|---|---|---|---|---|---|
| PIO0_17/MOSI | 32 | 44 | [2] [3] | no | I/O | I; PU | **PIO0_17 —** General purpose digital input/output pin. |
| | | | | | I/O | - | **MOSI —** Master Out Slave In for SSP/SPI. |
| PIO0_18/SWCLK/ CT32B0_CAP0/ CT32B0_MAT0 | 33 | 45 | [2] [3] | no | I/O | I; PU | **PIO0_18 —** General purpose digital input/output pin. |
| | | | | | I | - | **SWCLK —** Serial wire clock, alternate location. |
| | | | | | I | - | **CT32B0_CAP0 —** Capture input, channel 0 for 32-bit timer 0. |
| | | | | | O | - | **CT32B0_MAT0 —** Match output, channel 0 for 32-bit timer 0. |
| PIO0_19/ACMP0_I0/ CT32B0_CAP1/ CT32B0_MAT1 | 4 | 4 | [6] [7] | no | I/O | I; PU | **PIO0_19 —** General purpose digital input/output pin. |
| | | | | | I | - | **ACMP0_I0 —** Input 0 for comparator 0. |
| | | | | | I | - | **CT32B0_CAP1 —** Capture input, channel 1 for 32-bit timer 0. |
| | | | | | O | - | **CT32B0_MAT1 —** Match output, channel 1 for 32-bit timer 0 |
| PIO0_20/ACMP0_I1/ CT32B0_CAP2/ CT32B0_MAT2 | 5 | 5 | [6] [7] | no | I/O | I; PU | **PIO0_20 —** General purpose digital input/output pin. |
| | | | | | I | - | **ACMP0_I1 —** Input 1 for comparator 0. |
| | | | | | I | - | **CT32B0_CAP2 —** Capture input, channel 2 for 32-bit timer 0. |
| | | | | | O | - | **CT32B0_MAT2 —** Match output, channel 2 for 32-bit timer 0. |
| PIO0_21/ACMP0_I2/ CT32B0_CAP3/ CT32B0_MAT3 | 6 | 6 | [6] [7] | no | I/O | I; PU | **PIO0_21 —** General purpose digital input/output pin. |
| | | | | | I | - | **ACMP0_I2 —** Input 2 for comparator 0. |
| | | | | | I | - | **CT32B0_CAP3 —** Capture input, channel 3 for 32-bit timer 0. |
| | | | | | O | - | **CT32B0_MAT3 —** Match output, channel 3 for 32-bit timer 0. |
| PIO0_22/ACMP0_I3 | 7 | 7 | [6] [7] | no | I/O | I; PU | **PIO0_22 —** General purpose digital input/output pin. |
| | | | | | I | - | **ACMP0_I3 —** Input 3 for comparator 0. |
| PIO0_23/ ACMP1_I0/ CT32B1_CAP0/ CT32B1_MAT0 | 8 | 8 | [6] [7] | no | I/O | I; PU | **PIO0_23 —** General purpose digital input/output pin. |
| | | | | | I | - | **ACMP1_I0 —** Input 0 for comparator 1. |
| | | | | | I | - | **CT32B1_CAP0 —** Capture input, channel 0 for 32-bit timer 1. |
| | | | | | O | - | **CT32B1_MAT0 —** Match output, channel 0 for 32-bit timer 1. |
| PIO0_24/ACMP1_I1/ CT32B1_CAP1/ CT32B1_MAT1 | 9 | 9 | [6] [7] | no | I/O | I; PU | **PIO0_24 —** General purpose digital input/output pin. |
| | | | | | I | - | **ACMP1_I1 —** Input 1 for comparator 1. |
| | | | | | I | - | **CT32B1_CAP1 —** Capture input, channel 1 for 32-bit timer 1. |
| | | | | | O | - | **CT32B1_MAT1 —** Match output, channel 1 for 32-bit timer 1. |
| SWDIO/ACMP1_I2/ CT32B1_CAP2/ CT32B1_MAT2/ PIO0_25 | 10 | 10 | [6] [7] | no | I/O | I; PU | **SWDIO —** Serial wire debug input/output, default location. |
| | | | | | I | - | **ACMP1_I2 —** Input 2 for comparator 1. |
| | | | | | I | - | **CT32B1_CAP2 —** Capture input, channel 2 for 32-bit timer 1. |
| | | | | | O | - | **CT32B1_MAT2 —** Match output, channel 2 for 32-bit timer 1. |
| | | | | | I/O | - | **PIO0_25 —** General purpose digital input/output pin. |
| SWCLK/ACMP1_I3/ CT32B1_CAP3/ CT32B1_MAT3/ PIO0_26 | 11 | 11 | [6] [7] | no | I | I; PU | **SWCLK —** Serial wire clock, default location. |
| | | | | | I | - | **ACMP1_I3 —** Input 3 for comparator 1. |
| | | | | | I | - | **CT32B1_CAP3 —** Capture input, channel 3 or 32-bit timer 1. |
| | | | | | O | - | **CT32B1_MAT3 —** Match output, channel 3 for 32-bit timer 1. |
| | | | | | I/O | | **PIO0_26 —** General purpose digital input/output pin. |

**Table 3. LPC122x pin description** *…continued*

| Symbol | Pin LQFP48 | Pin LQFP64 | Start logic input | Type | Reset state [1] | Description |
|---|---|---|---|---|---|---|
| $V_{DD(IO)}$ | 47 | 63 | - | I | - | Input/output supply voltage. |
| $V_{DD(3V3)}$ | 44 | 56 | - | I | - | 3.3 V supply voltage to the internal regulator and the ADC. Also used as the ADC reference voltage. |
| $V_{SSIO}$ | 48 | 64 | - | I | - | Ground. |
| $V_{SS}$ | 43 | 55 | - | I | - | Ground. |

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled.

[2] 3.3 V tolerant, digital I/O pin; default: pull-up enabled, no hysteresis.

[3] If set to output, this normal-drive pin is in low mode by default.

[4] $I^2C$-bus pins; 5 V tolerant; open-drain; default: no pull-up/pull-down; no hysteresis.

[5] 3.3 V tolerant, digital I/O pin with $\overline{\text{RESET}}$ function; default: pull-up enabled, no hysteresis. An external pull-up resistor is required on this pin for the Deep power-down mode.

[6] 3.3 V tolerant, digital I/O pin with analog function; default: pull-up enabled, no hysteresis.

[7] If set to output, this normal-drive pin is in high mode by default.

[8] 3.3 V tolerant, digital I/O pin with analog function and WAKEUP function; default: pull-up enabled, no hysteresis.

[9] 3.3 V tolerant, high-drive digital I/O pin; default: pull-up enabled, no hysteresis.

[10] If the RTC is not used, RTCXIN and RTCXOUT can be left floating.

To enable a peripheral function, find the corresponding port pin, or select a port pin if the function is multiplexed, and program the port pin's IOCONFIG register to enable that function. The primary SWD functions and $\overline{\text{RESET}}$ are the default functions on their pins after reset.

**Table 4. Pin multiplexing**

| Peripheral | Function | Type | Available on ports: | | |
|---|---|---|---|---|---|
| Analog comparators | ROSC | I/O | PIO0_29 | - | - |
| | ACMP0_I0 | I | PIO0_19 | - | - |
| | ACMP0_I1 | I | PIO0_20 | - | - |
| | ACMP0_I2 | I | PIO0_21 | - | - |
| | ACMP0_I3 | I | PIO0_22 | - | - |
| | ACMP0_O | O | PIO0_27 | - | - |
| | ACMP1_I0 | I | PIO0_23 | - | - |
| | ACMP1_I1 | I | PIO0_24 | - | - |
| | ACMP1_I2 | I | PIO0_25 | - | - |
| | ACMP1_I3 | I | PIO0_26 | - | - |
| | ACMP1_O | O | PIO0_28 | - | - |

- Comparator outputs connect to two timers, allowing for the recording of comparison event time stamps.

## 7.15 General purpose external event counter/timers

The LPC122x includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes up to four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

### 7.15.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- Up to four capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Supports timed DMA requests.

## 7.16 Windowed WatchDog timer (WWDT)

The purpose of the watchdog is to reset the microcontroller within a windowed amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to ‘feed’ (or reload) the watchdog within a predetermined amount of time.

### 7.16.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Safe operation: can be locked by software to be always on.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.

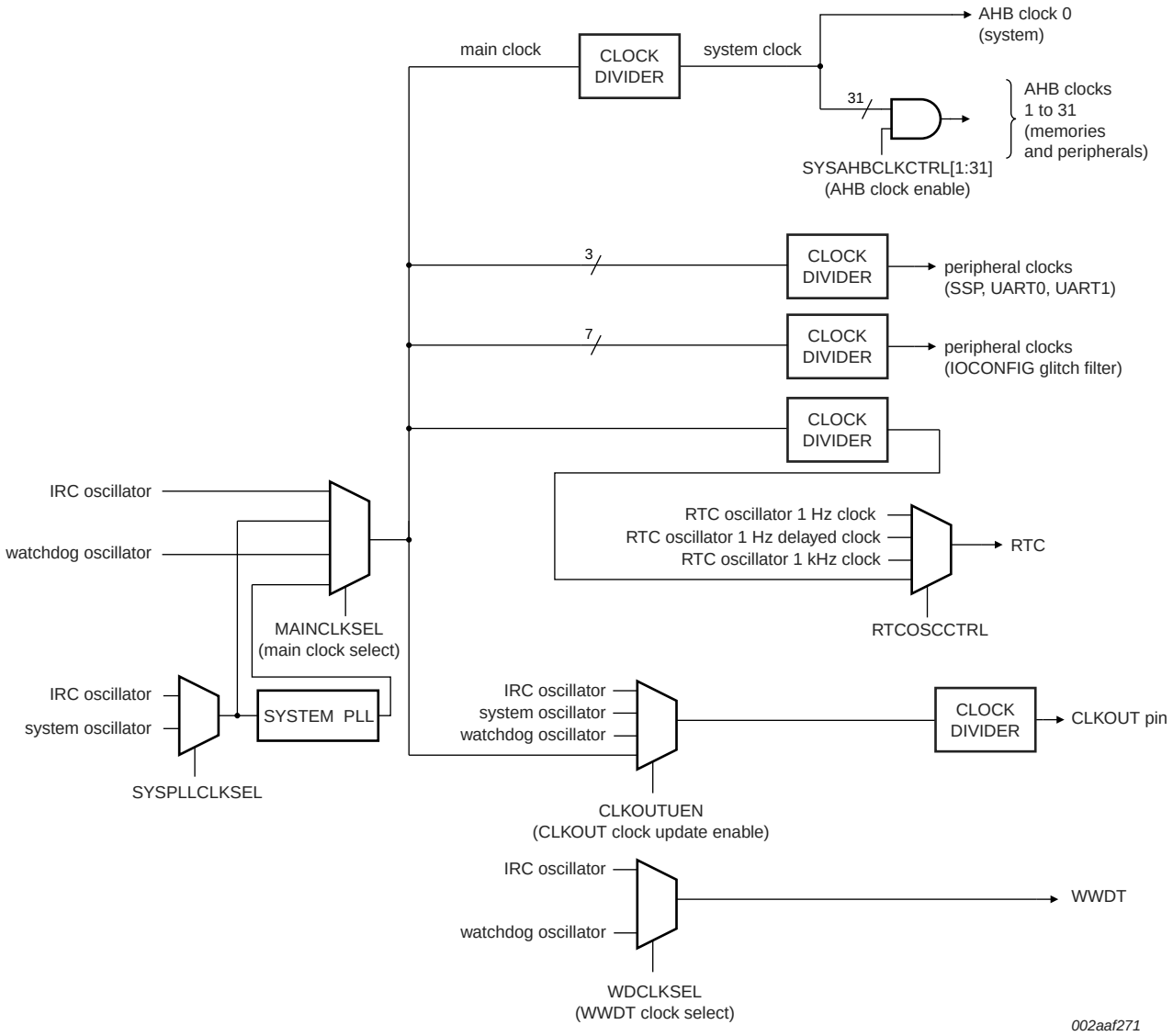



**Fig 5. LPC122x clocking generation block diagram**

### 7.18.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC122x use the IRC as the clock source. Software may later switch to one of the other available clock sources.

### 7.18.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL.

An external pull-up resistor is required on the $\overline{\text{RESET}}$ pin if Deep power-down mode is used.

### 7.19.3 Brownout detection

The LPC122x includes four levels for monitoring the voltage on the $V_{DD(3V3)}$ pin. If this voltage falls below one of the four selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register. An additional threshold level can be selected to cause a forced reset of the chip.

### 7.19.4 Code security (Code Read Protection - CRP)

This feature of the LPC122x allows user to enable different levels of security in the system so that access to the on-chip flash and use of the SWD and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of Code Read Protection:

1. CRP1 disables access to chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_12 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

**CAUTION**

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_12 for valid user code can be disabled.

### 7.19.5 APB interface

The APB peripherals are located on one APB bus.

### 7.19.6 AHB-Lite

The AHB-Lite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the Boot ROM.

### 7.19.7 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs.

## 7.20 Emulation and debugging

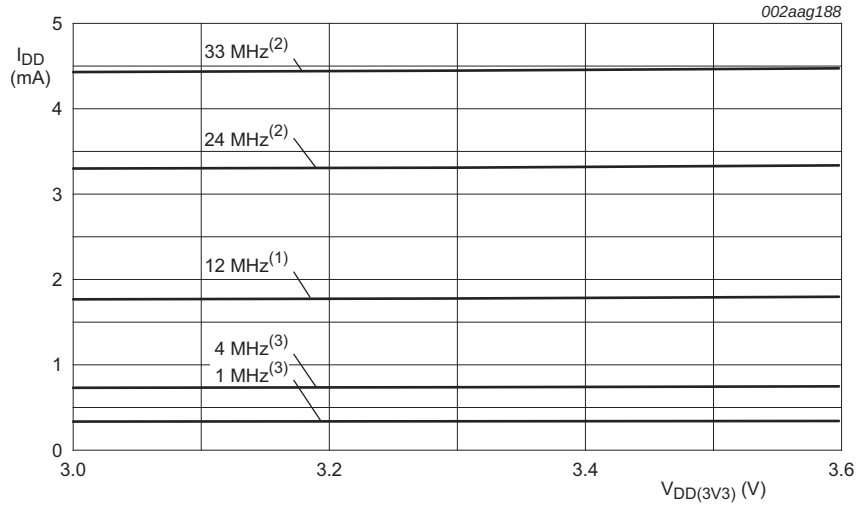
Debug functions are integrated into the ARM Cortex-M0. Serial wire debug is supported.

## 7.21 Integer division routines

The LPC122x contain performance-optimized integer division routines with support for up to 32-bit width in the numerator and denominator. Routines for signed and unsigned division and division with remainder are available. The integer division routines are ROM-based to reduce code-size.

**Table 7. Static characteristics** *…continued*
*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | LOW-level input voltage | | | - | - | $0.3V_{DD(IO)}$ | V |
| $V_{hys}$ | hysteresis voltage | | | - | 0.4 | - | V |
| $V_{OH}$ | HIGH-level output voltage | low mode; $I_{OH}$ = −2 mA | | $V_{DD(IO)}$ − 0.4 | - | - | V |
| | | high mode; $I_{OH}$ = −4 mA | | $V_{DD(IO)}$ − 0.4 | - | - | V |
| $V_{OL}$ | LOW-level output voltage | low mode; $I_{OL}$ = 2 mA | | - | - | 0.4 | V |
| | | high mode; $I_{OL}$ = 4 mA | | | | 0.4 | |
| $I_{OH}$ | HIGH-level output current | low mode; $V_{OH} = V_{DD(IO)}$ − 0.4 V | | −2 | - | - | mA |
| | | high mode; $V_{OH} = V_{DD(IO)}$ − 0.4 V | | −4 | - | - | mA |
| $I_{OL}$ | LOW-level output current | low mode; $V_{OL}$ = 0.4 V | | 2 | - | - | mA |
| | | high mode; $V_{OL}$ = 0.4 V | | 4 | - | - | mA |
| $I_{OHS}$ | HIGH-level short-circuit output current | $V_{OH}$ = 0 V | [5] | - | - | −45 | mA |
| $I_{OLS}$ | LOW-level short-circuit output current | $V_{OL} = V_{DDA}$ | [5] | - | - | 50 | mA |
| $I_{pu}$ | pull-up current | $V_I$ = 0 V | | −50 | −80 | −100 | μA |
| **High-drive output pins (PIO0_27, PIO0_28, PIO0_29, PIO0_12)** | | | | | | | |
| $I_{IL}$ | LOW-level input current | $V_I$ = 0 V; | | - | - | 100 | nA |
| $I_{IH}$ | HIGH-level input current | $V_I = V_{DD(IO)}$; | | - | - | 100 | nA |
| $I_{OZ}$ | OFF-state output current | $V_O$ = 0 V; $V_O = V_{DD(IO)}$; | | - | - | 100 | nA |
| $V_I$ | input voltage | pin configured to provide a digital function | [2][3] [4] | 0 | - | $V_{DD(IO)}$ | V |
| $V_O$ | output voltage | output active | | 0 | - | $V_{DD(IO)}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | $0.7V_{DD(IO)}$ | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | - | - | $0.3V_{DD(IO)}$ | - | - |
| $V_{hys}$ | hysteresis voltage | | | | - | - | V |
| $V_{OH}$ | HIGH-level output voltage | low mode; $I_{OH}$ = −20 mA | | $V_{DD(IO)}$ − 0.7 | - | - | V |
| | | high mode; $I_{OH}$ = −28 mA | | $V_{DD(IO)}$ − 0.7 | - | - | V |
| $V_{OL}$ | LOW-level output voltage | low mode; $I_{OL}$ = 12 mA | | - | - | 0.4 | V |
| | | high mode; $I_{OL}$ = 18 mA | | - | - | 0.4 | V |



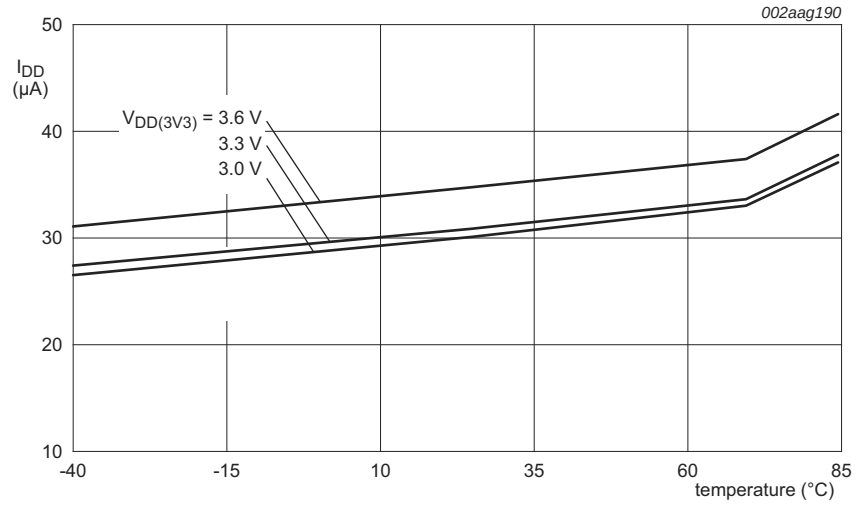

Conditions: $V_{DD(3V3)}$ = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

(3) System oscillator enabled with external clock input; IRC and system PLL disabled.

**Fig 10. Sleep mode: Typical supply current $I_{DD}$ versus supply voltage $V_{DD(3V3)}$ for different system clock frequencies**




Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register

**Fig 11. Deep-sleep mode: Typical supply current $I_{DD}$ versus temperature for different supply voltages $V_{DD(3V3)}$**

## 10.4 ADC characteristics

**Table 9. ADC static characteristics**

*$T_{amb}$ = −40 °C to +85 °C unless otherwise specified; ADC frequency 9 MHz, $V_{DD(3V3)}$ = 3.0 V to 3.6 V.*

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IA}$ | analog input voltage | | 0 | - | $V_{DD(3V3)}$ | V |
| $C_{ia}$ | analog input capacitance | | - | - | 1 | pF |
| $E_D$ | differential linearity error | [2][3][4] | - | - | ± 1 | LSB |
| $E_{L(adj)}$ | integral non-linearity | [2][5] | - | - | ± 2.5 | LSB |
| $E_O$ | offset error | [2][6] | - | - | ± 1 | LSB |
| $E_G$ | gain error | [2][7] | - | - | ± 3 | LSB |
| $E_T$ | absolute error | [2][8] | - | - | ± 3 | LSB |
| $f_{c(ADC)}$ | ADC conversion frequency | | - | - | 257 | kHz |
| $R_i$ | input resistance | [9][10] | - | - | 3.9 | MΩ |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Conditions: $V_{SS}$ = 0 V, $V_{DD(3V3)}$ = 3.3 V.

[3] The ADC is monotonic, there are no missing codes.

[4] The differential linearity error ($E_D$) is the difference between the actual step width and the ideal step width. See Figure 19.

[5] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 19.

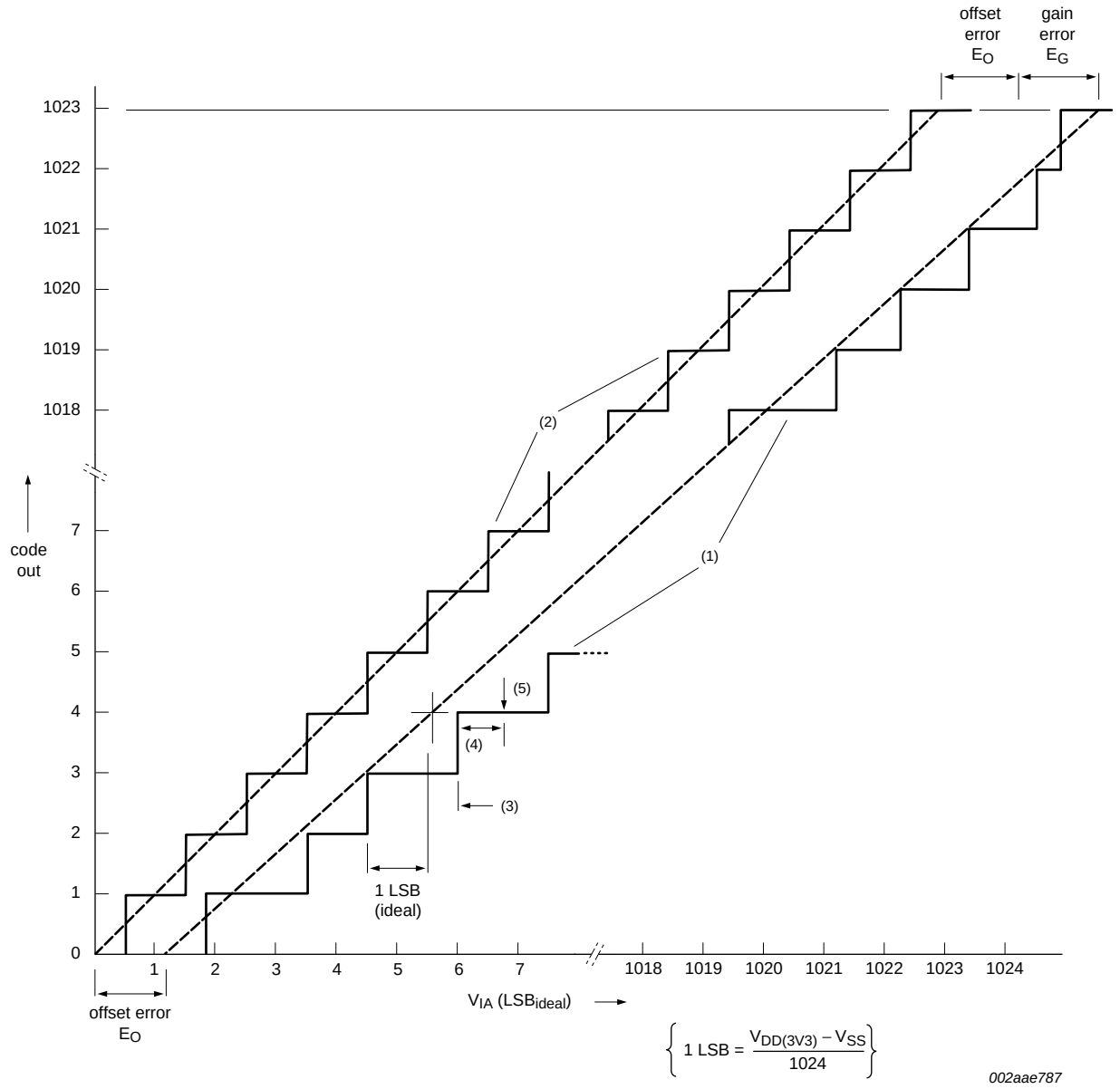
[6] The offset error ($E_O$) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 19.

[7] The gain error ($E_G$) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 19.

[8] The absolute error ($E_T$) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 19.

[9] $T_{amb}$ = 25 °C; maximum sampling frequency $f_s$ = 257 kHz and analog input capacitance $C_{ia}$ = 1 pF.

[10] Input resistance $R_i$ depends on the sampling frequency fs: $R_i = 1 / (f_s \times C_{ia})$.




(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error ($E_D$).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

**Fig 19. ADC characteristics**

## 10.5 BOD static characteristics

**Table 10. BOD static characteristics[1]**
$T_{amb}$ = 25 °C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{th}$ | threshold voltage | interrupt level 1 | | | | |
| | | assertion | - | 2.25 | - | V |
| | | de-assertion | - | 2.39 | - | V |
| | | interrupt level 2 | | | | |
| | | assertion | - | 2.54 | - | V |
| | | de-assertion | - | 2.67 | - | V |
| | | interrupt level 3 | | | | |
| | | assertion | - | 2.83 | - | V |
| | | de-assertion | - | 2.93 | - | V |
| | | reset level 1 | | | | |
| | | assertion | - | 2.04 | - | V |
| | | de-assertion | - | 2.18 | - | V |
| | | reset level 2 | | | | |
| | | assertion | - | 2.34 | - | V |
| | | de-assertion | - | 2.47 | - | V |
| | | reset level 3 | | | | |
| | | assertion | - | 2.62 | - | V |
| | | de-assertion | - | 2.76 | - | V |

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC122x user manual*.

# 11. Dynamic characteristics

## 11.1 Power-up ramp conditions

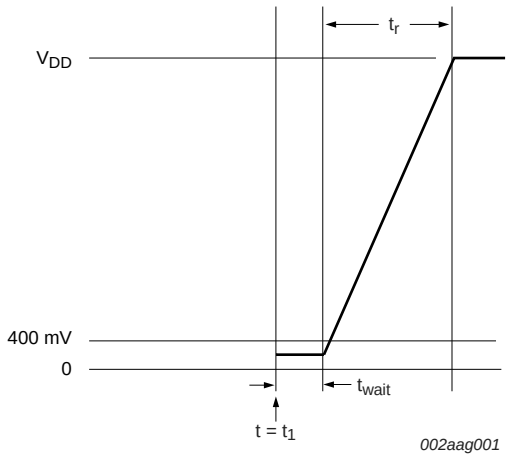
**Table 11. Power-up characteristics**

*$T_{amb}$ = –40 °C to +85 °C.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_r$ | rise time | at t = $t_1$: 0 < $V_I \leq$ 400 mV | [1] | 0 | - | 500 | ms |
| $t_{wait}$ | wait time | | [1][2] | 12 | - | - | µs |
| $V_I$ | input voltage | at t = $t_1$ on pin $V_{DD}$ | | 0 | - | 400 | mV |

[1] See Figure 20.

[2] The wait time specifies the time the power supply must be at levels below 400 mV before ramping up.




Condition: 0 < $V_I \leq$ 400 mV at start of power-up (t = $t_1$)

**Fig 20. Power-up ramp**

## 11.5 I²C-bus

**Table 16. Dynamic characteristic: I²C-bus pins**
*$T_{amb}$ = −40 °C to +85 °C.*[1]

| Symbol | Parameter | | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | | Standard-mode | 0 | 100 | kHz |
| | | | Fast-mode | 0 | 400 | kHz |
| | | | Fast-mode Plus | 0 | 1 | MHz |
| $t_f$ | fall time | [3][4][5][6] | of both SDA and SCL signals | - | 300 | ns |
| | | | Standard-mode | | | |
| | | | Fast-mode | $20 + 0.1 \times C_b$ | 300 | ns |
| | | | Fast-mode Plus | - | 120 | ns |
| $t_{LOW}$ | LOW period of the SCL clock | | Standard-mode | 4.7 | - | µs |
| | | | Fast-mode | 1.3 | - | µs |
| | | | Fast-mode Plus | 0.5 | - | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | | Standard-mode | 4.0 | - | µs |
| | | | Fast-mode | 0.6 | - | µs |
| | | | Fast-mode Plus | 0.26 | - | µs |
| $t_{HD;DAT}$ | data hold time | [2][3][7] | Standard-mode | 0 | - | µs |
| | | | Fast-mode | 0 | - | µs |
| | | | Fast-mode Plus | 0 | - | µs |
| $t_{SU;DAT}$ | data set-up time | [8][9] | Standard-mode | 250 | - | ns |
| | | | Fast-mode | 100 | - | ns |
| | | | Fast-mode Plus | 50 | - | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH}$(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[4] $C_b$ = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.

[5] The maximum $t_f$ for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage $t_f$ is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified $t_f$.

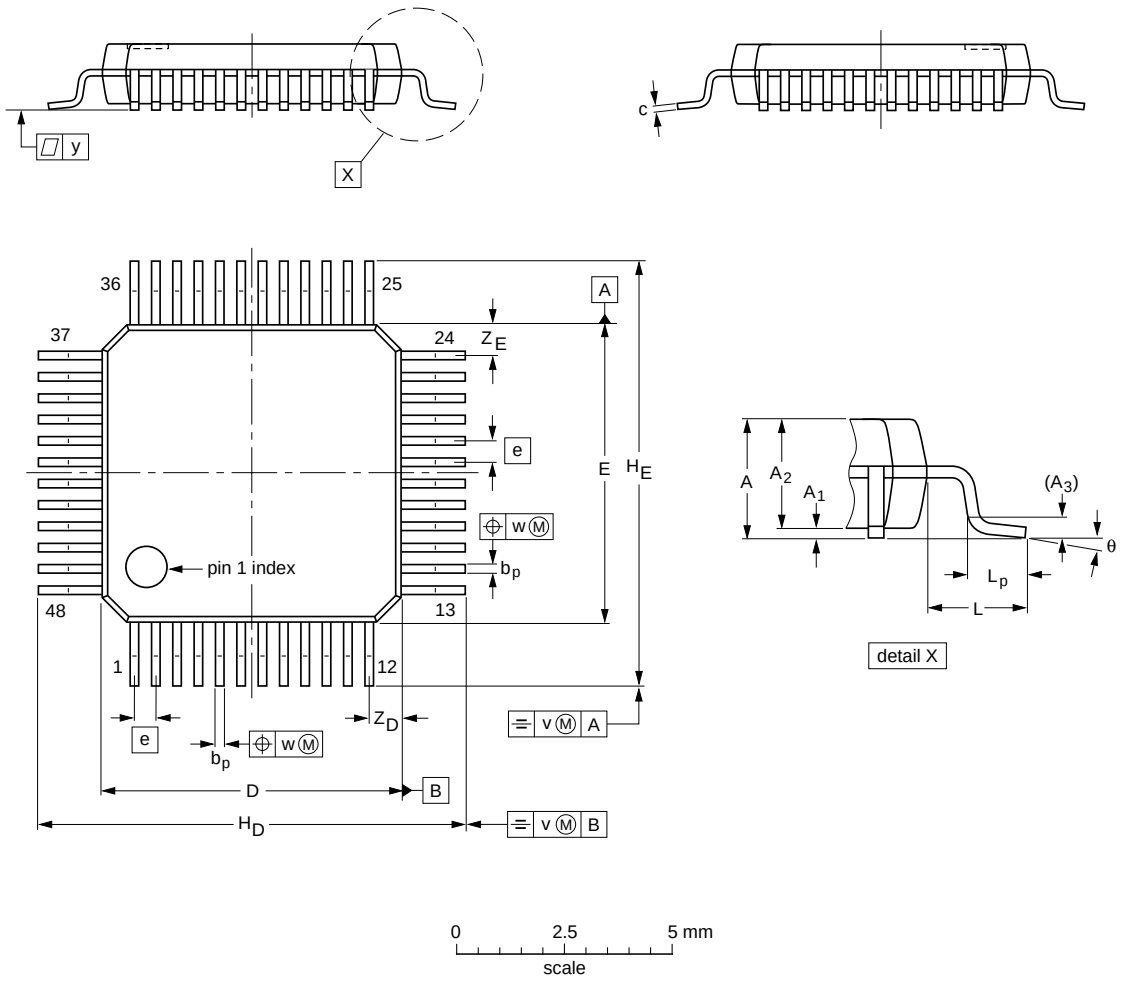
[6] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[7] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period ($t_{LOW}$) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[8] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[9] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

**LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm** **SOT313-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.6 | 0.20<br>0.05 | 1.45<br>1.35 | 0.25 | 0.27<br>0.17 | 0.18<br>0.12 | 7.1<br>6.9 | 7.1<br>6.9 | 0.5 | 9.15<br>8.85 | 9.15<br>8.85 | 1 | 0.75<br>0.45 | 0.2 | 0.12 | 0.1 | 0.95<br>0.55 | 0.95<br>0.55 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT313-2 | 136E05 | MS-026 | | | | ~~00-01-19~~<br>03-02-25 |

**Fig 26. Package outline SOT313-2 (LQFP48)**

# 15. Abbreviations

**Table 18. Abbreviations**

| Acronym | Description |
|---|---|
| ADC | Analog-to-Digital-Converter |
| AHB | Advanced High-performance Bus |
| APB | Advanced Peripheral Bus |
| BOD | BrownOut Detection |
| CCITT | Comité Consultatif International Téléphonique et Télégraphique |
| CRC | Cyclic Redundancy Check |
| DMA | Direct Memory Access |
| FIFO | First-In-First-Out |
| GPIO | General Purpose Input/Output |
| I/O | Input/Output |
| IrDA | Infrared Data Association |
| IRC | Internal Resistor-Capacitor |
| JEDEC | Joint Electron Devices Engineering Council |
| PLL | Phase-Locked Loop |
| SPI | Serial Peripheral Interface |
| SSI | Serial Synchronous Interface |
| SSP | Synchronous Serial Port |
| UART | Universal Asynchronous Receiver/Transmitter |

# 16. Revision history

**Table 19. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| LPC122X v.2 | 20110826 | Product data sheet | - | LPC122X v.1.2 |
| Modifications: | • Power consumption data updated in Table 7.<br>• Power consumption graphs added in Section 10.2.<br>• Electrical pin characteristics updated for all pins in Table 7 and Section 10.3.<br>• Parameter $R_i$ added to Table 9.<br>• EMC data added (Section 12.3).<br>• Parameter $V_I$ updated for $I^2C$-bus pins in Table 5.<br>• Section 11.1 “Power-up ramp conditions” added.<br>• Data sheet status updated to Product Data Sheet.<br>• SSP dynamic characteristics removed. | | | |
| LPC122X v.1.2 | 20110329 | Objective data sheet | - | LPC122X v.1.1 |
| Modifications: | • Figure 2 “Pin configuration LQFP64 package”: Pin RTCXIN changed to 58 and pin RTCXOUT changed to 57.<br>• Table 3 “LPC122x pin description”: In column Pin LQFP64, pin RTCXIN changed to 58 and pin RTCXOUT changed to 57. | | | |
| LPC122X v.1.1 | 20110221 | Objective data sheet | - | LPC122X v.1 |
| Modifications: | • Section 1 “General description”: Updated text.<br>• Section 2 “Features and benefits”: Updated text. | | | |
| LPC122X v.1 | 20110214 | Objective data sheet | - | - |

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## 17.4 Trademarks

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# 18. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 26 August 2011**
**Document identifier: LPC122X**