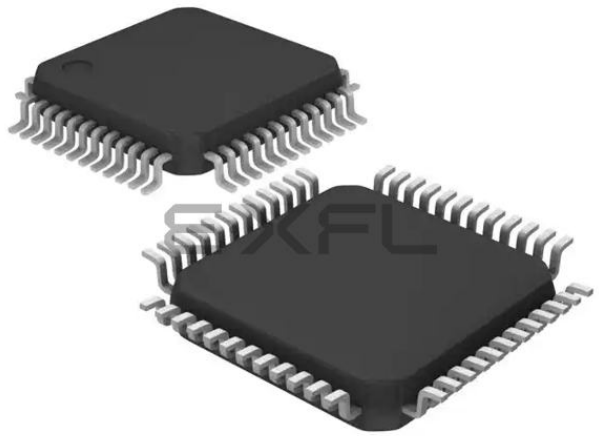

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 45MHz |
| Connectivity | I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, WDT |
| Number of I/O | 39 |
| Program Memory Size | 80KB (80K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1225fbd48-321-1 |

# 5. Block diagram

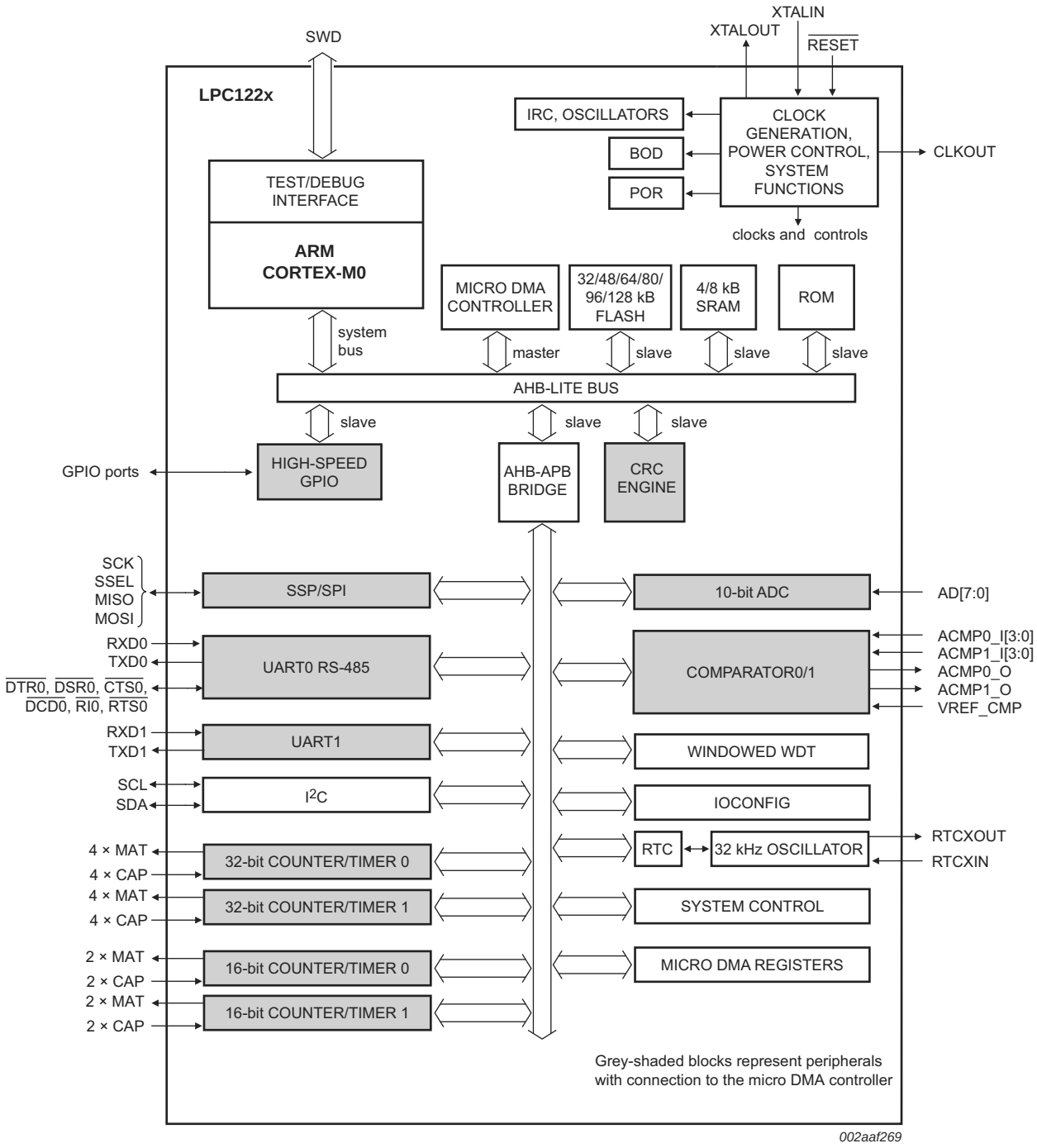
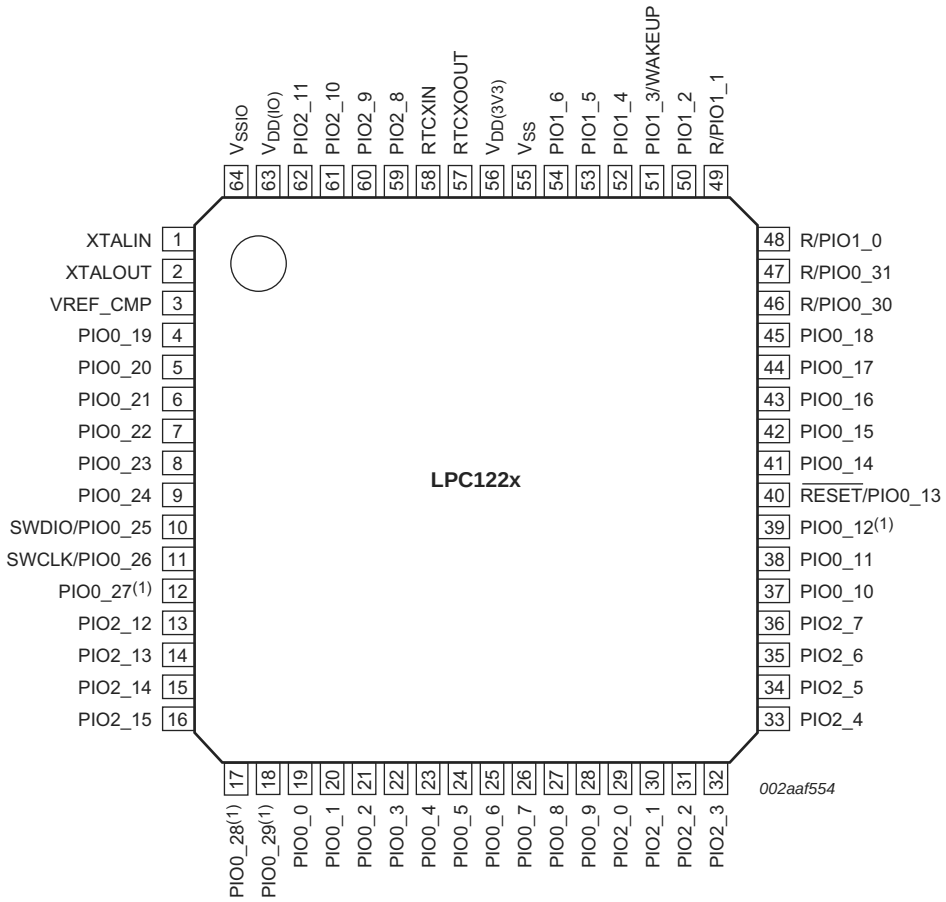



**Fig 1. LPC122x block diagram**

# 6. Pinning information

## 6.1 Pinning




(1) High-current output driver.

**Remark:** For a full listing of all functions for each pin see Table 3.

**Fig 2. Pin configuration LQFP64 package**

**Table 3. LPC122x pin description** *…continued*

| Symbol | Pin LQFP48 | Pin LQFP64 | | Start logic input | Type | Reset state [1] | Description |
|---|---|---|---|---|---|---|---|
| PIO0_7/$\overline{\text{CTS0}}$/ CT32B1_CAP1/ CT32B1_MAT1 | 22 | 26 | [2] [3] | yes | I/O | I; PU | **PIO0_7 —** General purpose digital input/output pin. |
| | | | | | I | - | **$\overline{\text{CTS0}}$ —** Clear To Send input for UART0. |
| | | | | | I | - | **CT32B1_CAP1 —** Capture input, channel 1 for 32-bit timer 1. |
| | | | | | O | - | **CT32B1_MAT1 —** Match output, channel 1 for 32-bit timer 1. |
| PIO0_8/RXD1/ CT32B1_CAP2/ CT32B1_MAT2 | 23 | 27 | [2] [3] | yes | I/O | I; PU | **PIO0_8 —** General purpose digital input/output pin. |
| | | | | | I | - | **RXD1 —** Receiver input for UART1. |
| | | | | | I | - | **CT32B1_CAP2 —** Capture input, channel 2 for 32-bit timer 1. |
| | | | | | O | - | **CT32B1_MAT2 —** Match output, channel 2 for 32-bit timer 1. |
| PIO0_9/TXD1/ CT32B1_CAP3/ CT32B1_MAT3 | 24 | 28 | [2] [3] | yes | I/O | I; PU | **PIO0_9 —** General purpose digital input/output pin. |
| | | | | | O | - | **TXD1 —** Transmitter output for UART1. |
| | | | | | I | - | **CT32B1_CAP3 —** Capture input, channel 3 for 32-bit timer 1. |
| | | | | | O | - | **CT32B1_MAT3 —** Match output, channel 3 for 32-bit timer 1. |
| PIO0_10/SCL | 25 | 37 | [4] | yes | I/O | I; IA | **PIO0_10 —** General purpose digital input/output pin. |
| | | | | | I/O | - | **SCL —** $I^2C$-bus clock input/output. |
| PIO0_11/SDA/ CT16B0_CAP0/ CT16B0_MAT0 | 26 | 38 | [4] | yes | I/O | I; IA | **PIO0_11 —** General purpose digital input/output pin. |
| | | | | | I/O | - | **SDA —** $I^2C$-bus data input/output. |
| | | | | | I | - | **CT16B0_CAP0 —** Capture input, channel 0 for 16-bit timer 0. |
| | | | | | O | - | **CT16B0_MAT0 —** Match output, channel 0 for 16-bit timer 0. |
| PIO0_12/CLKOUT/ CT16B0_CAP1/ CT16B0_MAT1 | 27 | 39 | [9] | no | I/O | I; PU | **PIO0_12 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler. High-current output driver. |
| | | | | | O | - | **CLKOUT —** Clock out pin. |
| | | | | | I | - | **CT16B0_CAP1 —** Capture input, channel 1 for 16-bit timer 0. |
| | | | | | O | - | **CT16B0_MAT1 —** Match output, channel 1 for 16-bit timer 0. |
| $\overline{\text{RESET}}$/PIO0_13 | 28 | 40 | [5] [3] | no | I | I; PU | **$\overline{\text{RESET}}$ —** External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. |
| | | | | | I/O | - | **PIO0_13 —** General purpose digital input/output pin. |
| PIO0_14/SCK | 29 | 41 | [2] [3] | no | I/O | I; PU | **PIO0_14 —** General purpose digital input/output pin. |
| | | | | | I/O | - | **SCK —** Serial clock for SSP/SPI. |
| PIO0_15/SSEL/ CT16B1_CAP0/ CT16B1_MAT0 | 30 | 42 | [2] [3] | no | I/O | I; PU | **PIO0_15 —** General purpose digital input/output pin. |
| | | | | | I/O | - | **SSEL —** Slave select for SSP/SPI. |
| | | | | | I | - | **CT16B1_CAP0 —** Capture input, channel 0 for 16-bit timer 1. |
| | | | | | O | - | **CT16B1_MAT0 —** Match output, channel 0 for 16-bit timer 1. |
| PIO0_16/MISO/ CT16B1_CAP1/ CT16B1_MAT1 | 31 | 43 | [2] [3] | no | I/O | I; PU | **PIO0_16 —** General purpose digital input/output pin. |
| | | | | | I/O | - | **MISO —** Master In Slave Out for SSP/SPI. |
| | | | | | I | - | **CT16B1_CAP1 —** Capture input, channel 1 for 16-bit timer 1. |
| | | | | | O | - | **CT16B1_MAT1 —** Match output, channel 1 for 16-bit timer 1. |

**Table 3. LPC122x pin description** *…continued*

| Symbol | Pin LQFP48 | Pin LQFP64 | | Start logic input | Type | Reset state [1] | Description |
|---|---|---|---|---|---|---|---|
| PIO0_17/MOSI | 32 | 44 | [2] [3] | no | I/O | I; PU | **PIO0_17 —** General purpose digital input/output pin. |
| | | | | | I/O | - | **MOSI —** Master Out Slave In for SSP/SPI. |
| PIO0_18/SWCLK/ CT32B0_CAP0/ CT32B0_MAT0 | 33 | 45 | [2] [3] | no | I/O | I; PU | **PIO0_18 —** General purpose digital input/output pin. |
| | | | | | I | - | **SWCLK —** Serial wire clock, alternate location. |
| | | | | | I | - | **CT32B0_CAP0 —** Capture input, channel 0 for 32-bit timer 0. |
| | | | | | O | - | **CT32B0_MAT0 —** Match output, channel 0 for 32-bit timer 0. |
| PIO0_19/ACMP0_I0/ CT32B0_CAP1/ CT32B0_MAT1 | 4 | 4 | [6] [7] | no | I/O | I; PU | **PIO0_19 —** General purpose digital input/output pin. |
| | | | | | I | - | **ACMP0_I0 —** Input 0 for comparator 0. |
| | | | | | I | - | **CT32B0_CAP1 —** Capture input, channel 1 for 32-bit timer 0. |
| | | | | | O | - | **CT32B0_MAT1 —** Match output, channel 1 for 32-bit timer 0 |
| PIO0_20/ACMP0_I1/ CT32B0_CAP2/ CT32B0_MAT2 | 5 | 5 | [6] [7] | no | I/O | I; PU | **PIO0_20 —** General purpose digital input/output pin. |
| | | | | | I | - | **ACMP0_I1 —** Input 1 for comparator 0. |
| | | | | | I | - | **CT32B0_CAP2 —** Capture input, channel 2 for 32-bit timer 0. |
| | | | | | O | - | **CT32B0_MAT2 —** Match output, channel 2 for 32-bit timer 0. |
| PIO0_21/ACMP0_I2/ CT32B0_CAP3/ CT32B0_MAT3 | 6 | 6 | [6] [7] | no | I/O | I; PU | **PIO0_21 —** General purpose digital input/output pin. |
| | | | | | I | - | **ACMP0_I2 —** Input 2 for comparator 0. |
| | | | | | I | - | **CT32B0_CAP3 —** Capture input, channel 3 for 32-bit timer 0. |
| | | | | | O | - | **CT32B0_MAT3 —** Match output, channel 3 for 32-bit timer 0. |
| PIO0_22/ACMP0_I3 | 7 | 7 | [6] [7] | no | I/O | I; PU | **PIO0_22 —** General purpose digital input/output pin. |
| | | | | | I | - | **ACMP0_I3 —** Input 3 for comparator 0. |
| PIO0_23/ ACMP1_I0/ CT32B1_CAP0/ CT32B1_MAT0 | 8 | 8 | [6] [7] | no | I/O | I; PU | **PIO0_23 —** General purpose digital input/output pin. |
| | | | | | I | - | **ACMP1_I0 —** Input 0 for comparator 1. |
| | | | | | I | - | **CT32B1_CAP0 —** Capture input, channel 0 for 32-bit timer 1. |
| | | | | | O | - | **CT32B1_MAT0 —** Match output, channel 0 for 32-bit timer 1. |
| PIO0_24/ACMP1_I1/ CT32B1_CAP1/ CT32B1_MAT1 | 9 | 9 | [6] [7] | no | I/O | I; PU | **PIO0_24 —** General purpose digital input/output pin. |
| | | | | | I | - | **ACMP1_I1 —** Input 1 for comparator 1. |
| | | | | | I | - | **CT32B1_CAP1 —** Capture input, channel 1 for 32-bit timer 1. |
| | | | | | O | - | **CT32B1_MAT1 —** Match output, channel 1 for 32-bit timer 1. |
| SWDIO/ACMP1_I2/ CT32B1_CAP2/ CT32B1_MAT2/ PIO0_25 | 10 | 10 | [6] [7] | no | I/O | I; PU | **SWDIO —** Serial wire debug input/output, default location. |
| | | | | | I | - | **ACMP1_I2 —** Input 2 for comparator 1. |
| | | | | | I | - | **CT32B1_CAP2 —** Capture input, channel 2 for 32-bit timer 1. |
| | | | | | O | - | **CT32B1_MAT2 —** Match output, channel 2 for 32-bit timer 1. |
| | | | | | I/O | - | **PIO0_25 —** General purpose digital input/output pin. |
| SWCLK/ACMP1_I3/ CT32B1_CAP3/ CT32B1_MAT3/ PIO0_26 | 11 | 11 | [6] [7] | no | I | I; PU | **SWCLK —** Serial wire clock, default location. |
| | | | | | I | - | **ACMP1_I3 —** Input 3 for comparator 1. |
| | | | | | I | - | **CT32B1_CAP3 —** Capture input, channel 3 or 32-bit timer 1. |
| | | | | | O | - | **CT32B1_MAT3 —** Match output, channel 3 for 32-bit timer 1. |
| | | | | | I/O | | **PIO0_26 —** General purpose digital input/output pin. |

**Table 3. LPC122x pin description** *…continued*

| Symbol | Pin LQFP48 | Pin LQFP64 | | Start logic input | Type | Reset state [1] | Description |
|---|---|---|---|---|---|---|---|
| PIO1_5/AD7/ CT16B1_CAP0/ CT16B1_MAT0 | 41 | 53 | [6] [3] | no | I/O | I; PU | **PIO1_5 —** General purpose digital input/output pin. |
| | | | | | I | - | **AD7 —** A/D converter, input 7. |
| | | | | | I | - | **CT16B1_CAP0 —** Capture input, channel 0 for 16-bit timer 1. |
| | | | | | O | - | **CT16B1_MAT0 —** Match output, channel 0 for 16-bit timer 1. |
| PIO1_6/ CT16B1_CAP1/ CT16B1_MAT1 | 42 | 54 | [2] [3] | no | I/O | I; PU | **PIO1_6 —** General purpose digital input/output pin. |
| | | | | | I | - | **CT16B1_CAP1 —** Capture input, channel 1 for 16-bit timer 1. |
| | | | | | O | - | **CT16B1_MAT1 —** Match output, channel 1 for 16-bit timer 1. |
| PIO2_0 to PIO2_15 | | | | | I/O | | **Port 2 —** Port 2 is a 32-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block. Pins PIO2_16 through PIO2_31 are not available. |
| PIO2_0/ CT16B0_CAP0/ CT16B0_MAT0/ $\overline{\text{RTS0}}$ | - | 29 | [2] [3] | no | I/O | I; PU | **PIO2_0 —** General purpose digital input/output pin. |
| | | | | | I | - | **CT16B0_CAP0 —** Capture input, channel 0 for 16-bit timer 0. |
| | | | | | O | - | **CT16B0_MAT0 —** Match output, channel 0 for 16-bit timer 0. |
| | | | | | O | - | **$\overline{\text{RTS0}}$ —** Request To Send output for UART0. |
| PIO2_1/ CT16B0_CAP1/ CT16B0_MAT1/RXD0 | - | 30 | [2] [3] | no | I/O | I; PU | **PIO2_1 —** General purpose digital input/output pin. |
| | | | | | I | - | **CT16B0_CAP1 —** Capture input, channel 1 for 16-bit timer 0. |
| | | | | | O | - | **CT16B0_MAT1 —** Match output, channel 1 for 16-bit timer 0. |
| | | | | | I | - | **RXD0 —** Receiver input for UART0. |
| PIO2_2/ CT16B1_CAP0/ CT16B1_MAT0/TXD0 | - | 31 | [2] [3] | no | I/O | I; PU | **PIO2_2 —** General purpose digital input/output pin. |
| | | | | | I | - | **CT16B1_CAP0 —** Capture input, channel 0 for 16-bit timer 1. |
| | | | | | O | - | **CT16B1_MAT0 —** Match output, channel 0 for 16-bit timer 1. |
| | | | | | O | - | **TXD0 —** Transmitter output for UART0. |
| PIO2_3/ CT16B1_CAP1/ CT16B1_MAT1/$\overline{\text{DTR0}}$ | - | 32 | [2] [3] | no | I/O | I; PU | **PIO2_3 —** General purpose digital input/output pin. |
| | | | | | I | - | **CT16B1_CAP1 —** Capture input, channel 1 for 16-bit timer 1. |
| | | | | | O | - | **CT16B1_MAT1 —** Match output, channel 1 for 16-bit timer 1. |
| | | | | | O | - | **$\overline{\text{DTR0}}$ —** Data Terminal Ready output for UART0. |
| PIO2_4/ CT32B0_CAP0/ CT32B0_MAT0/$\overline{\text{CTS0}}$ | - | 33 | [2] [3] | no | I/O | I; PU | **PIO2_4 —** General purpose digital input/output pin. |
| | | | | | I | - | **CT32B0_CAP0 —** Capture input, channel 0 for 32-bit timer 0. |
| | | | | | O | - | **CT32B0_MAT0 —** Match output, channel 0 for 32-bit timer 0. |
| | | | | | I | - | **$\overline{\text{CTS0}}$ —** Clear To Send input for UART0. |
| PIO2_5/ CT32B0_CAP1/ CT32B0_MAT1/$\overline{\text{RI0}}$ | - | 34 | [2] [3] | no | I/O | I; PU | **PIO2_5 —** General purpose digital input/output pin. |
| | | | | | I | - | **CT32B0_CAP1 —** Capture input, channel 1 for 32-bit timer 0. |
| | | | | | O | - | **CT32B0_MAT1 —** Match output, channel 1 for 32-bit timer 0. |
| | | | | | I | - | **$\overline{\text{RI0}}$ —** Ring Indicator input for UART0. |

**Table 4. Pin multiplexing**

| Peripheral | Function | Type | Available on ports: | | |
|---|---|---|---|---|---|
| ADC | AD0 | I | PIO0_30 | - | - |
| | AD1 | I | PIO0_31 | - | - |
| | AD2 | I | PIO1_0 | - | - |
| | AD3 | I | PIO1_1 | - | - |
| | AD4 | I | PIO1_2 | - | - |
| | AD5 | I | PIO1_3 | - | - |
| | AD6 | I | PIO1_4 | - | - |
| | AD7 | I | PIO1_5 | - | - |
| CT16B0 | CT16B0_CAP0 | I | PIO0_11 | PIO0_28 | PIO2_0 |
| | CT16B0_CAP1 | I | PIO0_12 | PIO0_29 | PIO2_1 |
| | CT16B0_MAT0 | O | PIO0_11 | PIO0_28 | PIO2_0 |
| | CT16B0_MAT1 | O | PIO0_12 | PIO0_29 | PIO2_1 |
| CT16B1 | CT16B1_CAP0 | I | PIO0_15 | PIO1_5 | PIO2_2 |
| | CT16B1_CAP1 | I | PIO0_16 | PIO1_6 | PIO2_3 |
| | CT16B1_MAT0 | O | PIO0_15 | PIO1_5 | PIO2_2 |
| | CT16B1_MAT1 | O | PIO0_16 | PIO1_6 | PIO2_3 |
| CT32B0 | CT32B0_CAP0 | I | PIO0_1 | PIO0_18 | PIO2_4 |
| | CT32B0_CAP1 | I | PIO0_2 | PIO0_19 | PIO2_5 |
| | CT32B0_CAP2 | I | PIO0_3 | PIO0_20 | PIO2_6 |
| | CT32B0_CAP3 | I | PIO0_4 | PIO0_21 | PIO2_7 |
| | CT32B0_MAT0 | O | PIO0_1 | PIO0_18 | PIO2_4 |
| | CT32B0_MAT1 | O | PIO0_2 | PIO0_19 | PIO2_5 |
| | CT32B0_MAT2 | O | PIO0_3 | PIO0_20 | PIO2_6 |
| | CT32B0_MAT3 | O | PIO0_4 | PIO0_21 | PIO2_7 |
| CT32B1 | CT32B1_CAP0 | I | PIO0_6 | PIO0_23 | PIO2_8 |
| | CT32B1_CAP1 | I | PIO0_7 | PIO0_24 | PIO2_9 |
| | CT32B1_CAP2 | I | PIO0_8 | PIO0_25 | PIO2_10 |
| | CT32B1_CAP3 | I | PIO0_9 | PIO0_26 | PIO2_11 |
| | CT32B1_MAT0 | O | PIO0_6 | PIO0_23 | PIO2_8 |
| | CT32B1_MAT1 | O | PIO0_7 | PIO0_24 | PIO2_9 |
| | CT32B1_MAT2 | O | PIO0_8 | PIO0_25 | PIO2_10 |
| | CT32B1_MAT3 | O | PIO0_9 | PIO0_26 | PIO2_11 |
| UART0 | RXD0 | I | PIO0_1 | PIO2_1 | - |
| | TXD0 | O | PIO0_2 | PIO2_2 | - |
| | $\overline{\text{CTS0}}$ | I | PIO0_7 | PIO2_4 | - |
| | $\overline{\text{DCD0}}$ | I | PIO0_5 | PIO2_6 | - |
| | $\overline{\text{DSR0}}$ | I | PIO0_4 | PIO2_7 | - |
| | $\overline{\text{DTR0}}$ | O | PIO0_3 | PIO2_3 | - |
| | $\overline{\text{RI0}}$ | I | PIO0_6 | PIO2_5 | - |
| | $\overline{\text{RTS0}}$ | O | PIO0_0 | PIO2_0 | - |

**Table 4. Pin multiplexing**

| Peripheral | Function | Type | Available on ports: | | |
|---|---|---|---|---|---|
| UART1 | RXD1 | I | PIO0_8 | PIO2_11 | PIO2_12 |
| | TXD1 | O | PIO0_9 | PIO2_10 | PIO2_13 |
| SSP/SPI | SCK | I/O | PIO0_14 | - | - |
| | MISO | I/O | PIO0_16 | - | - |
| | MOSI | I/O | PIO0_17 | - | - |
| | SSEL | I/O | PIO0_15 | - | - |
| I2C | SCL | I/O | PIO0_10 | - | - |
| | SDA | I/O | PIO0_11 | - | - |
| SWD | SWCLK[1] | I | PIO0_18 | PIO0_26 | - |
| | SWDIO[1] | I/O | PIO0_25 | PIO1_2 | - |
| Reset | $\overline{\text{RESET}}$ | I | PIO0_13 | - | - |
| Clockout pin | CLKOUT | O | PIO0_12 | - | - |

[1] After reset, the SWD functions are selected by default on pins PIO0_26 and PIO0_25.

# 7. Functional description

## 7.1 ARM Cortex-M0 processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption.

### 7.1.1 System tick timer

The ARM Cortex-M0 includes a System Tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval.

## 7.2 On-chip flash program memory

The LPC122x contain up to 128 kB of on-chip flash memory.

## 7.3 On-chip SRAM

The LPC122x contain a total of up to 8 kB on-chip static RAM memory.

## 7.4 Memory map

The LPC122x incorporates several distinct memory regions, shown in the following figures. Figure 4 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 megabyte in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kilobytes of space. This allows simplifying the address decoding for each peripheral.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

#### 7.18.5.2 Deep-sleep mode

In Deep-sleep mode, the chip is in Sleep mode, and in addition all analog blocks are shut down. As an exception, the user has the option to keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection. Deep-sleep mode allows for additional power savings.

The GPIO pins PIO0_0 to PIO0_11 (up to 12 pins total) and the RTC match interrupt can serve as a wake-up input to the start logic to wake up the chip from Deep-sleep mode.

Unless the watchdog oscillator is selected to run in Deep-sleep mode, the clock source should be switched to IRC before entering Deep-sleep mode, because the IRC can be switched on and off glitch-free.

#### 7.18.5.3 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip with the exception of the Real Time Clock, the four general-purpose registers, and the WAKEUP pin. The LPC122x can wake up from Deep power-down mode via the WAKEUP pin or the RTC match interrupt.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. The $\overline{\text{RESET}}$ pin must also be held HIGH to prevent it from floating while in Deep power-down mode.

## 7.19 System control

### 7.19.1 Start logic

The start logic connects external pins to corresponding interrupts in the NVIC. Each pin shown in Table 3 as input to the start logic has an individual interrupt in the NVIC interrupt vector table. The start logic pins can serve as external interrupt pins when the chip is running. In addition, an input signal on the start logic pins can wake up the chip from Deep-sleep mode when all clocks are shut down.

The start logic must be configured in the system configuration block and in the NVIC before being used.

### 7.19.2 Reset

Reset has four sources on the LPC122x: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

An external pull-up resistor is required on the $\overline{\text{RESET}}$ pin if Deep power-down mode is used.

### 7.19.3 Brownout detection

The LPC122x includes four levels for monitoring the voltage on the $V_{DD(3V3)}$ pin. If this voltage falls below one of the four selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register. An additional threshold level can be selected to cause a forced reset of the chip.

### 7.19.4 Code security (Code Read Protection - CRP)

This feature of the LPC122x allows user to enable different levels of security in the system so that access to the on-chip flash and use of the SWD and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of Code Read Protection:

1. CRP1 disables access to chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_12 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

**CAUTION**

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_12 for valid user code can be disabled.

### 7.19.5 APB interface

The APB peripherals are located on one APB bus.

### 7.19.6 AHB-Lite

The AHB-Lite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the Boot ROM.

### 7.19.7 External interrupt inputs

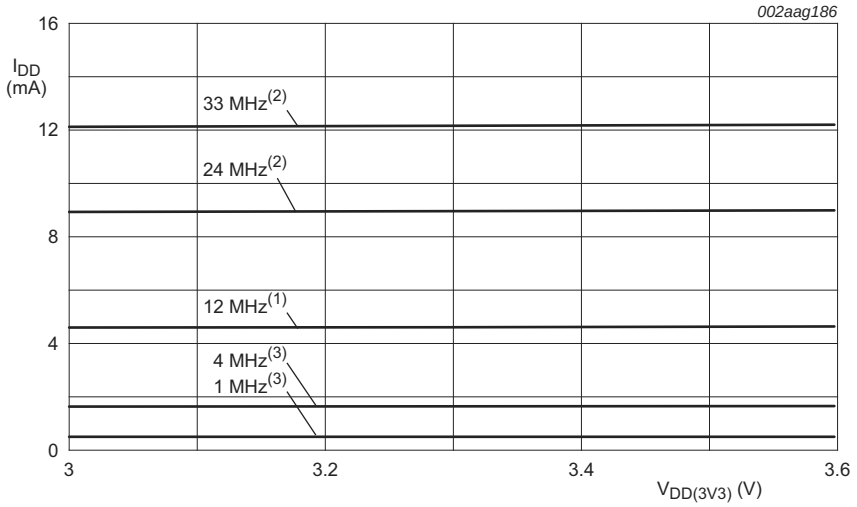
All GPIO pins can be level or edge sensitive interrupt inputs.

## 7.20 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug is supported.

## 7.21 Integer division routines

The LPC122x contain performance-optimized integer division routines with support for up to 32-bit width in the numerator and denominator. Routines for signed and unsigned division and division with remainder are available. The integer division routines are ROM-based to reduce code-size.



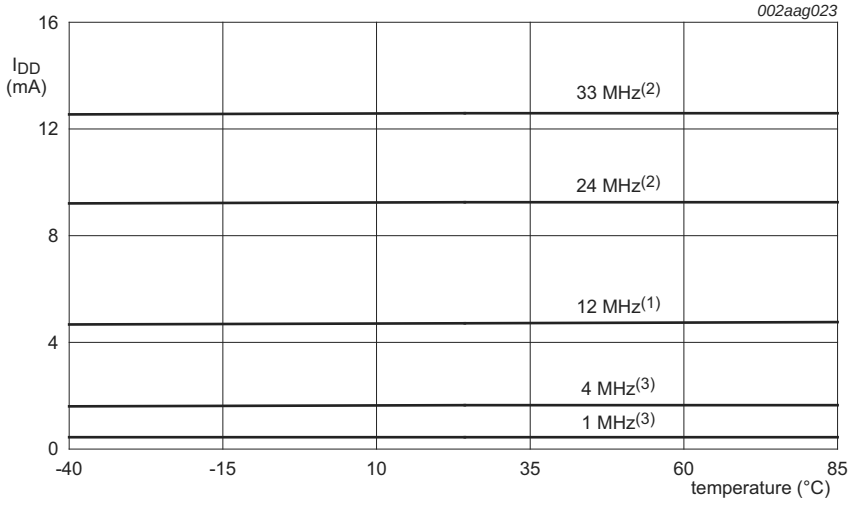

Conditions: $T_{amb}$ = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

(3) System oscillator enabled; IRC and system PLL disabled.

**Fig 6. Active mode: Typical supply current $I_{DD}$ versus supply voltage $V_{DD(3V3)}$ for different system clock frequencies (all peripherals disabled)**



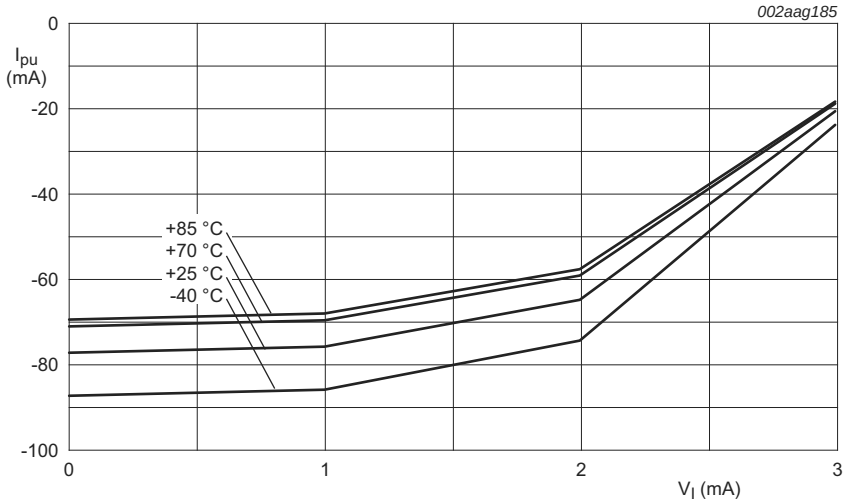

Conditions: $V_{DD(3V3)}$ = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

(3) System oscillator enabled; IRC and system PLL disabled.

**Fig 7. Active mode: Typical supply current $I_{DD}$ versus temperature for different system clock frequencies (peripherals disabled)**




Conditions: $V_{DD(IO)}$ = 3.3 V.

**Fig 18. Typical pull-up current $I_{pu}$ versus input voltage $V_I$**

# 11. Dynamic characteristics

## 11.1 Power-up ramp conditions

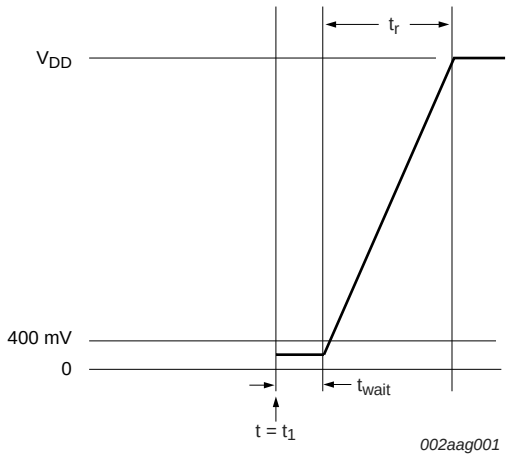
**Table 11. Power-up characteristics**

*$T_{amb}$ = –40 °C to +85 °C.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_r$ | rise time | at t = $t_1$: 0 < $V_I \leq$ 400 mV | [1] | 0 | - | 500 | ms |
| $t_{wait}$ | wait time | | [1][2] | 12 | - | - | µs |
| $V_I$ | input voltage | at t = $t_1$ on pin $V_{DD}$ | | 0 | - | 400 | mV |

[1] See Figure 20.

[2] The wait time specifies the time the power supply must be at levels below 400 mV before ramping up.




Condition: 0 < $V_I \leq$ 400 mV at start of power-up (t = $t_1$)

**Fig 20. Power-up ramp**

## 11.2 Flash memory

**Table 12. Dynamic characteristic: flash memory**
*$T_{amb}$ = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{er}$ | erase time | for one page (512 byte) | [1] | - | 20 | ms |
| | | for one sector (4 kB) | [1] | | 162 | ms |
| | | for all sectors; mass erase | [1] | - | 20 | ms |
| $t_{prog}$ | programming time | one word (4 bytes) | [1] | - | 49 | µs |
| | | four sequential words | [1] | - | 194 | µs |
| | | 128 bytes (one row of 32 words) | [1] | - | 765 | µs |
| $N_{endu}$ | endurance | | [2] | 20000 | - | cycles |
| $t_{ret}$ | retention time | | | 10 | - | years |

[1] Erase and programming times are valid over the lifetime of the device (minimum 20000 cycles).

[2] Number of program/erase cycles.

## 11.3 External clock

**Table 13. Dynamic characteristic: external clock**
*$T_{amb}$ = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.*[1]

| Symbol | Parameter | Conditions | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{osc}$ | oscillator frequency | | 1 | - | 25 | MHz |
| $T_{cy(clk)}$ | clock cycle time | | 40 | - | 1000 | ns |
| $t_{CHCX}$ | clock HIGH time | | $T_{cy(clk)} \times 0.4$ | - | - | ns |
| $t_{CLCX}$ | clock LOW time | | $T_{cy(clk)} \times 0.4$ | - | - | ns |
| $t_{CLCH}$ | clock rise time | | - | - | 5 | ns |
| $t_{CHCL}$ | clock fall time | | - | - | 5 | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

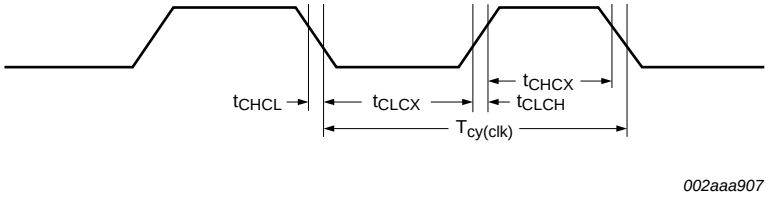



**Fig 21. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)**

## 11.4 Internal oscillators

**Table 14. Dynamic characteristic: internal oscillators**
*$T_{amb}$ = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.*[1]

| Symbol | Parameter | Conditions | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{osc(RC)}$ | internal RC oscillator frequency | - | 11.88 | 12 | 12.12 | MHz |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

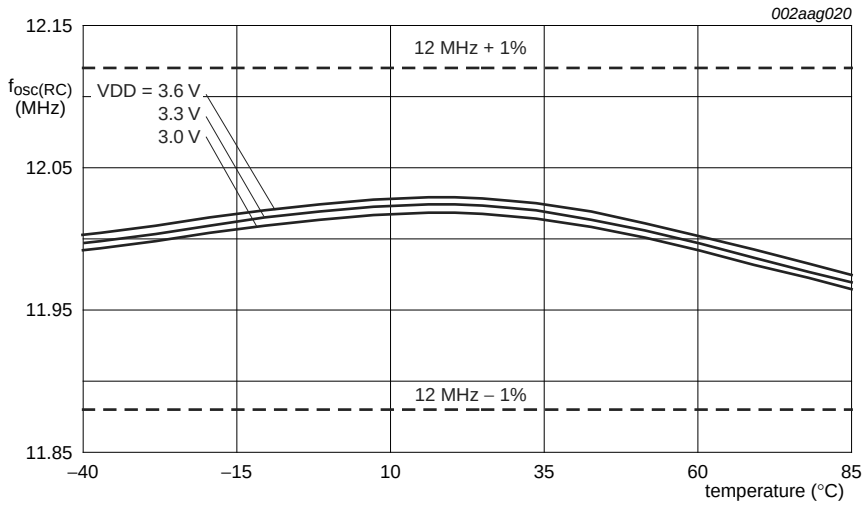



**Fig 22. Internal RC oscillator frequency versus temperature**

**Table 15. Dynamic characteristics: Watchdog oscillator**

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{osc(int)}$ | internal oscillator frequency | DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register; | [2][3] | - | 7.8 | - | kHz |
| | | DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register | [2][3] | - | 1700 | - | kHz |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature ($T_{amb}$ = −40 °C to +85 °C) is ±40 %.

[3] See the *LPC122x user manual*.

## 11.5 I²C-bus

**Table 16. Dynamic characteristic: I²C-bus pins**
*$T_{amb}$ = −40 °C to +85 °C.*[1]

| Symbol | Parameter | | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | | Standard-mode | 0 | 100 | kHz |
| | | | Fast-mode | 0 | 400 | kHz |
| | | | Fast-mode Plus | 0 | 1 | MHz |
| $t_f$ | fall time | [3][4][5][6] | of both SDA and SCL signals | - | 300 | ns |
| | | | Standard-mode | | | |
| | | | Fast-mode | $20 + 0.1 \times C_b$ | 300 | ns |
| | | | Fast-mode Plus | - | 120 | ns |
| $t_{LOW}$ | LOW period of the SCL clock | | Standard-mode | 4.7 | - | µs |
| | | | Fast-mode | 1.3 | - | µs |
| | | | Fast-mode Plus | 0.5 | - | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | | Standard-mode | 4.0 | - | µs |
| | | | Fast-mode | 0.6 | - | µs |
| | | | Fast-mode Plus | 0.26 | - | µs |
| $t_{HD;DAT}$ | data hold time | [2][3][7] | Standard-mode | 0 | - | µs |
| | | | Fast-mode | 0 | - | µs |
| | | | Fast-mode Plus | 0 | - | µs |
| $t_{SU;DAT}$ | data set-up time | [8][9] | Standard-mode | 250 | - | ns |
| | | | Fast-mode | 100 | - | ns |
| | | | Fast-mode Plus | 50 | - | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH}$(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[4] $C_b$ = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.

[5] The maximum $t_f$ for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage $t_f$ is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified $t_f$.

[6] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[7] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period ($t_{LOW}$) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[8] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[9] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

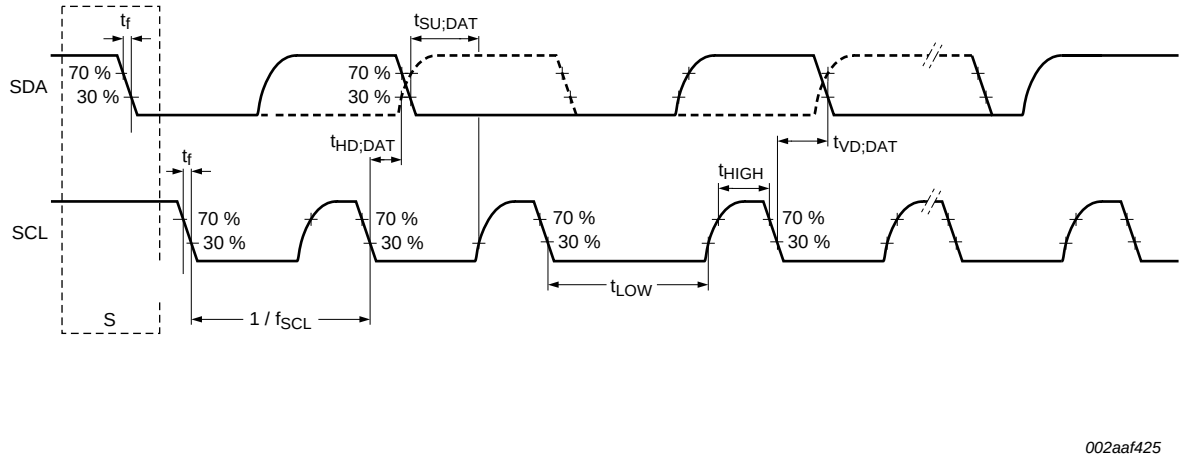
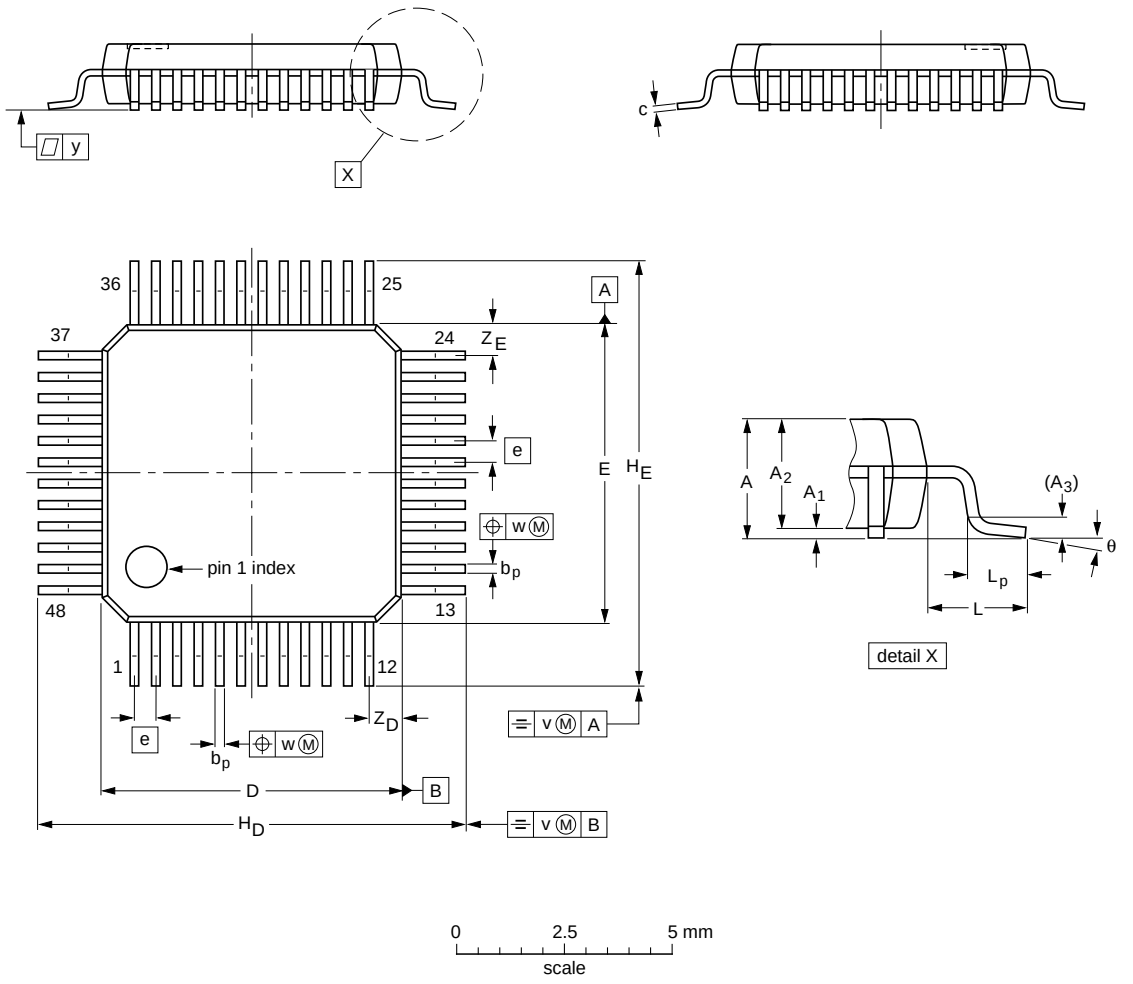



**Fig 23. $I^2C$-bus pins clock timing**

**LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm** **SOT313-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.6 | 0.20<br>0.05 | 1.45<br>1.35 | 0.25 | 0.27<br>0.17 | 0.18<br>0.12 | 7.1<br>6.9 | 7.1<br>6.9 | 0.5 | 9.15<br>8.85 | 9.15<br>8.85 | 1 | 0.75<br>0.45 | 0.2 | 0.12 | 0.1 | 0.95<br>0.55 | 0.95<br>0.55 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT313-2 | 136E05 | MS-026 | | | | ~~00-01-19~~<br>03-02-25 |

**Fig 26. Package outline SOT313-2 (LQFP48)**

# 15. Abbreviations

**Table 18. Abbreviations**

| Acronym | Description |
|---|---|
| ADC | Analog-to-Digital-Converter |
| AHB | Advanced High-performance Bus |
| APB | Advanced Peripheral Bus |
| BOD | BrownOut Detection |
| CCITT | Comité Consultatif International Téléphonique et Télégraphique |
| CRC | Cyclic Redundancy Check |
| DMA | Direct Memory Access |
| FIFO | First-In-First-Out |
| GPIO | General Purpose Input/Output |
| I/O | Input/Output |
| IrDA | Infrared Data Association |
| IRC | Internal Resistor-Capacitor |
| JEDEC | Joint Electron Devices Engineering Council |
| PLL | Phase-Locked Loop |
| SPI | Serial Peripheral Interface |
| SSI | Serial Synchronous Interface |
| SSP | Synchronous Serial Port |
| UART | Universal Asynchronous Receiver/Transmitter |

# 19. Contents



**continued >>**