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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	45MHz
Connectivity	I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	55
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1225fbd64-301-1

5. Block diagram

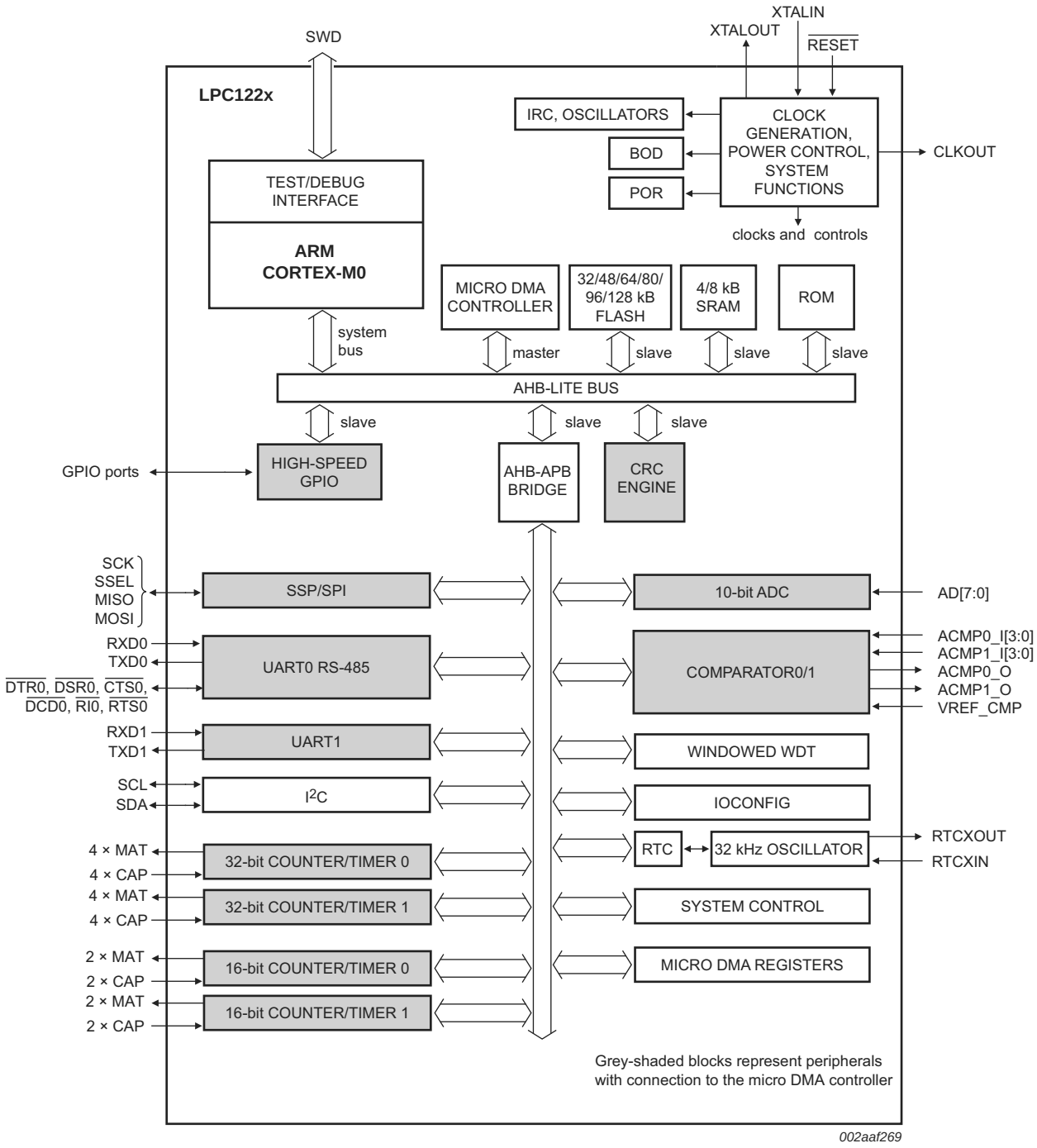
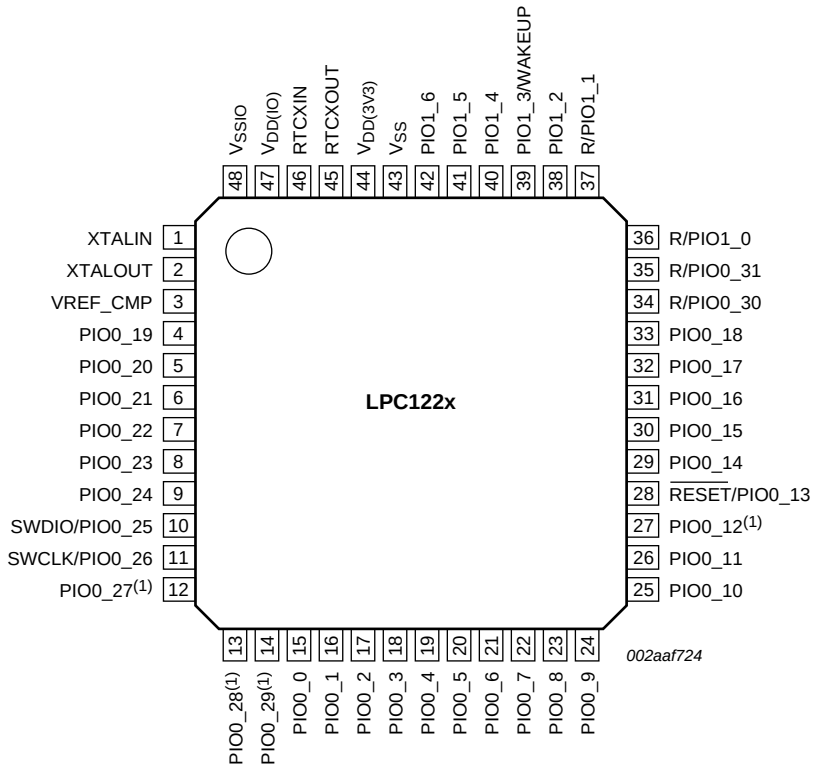


Fig 1. LPC122x block diagram



(1) High-current output driver.

Remark: For a full listing of all functions for each pin see Table 3.

Fig 3. Pin configuration LQFP48 package

6.2 Pin description

All pins except the supply pins can have more than one function as shown in Table 3. The pin function is selected through the pin's IOCON register in the IOCONFIG block. The multiplexed functions (see Table 4) include the counter/timer inputs and outputs, the UART receive, transmit, and control functions, and the serial wire debug functions.

For each pin, the default function is listed first together with the pin's reset state.

Table 3. LPC122x pin description

Symbol	Pin LQFP48	Pin LQFP64		Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_31					I/O		**Port 0 —** Port 0 is a 32-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
PIO0_0/$\overline{\text{RTS0}}$	15	19	[2] [3]	yes	I/O	I; PU	**PIO0_0 —** General purpose digital input/output pin.
					O	-	**$\overline{\text{RTS0}}$ —** Request To Send output for UART0.
PIO0_1/RXD0/ CT32B0_CAP0/ CT32B0_MAT0	16	20	[2] [3]	yes	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin.
					I	-	**RXD0 —** Receiver input for UART0.
					I	-	**CT32B0_CAP0 —** Capture input, channel 0 for 32-bit timer 0.
					O	-	**CT32B0_MAT0 —** Match output, channel 0 for 32-bit timer 0.
PIO0_2/TXD0/ CT32B0_CAP1/ CT32B0_MAT1	17	21	[2] [3]	yes	I/O	I; PU	**PIO0_2 —** General purpose digital input/output pin.
					O	-	**TXD0 —** Transmitter output for UART0.
					I	-	**CT32B0_CAP1 —** Capture input, channel 1 for 32-bit timer 0.
					O	-	**CT32B0_MAT1 —** Match output, channel 1 for 32-bit timer 0.
PIO0_3/$\overline{\text{DTR0}}$/ CT32B0_CAP2/ CT32B0_MAT2	18	22	[2] [3]	yes	I/O	I; PU	**PIO0_3 —** General purpose digital input/output pin.
					O	-	**$\overline{\text{DTR0}}$ —** Data Terminal Ready output for UART0.
					I	-	**CT32B0_CAP2 —** Capture input, channel 2 for 32-bit timer 0.
					O	-	**CT32B0_MAT2 —** Match output, channel 2 for 32-bit timer 0.
PIO0_4/$\overline{\text{DSR0}}$/ CT32B0_CAP3/ CT32B0_MAT3	19	23	[2] [3]	yes	I/O	I; PU	**PIO0_4 —** General purpose digital input/output pin.
					I	-	**$\overline{\text{DSR0}}$ —** Data Set Ready input for UART0.
					I	-	**CT32B0_CAP3 —** Capture input, channel 3 for 32-bit timer 0.
					O	-	**CT32B0_MAT3 —** Match output, channel 3 for 32-bit timer 0.
PIO0_5/$\overline{\text{DCD0}}$	20	24	[2] [3]	yes	I/O	I; PU	**PIO0_5 —** General purpose digital input/output pin.
					I	-	**$\overline{\text{DCD0}}$ —** Data Carrier Detect input for UART0.
PIO0_6/$\overline{\text{RI0}}$/ CT32B1_CAP0/ CT32B1_MAT0	21	25	[2] [3]	yes	I/O	I; PU	**PIO0_6 —** General purpose digital input/output pin.
					I	-	**$\overline{\text{RI0}}$ —** Ring Indicator input for UART0.
					I	-	**CT32B1_CAP0 —** Capture input, channel 0 for 32-bit timer 1.
					O	-	**CT32B1_MAT0 —** Match output, channel 0 for 32-bit timer 1.

Table 3. LPC122x pin description *…continued*

Symbol	Pin LQFP48	Pin LQFP64		Start logic input	Type	Reset state [1]	Description
PIO1_5/AD7/ CT16B1_CAP0/ CT16B1_MAT0	41	53	[6] [3]	no	I/O	I; PU	**PIO1_5 —** General purpose digital input/output pin.
					I	-	**AD7 —** A/D converter, input 7.
					I	-	**CT16B1_CAP0 —** Capture input, channel 0 for 16-bit timer 1.
					O	-	**CT16B1_MAT0 —** Match output, channel 0 for 16-bit timer 1.
PIO1_6/ CT16B1_CAP1/ CT16B1_MAT1	42	54	[2] [3]	no	I/O	I; PU	**PIO1_6 —** General purpose digital input/output pin.
					I	-	**CT16B1_CAP1 —** Capture input, channel 1 for 16-bit timer 1.
					O	-	**CT16B1_MAT1 —** Match output, channel 1 for 16-bit timer 1.
PIO2_0 to PIO2_15					I/O		**Port 2 —** Port 2 is a 32-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block. Pins PIO2_16 through PIO2_31 are not available.
PIO2_0/ CT16B0_CAP0/ CT16B0_MAT0/ $\overline{\text{RTS0}}$	-	29	[2] [3]	no	I/O	I; PU	**PIO2_0 —** General purpose digital input/output pin.
					I	-	**CT16B0_CAP0 —** Capture input, channel 0 for 16-bit timer 0.
					O	-	**CT16B0_MAT0 —** Match output, channel 0 for 16-bit timer 0.
					O	-	**$\overline{\text{RTS0}}$ —** Request To Send output for UART0.
PIO2_1/ CT16B0_CAP1/ CT16B0_MAT1/RXD0	-	30	[2] [3]	no	I/O	I; PU	**PIO2_1 —** General purpose digital input/output pin.
					I	-	**CT16B0_CAP1 —** Capture input, channel 1 for 16-bit timer 0.
					O	-	**CT16B0_MAT1 —** Match output, channel 1 for 16-bit timer 0.
					I	-	**RXD0 —** Receiver input for UART0.
PIO2_2/ CT16B1_CAP0/ CT16B1_MAT0/TXD0	-	31	[2] [3]	no	I/O	I; PU	**PIO2_2 —** General purpose digital input/output pin.
					I	-	**CT16B1_CAP0 —** Capture input, channel 0 for 16-bit timer 1.
					O	-	**CT16B1_MAT0 —** Match output, channel 0 for 16-bit timer 1.
					O	-	**TXD0 —** Transmitter output for UART0.
PIO2_3/ CT16B1_CAP1/ CT16B1_MAT1/$\overline{\text{DTR0}}$	-	32	[2] [3]	no	I/O	I; PU	**PIO2_3 —** General purpose digital input/output pin.
					I	-	**CT16B1_CAP1 —** Capture input, channel 1 for 16-bit timer 1.
					O	-	**CT16B1_MAT1 —** Match output, channel 1 for 16-bit timer 1.
					O	-	**$\overline{\text{DTR0}}$ —** Data Terminal Ready output for UART0.
PIO2_4/ CT32B0_CAP0/ CT32B0_MAT0/$\overline{\text{CTS0}}$	-	33	[2] [3]	no	I/O	I; PU	**PIO2_4 —** General purpose digital input/output pin.
					I	-	**CT32B0_CAP0 —** Capture input, channel 0 for 32-bit timer 0.
					O	-	**CT32B0_MAT0 —** Match output, channel 0 for 32-bit timer 0.
					I	-	**$\overline{\text{CTS0}}$ —** Clear To Send input for UART0.
PIO2_5/ CT32B0_CAP1/ CT32B0_MAT1/$\overline{\text{RI0}}$	-	34	[2] [3]	no	I/O	I; PU	**PIO2_5 —** General purpose digital input/output pin.
					I	-	**CT32B0_CAP1 —** Capture input, channel 1 for 32-bit timer 0.
					O	-	**CT32B0_MAT1 —** Match output, channel 1 for 32-bit timer 0.
					I	-	**$\overline{\text{RI0}}$ —** Ring Indicator input for UART0.

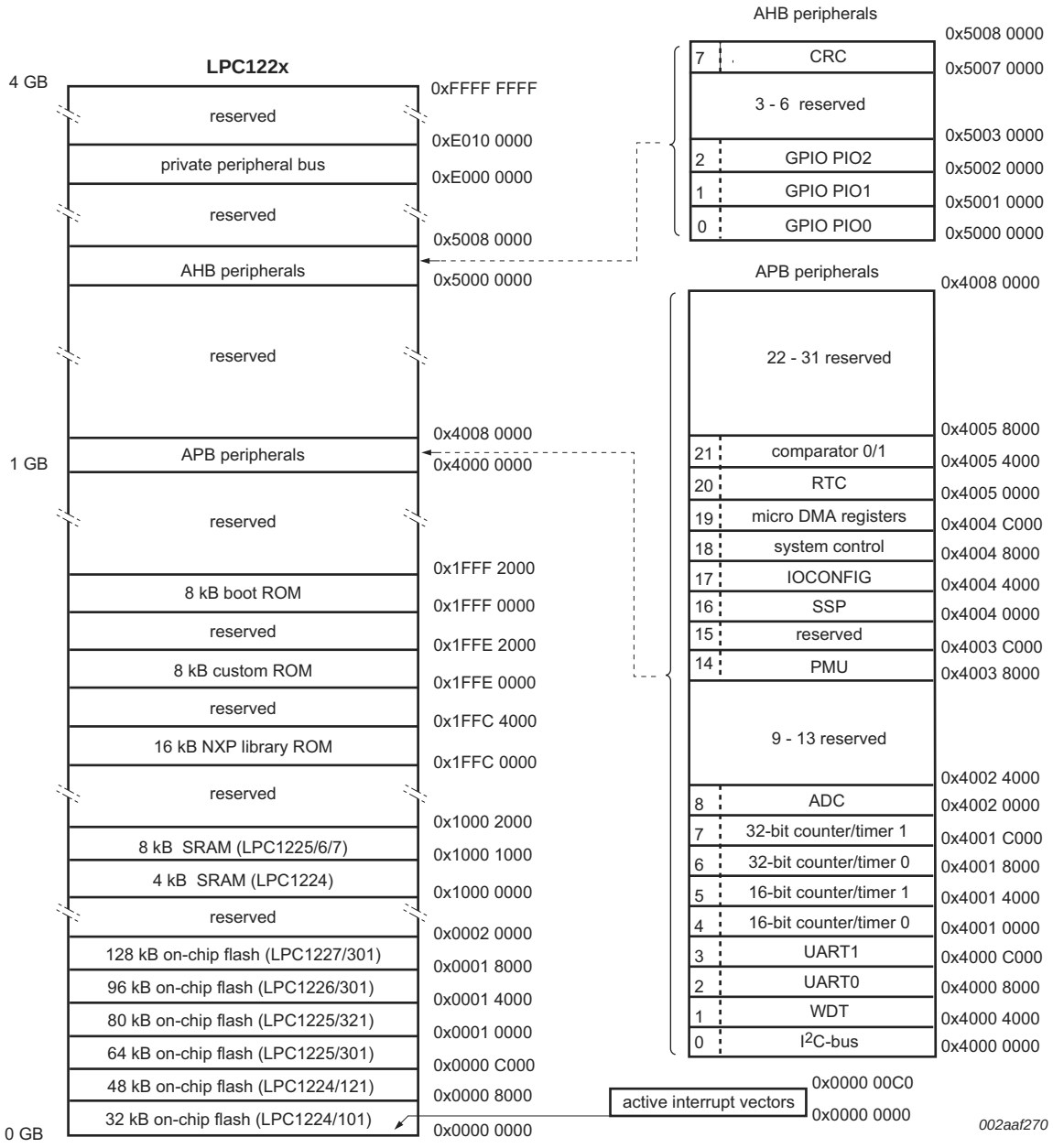


Fig 4. LPC122x memory map

7.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.

- In the LPC122x, the NVIC supports 32 vectored interrupts. In addition, up to 12 of the individual GPIO inputs are NVIC-vector capable.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation.
- Non-maskable Interrupt (NMI) can be programmed to use any of the peripheral interrupts. The NMI is not available on an external pin.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any GPIO pin (total of up to 55 pins) regardless of the selected function, can be programmed to generate an interrupt on a level, a rising edge or falling edge, or both.

7.6 IOCONFIG block

The IOCONFIG block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.6.1 Features

- Programmable pull-up resistor.
- Programmable digital glitch filter.
- Programmable input inverter.
- Programmable drive current.
- Programmable open-drain mode.

7.7 Micro DMA controller

The micro DMA controller enables memory-to-memory, memory-to-peripheral, and peripheral-to-memory data transfers. The supported peripherals are: UART0 (transmit and receive), UART1 (transmit and receive), SSP/SPI (transmit and receive), ADC, RTC, 32-bit counter/timer 0 (match output channels 0 and 1), 32-bit counter/timer 1 (match output channels 0 and 1), 16-bit counter/timer 0 (match output channel 0), 16-bit counter/timer 1 (match output channel 0), comparator 0, comparator 1, GPIO0 to GPIO2.

7.7.1 Features

- Single AHB-Lite master for transferring data using a 32-bit address bus and 32-bit data bus.
- 21 DMA channels.
- Handshake signals and priority level programmable for each channel.
- Each priority level arbitrates using a fixed priority that is determined by the DMA channel number.

7.10.1 Features

- 16-byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto-baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode (UART0).
- Support for modem control (UART0).

7.11 SSP/SPI serial I/O controller

The LPC122x contain one SSP/SPI controller. The SSP/SPI controller is capable of operation on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.11.1 Features

- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.12 I^2C-bus serial I/O controller

The LPC122x contain one I^2C-bus controller.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.12.1 Features

- The I^2C-interface is a standard I^2C-compliant bus interface with open-drain pins and supports I^2C Fast-mode Plus with bit rates of up to 1 Mbit/s.
- Programmable digital glitch filter providing a 60 ns to 1 μs input filter.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.

- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the Internal RC oscillator (IRC) or the Watchdog oscillator. This gives a wide range of potential timing choices of Watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring for increased reliability.

7.17 Real-time clock (RTC)

The RTC provides a basic alarm function or can be used as a long time base counter. The RTC generates an interrupt after counting for a programmed number of cycles of the RTC clock input.

7.17.1 Features

- Uses dedicated 32 kHz ultra low-power oscillator.
- Selectable clock inputs: RTC oscillator (1 Hz, delayed 1 Hz, or 1 kHz clock) or main clock with programmable clock divider.
- 32-bit counter.
- Programmable 32-bit match/compare register.
- Software maskable interrupt when counter and compare registers are identical.
- Generates wake-up from Deep-sleep and Deep power-down modes.

7.18 Clocking and power control

7.18.1 Crystal oscillators

The LPC122x include four independent oscillators. These are the system oscillator, the Internal RC oscillator (IRC), the RTC 32 kHz oscillator (for the RTC only), and the Watchdog oscillator. Except for the RTC oscillator, each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC122x will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 5 for an overview of the LPC122x clock generation.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL. The ARM processor clock frequency is referred to as CCLK elsewhere in this document.

7.18.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 7.8 kHz and 1.7 MHz. The frequency spread over processing and temperature is ±40 %.

7.18.2 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.18.3 Clock output

The LPC122x features a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.18.4 Wake-up process

The LPC122x begin operation at power-up and when awakened from Deep power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

7.18.5 Power control

The LPC122x support a variety of power control features. There are three special modes of processor power reduction: Sleep mode, Deep-sleep mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.18.5.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

An external pull-up resistor is required on the $\overline{\text{RESET}}$ pin if Deep power-down mode is used.

7.19.3 Brownout detection

The LPC122x includes four levels for monitoring the voltage on the $V_{DD(3V3)}$ pin. If this voltage falls below one of the four selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register. An additional threshold level can be selected to cause a forced reset of the chip.

7.19.4 Code security (Code Read Protection - CRP)

This feature of the LPC122x allows user to enable different levels of security in the system so that access to the on-chip flash and use of the SWD and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of Code Read Protection:

1. CRP1 disables access to chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_12 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_12 for valid user code can be disabled.

7.19.5 APB interface

The APB peripherals are located on one APB bus.

7.19.6 AHB-Lite

The AHB-Lite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the Boot ROM.

7.19.7 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs.

7.20 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug is supported.

7.21 Integer division routines

The LPC122x contain performance-optimized integer division routines with support for up to 32-bit width in the numerator and denominator. Routines for signed and unsigned division and division with remainder are available. The integer division routines are ROM-based to reduce code-size.

10.5 BOD static characteristics

Table 10. BOD static characteristics[1]
T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1				
		assertion	-	2.25	-	V
		de-assertion	-	2.39	-	V
		interrupt level 2				
		assertion	-	2.54	-	V
		de-assertion	-	2.67	-	V
		interrupt level 3				
		assertion	-	2.83	-	V
		de-assertion	-	2.93	-	V
		reset level 1				
		assertion	-	2.04	-	V
		de-assertion	-	2.18	-	V
		reset level 2				
		assertion	-	2.34	-	V
		de-assertion	-	2.47	-	V
		reset level 3				
		assertion	-	2.62	-	V
		de-assertion	-	2.76	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC122x user manual*.

11. Dynamic characteristics

11.1 Power-up ramp conditions

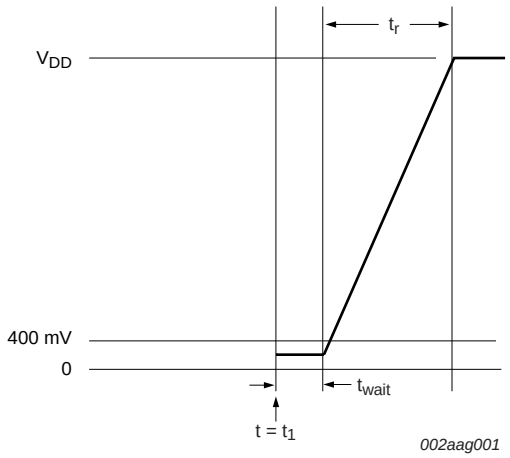
Table 11. Power-up characteristics

T_{amb} = –40 °C to +85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	at t = t_1: 0 < $V_I \leq$ 400 mV	[1]	0	-	500	ms
t_{wait}	wait time		[1][2]	12	-	-	µs
V_I	input voltage	at t = t_1 on pin V_{DD}		0	-	400	mV

[1] See Figure 20.

[2] The wait time specifies the time the power supply must be at levels below 400 mV before ramping up.



Condition: 0 < $V_I \leq$ 400 mV at start of power-up (t = t_1)

Fig 20. Power-up ramp

11.2 Flash memory

Table 12. Dynamic characteristic: flash memory
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.

Symbol	Parameter	Conditions		Min	Max	Unit
t_{er}	erase time	for one page (512 byte)	[1]	-	20	ms
		for one sector (4 kB)	[1]		162	ms
		for all sectors; mass erase	[1]	-	20	ms
t_{prog}	programming time	one word (4 bytes)	[1]	-	49	µs
		four sequential words	[1]	-	194	µs
		128 bytes (one row of 32 words)	[1]	-	765	µs
N_{endu}	endurance		[2]	20000	-	cycles
t_{ret}	retention time			10	-	years

[1] Erase and programming times are valid over the lifetime of the device (minimum 20000 cycles).

[2] Number of program/erase cycles.

11.3 External clock

Table 13. Dynamic characteristic: external clock
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

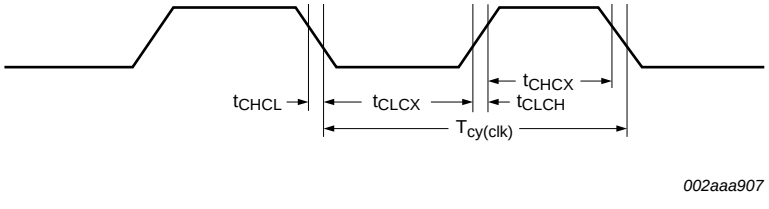


Fig 21. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

11.4 Internal oscillators

Table 14. Dynamic characteristic: internal oscillators
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12	12.12	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

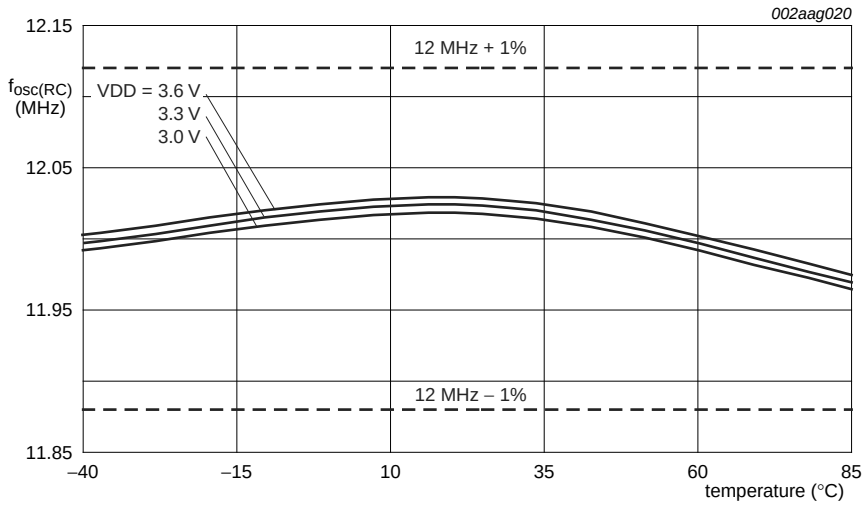


Fig 22. Internal RC oscillator frequency versus temperature

Table 15. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	7.8	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	1700	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +85 °C) is ±40 %.

[3] See the *LPC122x user manual*.

11.5 I²C-bus

Table 16. Dynamic characteristic: I²C-bus pins
T_{amb} = −40 °C to +85 °C.[1]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[3][4][5][6]	of both SDA and SCL signals	-	300	ns
			Standard-mode			
			Fast-mode	$20 + 0.1 \times C_b$	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[2][3][7]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[8][9]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[4] C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.

[5] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

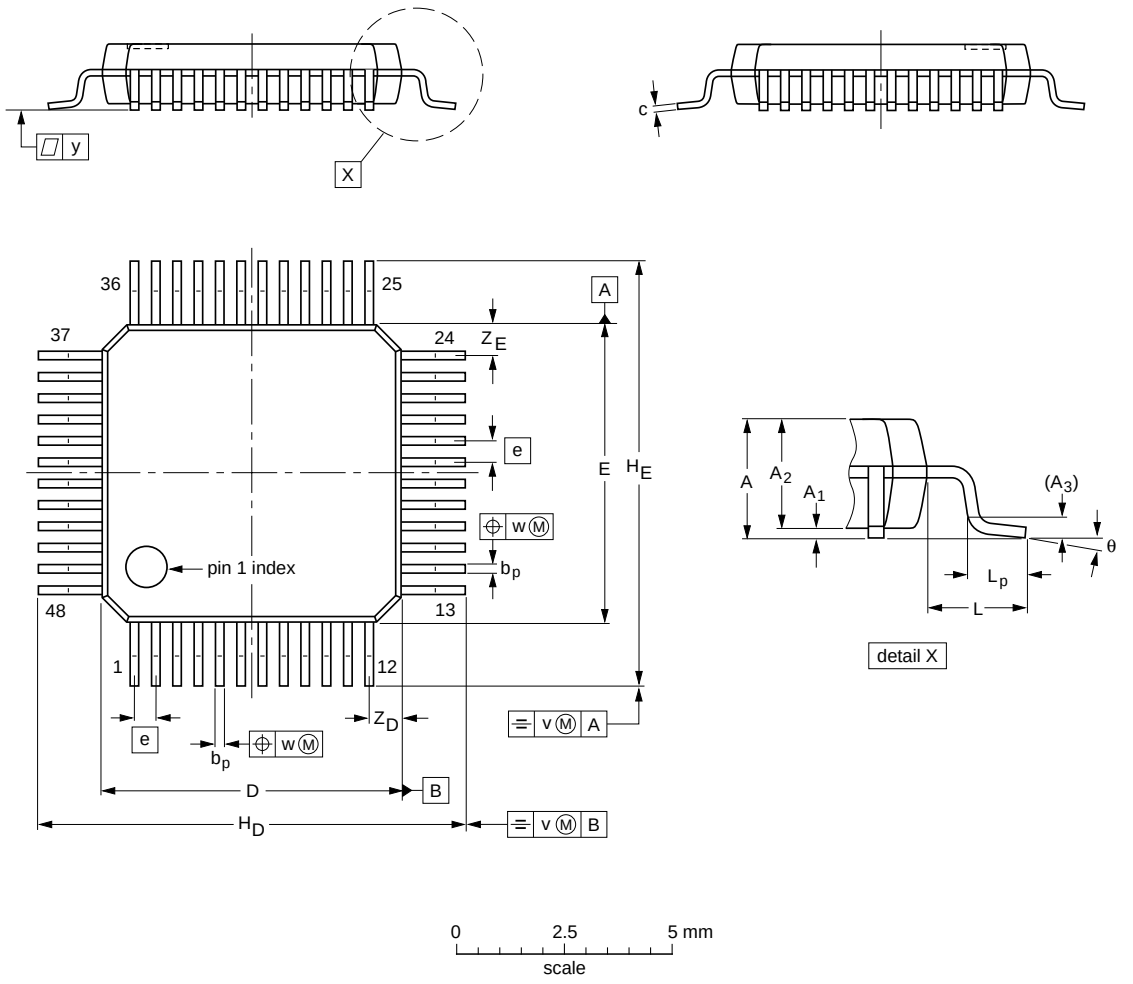
[6] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[7] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[8] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[9] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

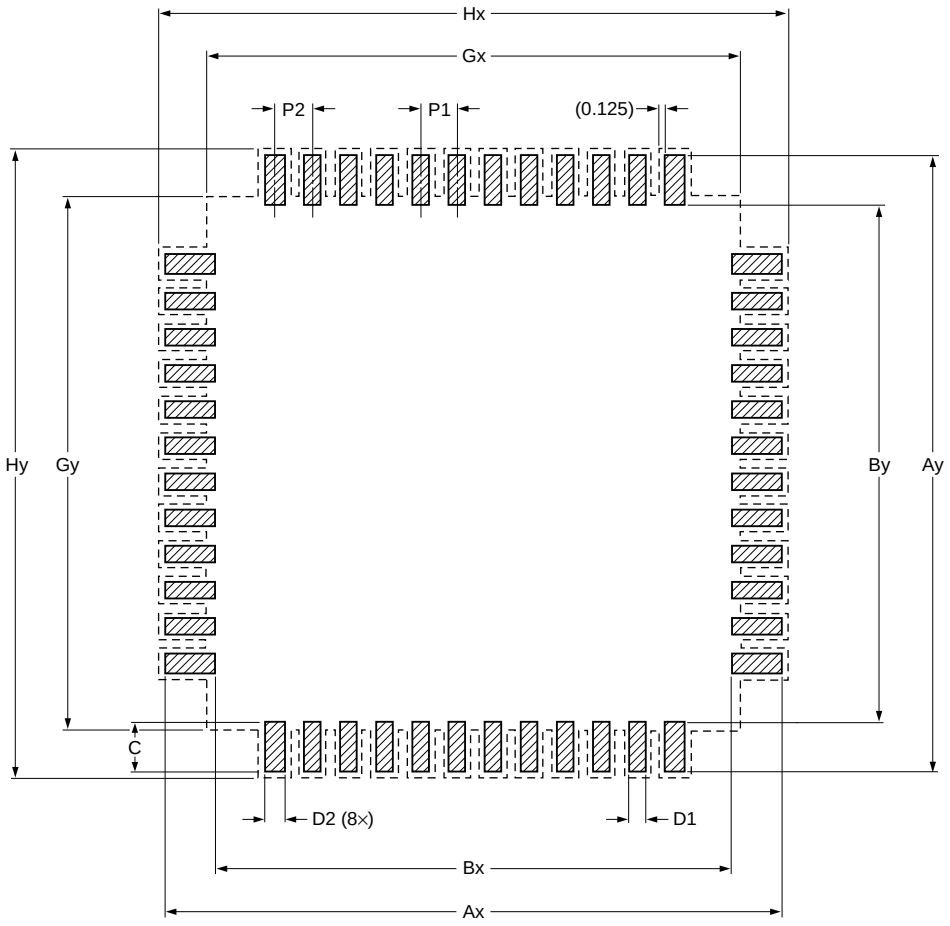
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 26. Package outline SOT313-2 (LQFP48)

14. Soldering

Footprint information for reflow soldering of LQFP48 package **SOT313-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	10.350	10.350	7.350	7.350	1.500	0.280	0.500	7.500	7.500	10.650	10.650

sot313-2_fr

Fig 27. Reflow soldering of the LQFP48 package

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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