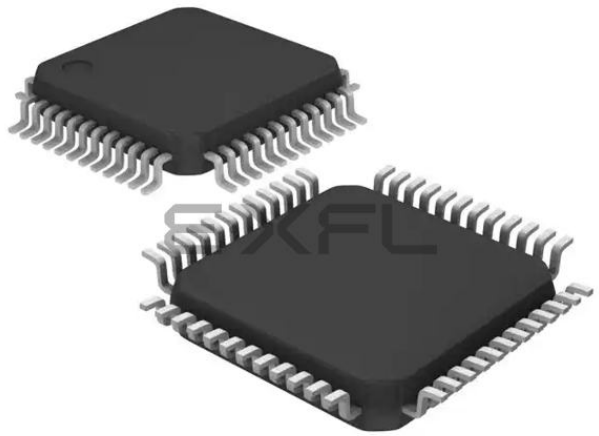

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	45MHz
Connectivity	I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	39
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1227fbd48-301-1

- Crystal oscillator with an operating range of 1 MHz to 25 MHz.
- 12 MHz Internal RC (IRC) oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
- PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
- Clock output function with divider that can reflect the system oscillator clock, IRC clock, main clock, and Watchdog clock.
- Real-Time Clock (RTC).

- Digital peripherals
  - Micro DMA controller with 21 channels.
  - CRC engine.
  - Two UARTs with fractional baud rate generation and internal FIFO. One UART with RS-485 and modem support and one standard UART with IrDA.
  - SSP/SPI controller with FIFO and multi-protocol capabilities.
  - I^2C-bus interface supporting full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode. I^2C-bus pins have programmable glitch filter.
  - Up to 55 General Purpose I/O (GPIO) pins with programmable pull-up resistor, open-drain mode, programmable digital input glitch filter, and programmable input inverter.
  - Programmable output drive on all GPIO pins. Four pins support high-current output drivers.
  - All GPIO pins can be used as edge and level sensitive interrupt sources.
  - Four general purpose counter/timers with four capture inputs and four match outputs (32-bit timers) or two capture inputs and two match outputs (16-bit timers).
  - Windowed WatchDog Timer (WWDT); IEC-60335 Class B certified.
- Analog peripherals
  - One 8-channel, 10-bit ADC.
  - Two highly flexible analog comparators. Comparator outputs can be programmed to trigger a timer match signal or can be used to emulate 555 timer behavior.
- Power
  - Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.
  - Processor wake-up from Deep-sleep mode via start logic using 12 port pins.
  - Processor wake-up from Deep-power down and Deep-sleep modes via the RTC.
  - Brownout detect with three separate thresholds each for interrupt and forced reset.
  - Power-On Reset (POR).
  - Integrated PMU (Power Management Unit).
- Unique device serial number for identification.
- 3.3 V power supply.
- Available as 64-pin and 48-pin LQFP package.

5. Block diagram

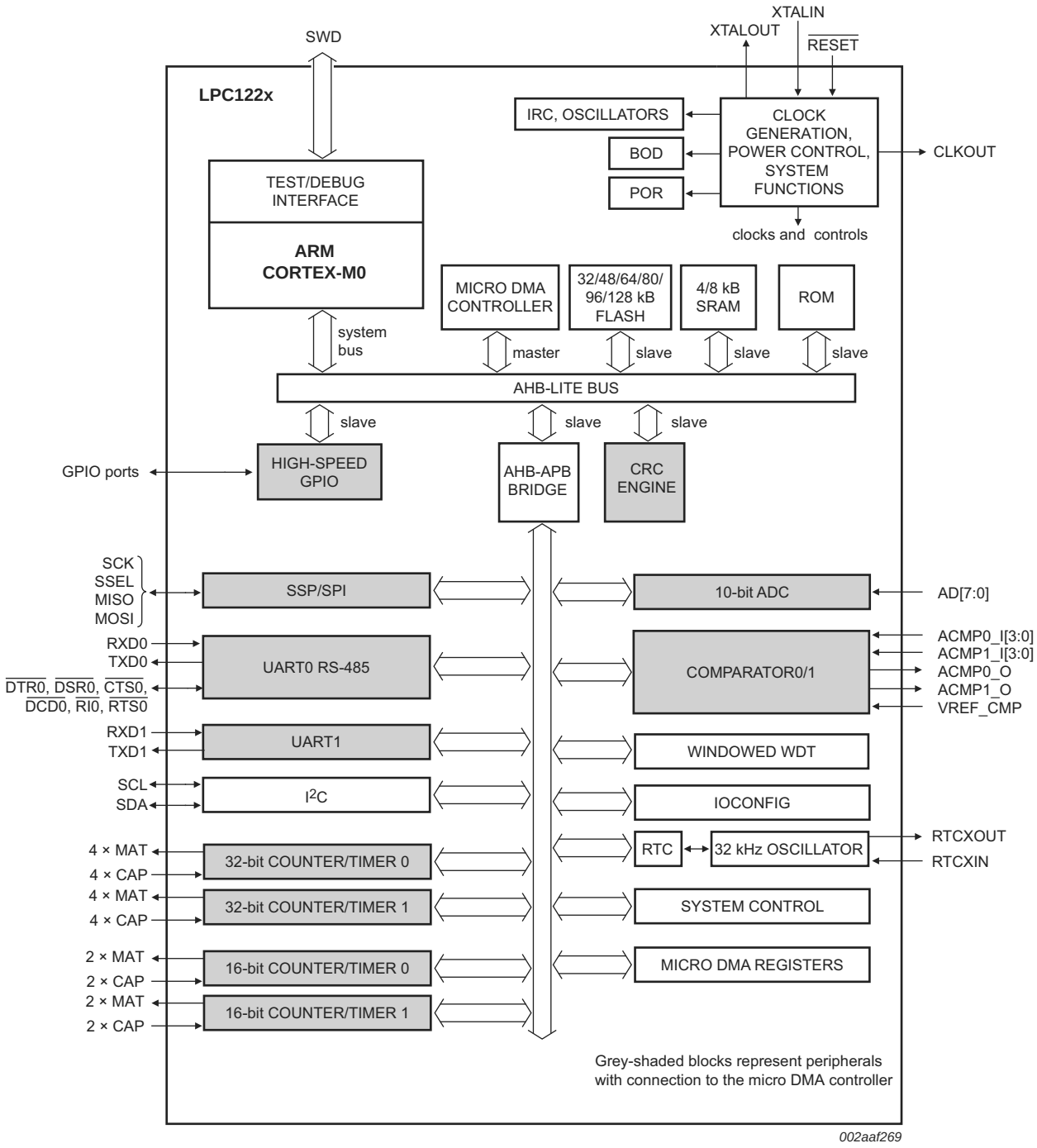


Fig 1. LPC122x block diagram

Table 3. LPC122x pin description *…continued*

Symbol	Pin LQFP48	Pin LQFP64		Start logic input	Type	Reset state [1]	Description
PIO1_5/AD7/ CT16B1_CAP0/ CT16B1_MAT0	41	53	[6] [3]	no	I/O	I; PU	**PIO1_5 —** General purpose digital input/output pin.
					I	-	**AD7 —** A/D converter, input 7.
					I	-	**CT16B1_CAP0 —** Capture input, channel 0 for 16-bit timer 1.
					O	-	**CT16B1_MAT0 —** Match output, channel 0 for 16-bit timer 1.
PIO1_6/ CT16B1_CAP1/ CT16B1_MAT1	42	54	[2] [3]	no	I/O	I; PU	**PIO1_6 —** General purpose digital input/output pin.
					I	-	**CT16B1_CAP1 —** Capture input, channel 1 for 16-bit timer 1.
					O	-	**CT16B1_MAT1 —** Match output, channel 1 for 16-bit timer 1.
PIO2_0 to PIO2_15					I/O		**Port 2 —** Port 2 is a 32-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block. Pins PIO2_16 through PIO2_31 are not available.
PIO2_0/ CT16B0_CAP0/ CT16B0_MAT0/ $\overline{\text{RTS0}}$	-	29	[2] [3]	no	I/O	I; PU	**PIO2_0 —** General purpose digital input/output pin.
					I	-	**CT16B0_CAP0 —** Capture input, channel 0 for 16-bit timer 0.
					O	-	**CT16B0_MAT0 —** Match output, channel 0 for 16-bit timer 0.
					O	-	**$\overline{\text{RTS0}}$ —** Request To Send output for UART0.
PIO2_1/ CT16B0_CAP1/ CT16B0_MAT1/RXD0	-	30	[2] [3]	no	I/O	I; PU	**PIO2_1 —** General purpose digital input/output pin.
					I	-	**CT16B0_CAP1 —** Capture input, channel 1 for 16-bit timer 0.
					O	-	**CT16B0_MAT1 —** Match output, channel 1 for 16-bit timer 0.
					I	-	**RXD0 —** Receiver input for UART0.
PIO2_2/ CT16B1_CAP0/ CT16B1_MAT0/TXD0	-	31	[2] [3]	no	I/O	I; PU	**PIO2_2 —** General purpose digital input/output pin.
					I	-	**CT16B1_CAP0 —** Capture input, channel 0 for 16-bit timer 1.
					O	-	**CT16B1_MAT0 —** Match output, channel 0 for 16-bit timer 1.
					O	-	**TXD0 —** Transmitter output for UART0.
PIO2_3/ CT16B1_CAP1/ CT16B1_MAT1/$\overline{\text{DTR0}}$	-	32	[2] [3]	no	I/O	I; PU	**PIO2_3 —** General purpose digital input/output pin.
					I	-	**CT16B1_CAP1 —** Capture input, channel 1 for 16-bit timer 1.
					O	-	**CT16B1_MAT1 —** Match output, channel 1 for 16-bit timer 1.
					O	-	**$\overline{\text{DTR0}}$ —** Data Terminal Ready output for UART0.
PIO2_4/ CT32B0_CAP0/ CT32B0_MAT0/$\overline{\text{CTS0}}$	-	33	[2] [3]	no	I/O	I; PU	**PIO2_4 —** General purpose digital input/output pin.
					I	-	**CT32B0_CAP0 —** Capture input, channel 0 for 32-bit timer 0.
					O	-	**CT32B0_MAT0 —** Match output, channel 0 for 32-bit timer 0.
					I	-	**$\overline{\text{CTS0}}$ —** Clear To Send input for UART0.
PIO2_5/ CT32B0_CAP1/ CT32B0_MAT1/$\overline{\text{RI0}}$	-	34	[2] [3]	no	I/O	I; PU	**PIO2_5 —** General purpose digital input/output pin.
					I	-	**CT32B0_CAP1 —** Capture input, channel 1 for 32-bit timer 0.
					O	-	**CT32B0_MAT1 —** Match output, channel 1 for 32-bit timer 0.
					I	-	**$\overline{\text{RI0}}$ —** Ring Indicator input for UART0.

Table 4. Pin multiplexing

Peripheral	Function	Type	Available on ports:		
ADC	AD0	I	PIO0_30	-	-
	AD1	I	PIO0_31	-	-
	AD2	I	PIO1_0	-	-
	AD3	I	PIO1_1	-	-
	AD4	I	PIO1_2	-	-
	AD5	I	PIO1_3	-	-
	AD6	I	PIO1_4	-	-
	AD7	I	PIO1_5	-	-
CT16B0	CT16B0_CAP0	I	PIO0_11	PIO0_28	PIO2_0
	CT16B0_CAP1	I	PIO0_12	PIO0_29	PIO2_1
	CT16B0_MAT0	O	PIO0_11	PIO0_28	PIO2_0
	CT16B0_MAT1	O	PIO0_12	PIO0_29	PIO2_1
CT16B1	CT16B1_CAP0	I	PIO0_15	PIO1_5	PIO2_2
	CT16B1_CAP1	I	PIO0_16	PIO1_6	PIO2_3
	CT16B1_MAT0	O	PIO0_15	PIO1_5	PIO2_2
	CT16B1_MAT1	O	PIO0_16	PIO1_6	PIO2_3
CT32B0	CT32B0_CAP0	I	PIO0_1	PIO0_18	PIO2_4
	CT32B0_CAP1	I	PIO0_2	PIO0_19	PIO2_5
	CT32B0_CAP2	I	PIO0_3	PIO0_20	PIO2_6
	CT32B0_CAP3	I	PIO0_4	PIO0_21	PIO2_7
	CT32B0_MAT0	O	PIO0_1	PIO0_18	PIO2_4
	CT32B0_MAT1	O	PIO0_2	PIO0_19	PIO2_5
	CT32B0_MAT2	O	PIO0_3	PIO0_20	PIO2_6
	CT32B0_MAT3	O	PIO0_4	PIO0_21	PIO2_7
CT32B1	CT32B1_CAP0	I	PIO0_6	PIO0_23	PIO2_8
	CT32B1_CAP1	I	PIO0_7	PIO0_24	PIO2_9
	CT32B1_CAP2	I	PIO0_8	PIO0_25	PIO2_10
	CT32B1_CAP3	I	PIO0_9	PIO0_26	PIO2_11
	CT32B1_MAT0	O	PIO0_6	PIO0_23	PIO2_8
	CT32B1_MAT1	O	PIO0_7	PIO0_24	PIO2_9
	CT32B1_MAT2	O	PIO0_8	PIO0_25	PIO2_10
	CT32B1_MAT3	O	PIO0_9	PIO0_26	PIO2_11
UART0	RXD0	I	PIO0_1	PIO2_1	-
	TXD0	O	PIO0_2	PIO2_2	-
	$\overline{\text{CTS0}}$	I	PIO0_7	PIO2_4	-
	$\overline{\text{DCD0}}$	I	PIO0_5	PIO2_6	-
	$\overline{\text{DSR0}}$	I	PIO0_4	PIO2_7	-
	$\overline{\text{DTR0}}$	O	PIO0_3	PIO2_3	-
	$\overline{\text{RI0}}$	I	PIO0_6	PIO2_5	-
	$\overline{\text{RTS0}}$	O	PIO0_0	PIO2_0	-

Table 4. Pin multiplexing

Peripheral	Function	Type	Available on ports:		
UART1	RXD1	I	PIO0_8	PIO2_11	PIO2_12
	TXD1	O	PIO0_9	PIO2_10	PIO2_13
SSP/SPI	SCK	I/O	PIO0_14	-	-
	MISO	I/O	PIO0_16	-	-
	MOSI	I/O	PIO0_17	-	-
	SSEL	I/O	PIO0_15	-	-
I2C	SCL	I/O	PIO0_10	-	-
	SDA	I/O	PIO0_11	-	-
SWD	SWCLK[1]	I	PIO0_18	PIO0_26	-
	SWDIO[1]	I/O	PIO0_25	PIO1_2	-
Reset	$\overline{\text{RESET}}$	I	PIO0_13	-	-
Clockout pin	CLKOUT	O	PIO0_12	-	-

[1] After reset, the SWD functions are selected by default on pins PIO0_26 and PIO0_25.

7. Functional description

7.1 ARM Cortex-M0 processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption.

7.1.1 System tick timer

The ARM Cortex-M0 includes a System Tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval.

7.2 On-chip flash program memory

The LPC122x contain up to 128 kB of on-chip flash memory.

7.3 On-chip SRAM

The LPC122x contain a total of up to 8 kB on-chip static RAM memory.

7.4 Memory map

The LPC122x incorporates several distinct memory regions, shown in the following figures. Figure 4 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 megabyte in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kilobytes of space. This allows simplifying the address decoding for each peripheral.

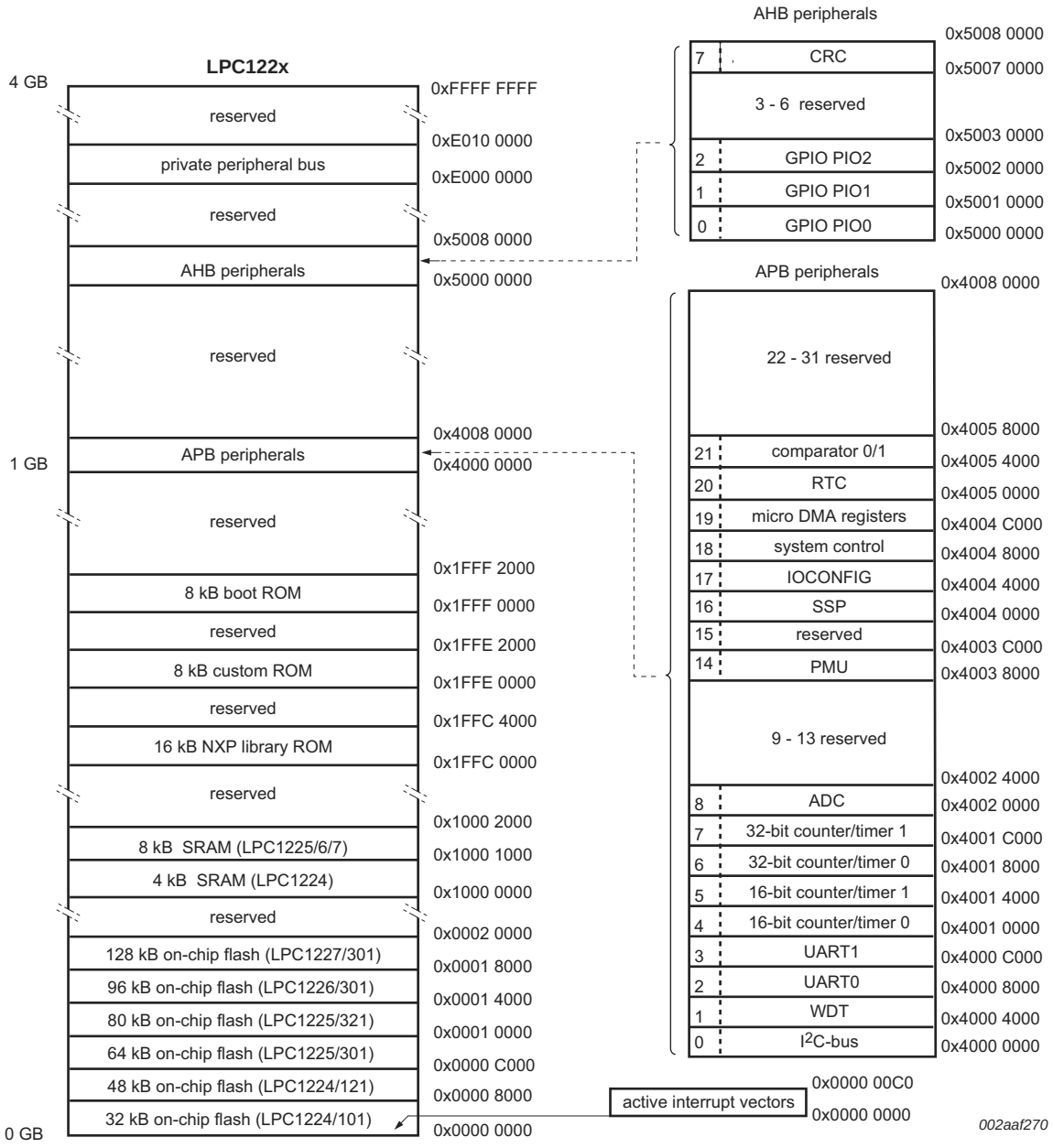


Fig 4. LPC122x memory map

7.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.

7.10.1 Features

- 16-byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto-baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode (UART0).
- Support for modem control (UART0).

7.11 SSP/SPI serial I/O controller

The LPC122x contain one SSP/SPI controller. The SSP/SPI controller is capable of operation on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.11.1 Features

- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.12 I^2C-bus serial I/O controller

The LPC122x contain one I^2C-bus controller.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.12.1 Features

- The I^2C-interface is a standard I^2C-compliant bus interface with open-drain pins and supports I^2C Fast-mode Plus with bit rates of up to 1 Mbit/s.
- Programmable digital glitch filter providing a 60 ns to 1 μs input filter.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.

- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the Internal RC oscillator (IRC) or the Watchdog oscillator. This gives a wide range of potential timing choices of Watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring for increased reliability.

7.17 Real-time clock (RTC)

The RTC provides a basic alarm function or can be used as a long time base counter. The RTC generates an interrupt after counting for a programmed number of cycles of the RTC clock input.

7.17.1 Features

- Uses dedicated 32 kHz ultra low-power oscillator.
- Selectable clock inputs: RTC oscillator (1 Hz, delayed 1 Hz, or 1 kHz clock) or main clock with programmable clock divider.
- 32-bit counter.
- Programmable 32-bit match/compare register.
- Software maskable interrupt when counter and compare registers are identical.
- Generates wake-up from Deep-sleep and Deep power-down modes.

7.18 Clocking and power control

7.18.1 Crystal oscillators

The LPC122x include four independent oscillators. These are the system oscillator, the Internal RC oscillator (IRC), the RTC 32 kHz oscillator (for the RTC only), and the Watchdog oscillator. Except for the RTC oscillator, each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC122x will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 5 for an overview of the LPC122x clock generation.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.18.5.2 Deep-sleep mode

In Deep-sleep mode, the chip is in Sleep mode, and in addition all analog blocks are shut down. As an exception, the user has the option to keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection. Deep-sleep mode allows for additional power savings.

The GPIO pins PIO0_0 to PIO0_11 (up to 12 pins total) and the RTC match interrupt can serve as a wake-up input to the start logic to wake up the chip from Deep-sleep mode.

Unless the watchdog oscillator is selected to run in Deep-sleep mode, the clock source should be switched to IRC before entering Deep-sleep mode, because the IRC can be switched on and off glitch-free.

7.18.5.3 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip with the exception of the Real Time Clock, the four general-purpose registers, and the WAKEUP pin. The LPC122x can wake up from Deep power-down mode via the WAKEUP pin or the RTC match interrupt.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. The $\overline{\text{RESET}}$ pin must also be held HIGH to prevent it from floating while in Deep power-down mode.

7.19 System control

7.19.1 Start logic

The start logic connects external pins to corresponding interrupts in the NVIC. Each pin shown in Table 3 as input to the start logic has an individual interrupt in the NVIC interrupt vector table. The start logic pins can serve as external interrupt pins when the chip is running. In addition, an input signal on the start logic pins can wake up the chip from Deep-sleep mode when all clocks are shut down.

The start logic must be configured in the system configuration block and in the NVIC before being used.

7.19.2 Reset

Reset has four sources on the LPC122x: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

7.20 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug is supported.

7.21 Integer division routines

The LPC122x contain performance-optimized integer division routines with support for up to 32-bit width in the numerator and denominator. Routines for signed and unsigned division and division with remainder are available. The integer division routines are ROM-based to reduce code-size.

9. Thermal characteristics

9.1 Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

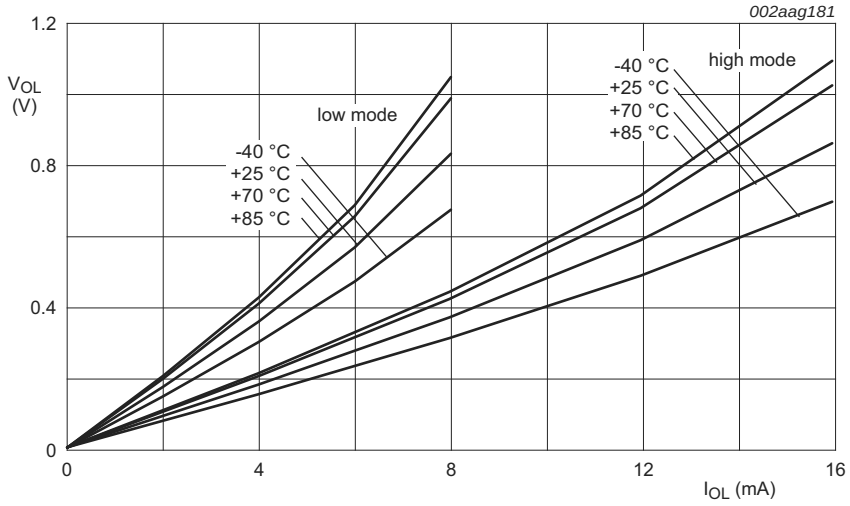
Table 6. Thermal characteristics

V_{DD} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC test board; no air flow	-			
		LQFP64 package		61	-	°C/W
		LQFP48 package		86	-	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case	JEDEC test board	-			
		LQFP64 package		19	-	°C/W
		LQFP48 package		36	-	°C/W
$T_{j(max)}$	maximum junction temperature		-	-	150	°C

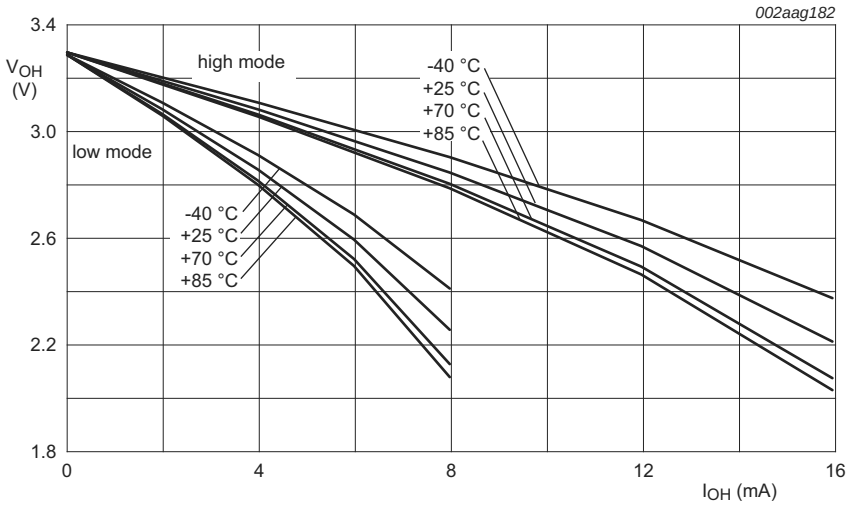
Table 7. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	low mode; I_{OH} = −2 mA		$V_{DD(IO)}$ − 0.4	-	-	V
		high mode; I_{OH} = −4 mA		$V_{DD(IO)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	low mode; I_{OL} = 2 mA		-	-	0.4	V
		high mode; I_{OL} = 4 mA				0.4	
I_{OH}	HIGH-level output current	low mode; $V_{OH} = V_{DD(IO)}$ − 0.4 V		−2	-	-	mA
		high mode; $V_{OH} = V_{DD(IO)}$ − 0.4 V		−4	-	-	mA
I_{OL}	LOW-level output current	low mode; V_{OL} = 0.4 V		2	-	-	mA
		high mode; V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[5]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DDA}$	[5]	-	-	50	mA
I_{pu}	pull-up current	V_I = 0 V		−50	−80	−100	μA
High-drive output pins (PIO0_27, PIO0_28, PIO0_29, PIO0_12)							
I_{IL}	LOW-level input current	V_I = 0 V;		-	-	100	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD(IO)}$;		-	-	100	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(IO)}$;		-	-	100	nA
V_I	input voltage	pin configured to provide a digital function	[2][3] [4]	0	-	$V_{DD(IO)}$	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD(IO)}$	-	-
V_{hys}	hysteresis voltage				-	-	V
V_{OH}	HIGH-level output voltage	low mode; I_{OH} = −20 mA		$V_{DD(IO)}$ − 0.7	-	-	V
		high mode; I_{OH} = −28 mA		$V_{DD(IO)}$ − 0.7	-	-	V
V_{OL}	LOW-level output voltage	low mode; I_{OL} = 12 mA		-	-	0.4	V
		high mode; I_{OL} = 18 mA		-	-	0.4	V



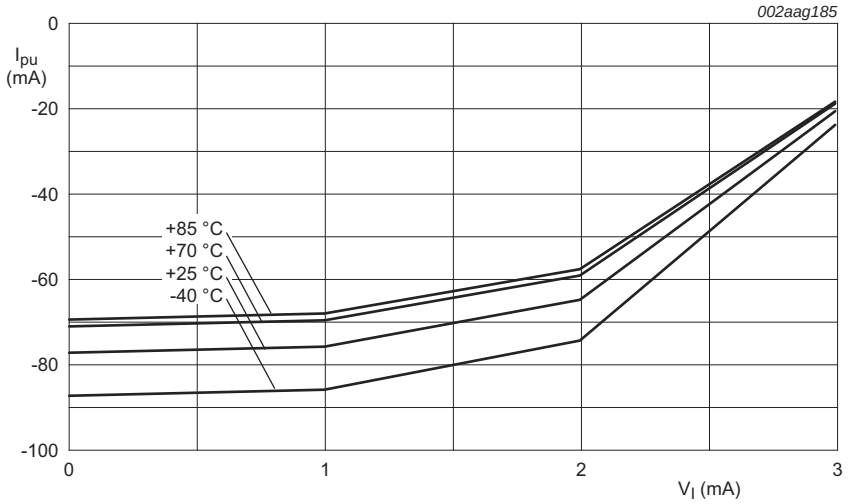
Conditions: $V_{DD(IO)}$ = 3.3 V.

Fig 16. Normal-drive pins: Typical LOW-level output voltage V_{OL} versus LOW-level output current I_{OL}



Conditions: $V_{DD(IO)}$ = 3.3 V.

Fig 17. Normal-drive pins: Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: $V_{DD(IO)}$ = 3.3 V.

Fig 18. Typical pull-up current I_{pu} versus input voltage V_I

11.2 Flash memory

Table 12. Dynamic characteristic: flash memory
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.

Symbol	Parameter	Conditions		Min	Max	Unit
t_{er}	erase time	for one page (512 byte)	[1]	-	20	ms
		for one sector (4 kB)	[1]		162	ms
		for all sectors; mass erase	[1]	-	20	ms
t_{prog}	programming time	one word (4 bytes)	[1]	-	49	µs
		four sequential words	[1]	-	194	µs
		128 bytes (one row of 32 words)	[1]	-	765	µs
N_{endu}	endurance		[2]	20000	-	cycles
t_{ret}	retention time			10	-	years

[1] Erase and programming times are valid over the lifetime of the device (minimum 20000 cycles).

[2] Number of program/erase cycles.

11.3 External clock

Table 13. Dynamic characteristic: external clock
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

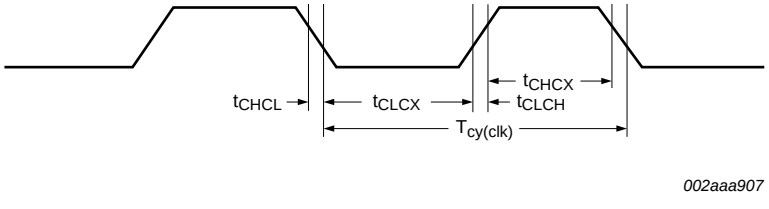


Fig 21. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

12.3 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for the LPC1227FBD64/301 in Table 17.

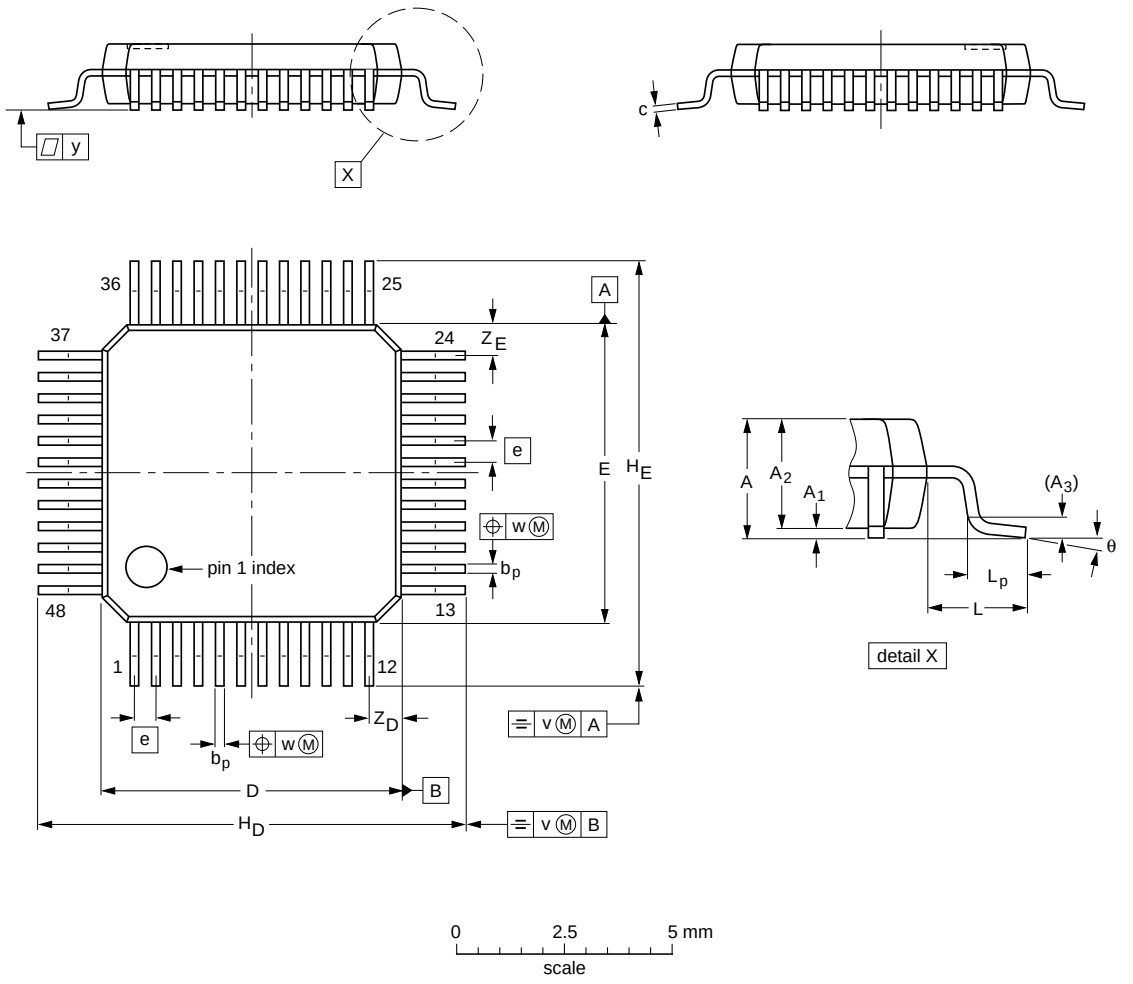
Table 17. ElectroMagnetic Compatibility (EMC) for part LPC1227FBD64/301 (TEM-cell method)

V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =			Unit
		12 MHz	24 MHz	33 MHz	
Input clock: IRC (12 MHz)					
maximum peak level	150 kHz - 30 MHz	−4.2	−3.8	−6.4	dBμV
	30 MHz - 150 MHz	7.3	5.4	9	dBμV
	150 MHz - 1 GHz	16.4	20.1	23.4	dBμV
IEC level[1]	-	M	L	L	-
Input clock: crystal oscillator (12 MHz)					
maximum peak level	150 kHz - 30 MHz	−4.8	−4	−6.6	dBμV
	30 MHz - 150 MHz	6.9	5.6	10	dBμV
	150 MHz - 1 GHz	16.3	20.3	22.3	dBμV
IEC level[1]	-	M	L	L	-

[1] IEC levels refer to *Appendix D in the IEC61967-2 Specification*.

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

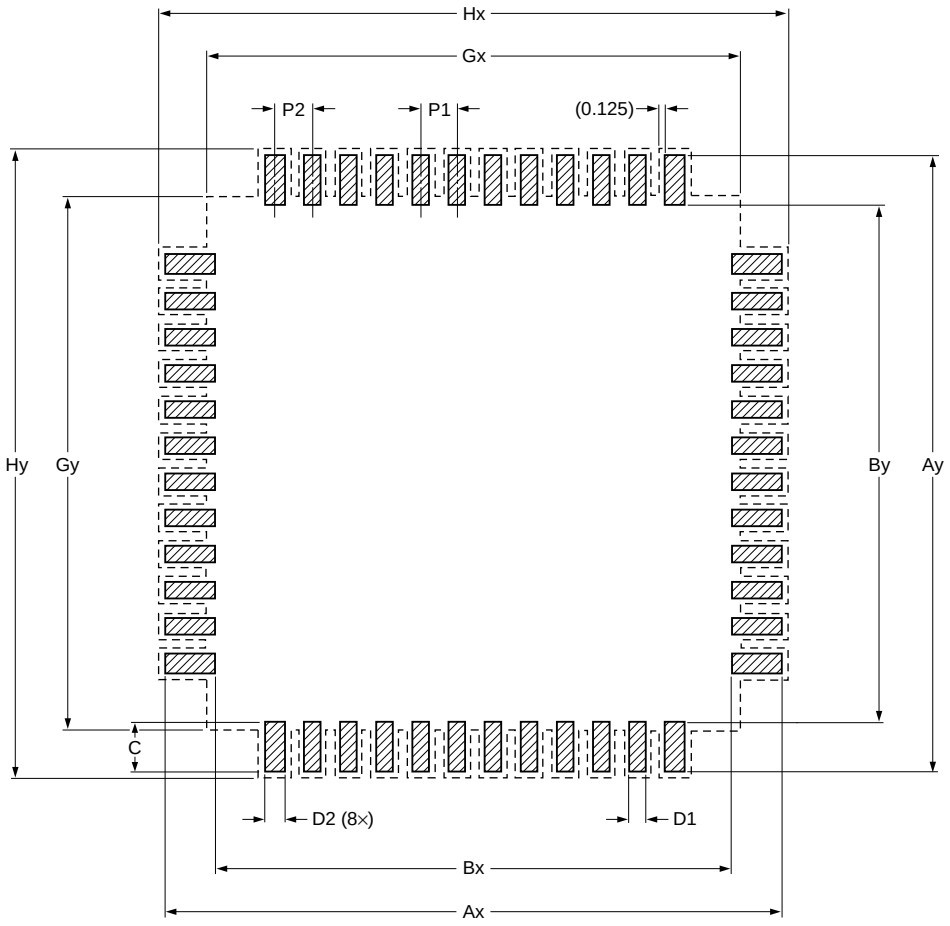
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 26. Package outline SOT313-2 (LQFP48)

14. Soldering

Footprint information for reflow soldering of LQFP48 package **SOT313-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	10.350	10.350	7.350	7.350	1.500	0.280	0.500	7.500	7.500	10.650	10.650

sot313-2_fr

Fig 27. Reflow soldering of the LQFP48 package

15. Abbreviations

Table 18. Abbreviations

Acronym	Description
ADC	Analog-to-Digital-Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
CCITT	Comité Consultatif International Téléphonique et Télégraphique
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
FIFO	First-In-First-Out
GPIO	General Purpose Input/Output
I/O	Input/Output
IrDA	Infrared Data Association
IRC	Internal Resistor-Capacitor
JEDEC	Joint Electron Devices Engineering Council
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
UART	Universal Asynchronous Receiver/Transmitter

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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