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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	45MHz
Connectivity	I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	55
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1227fbd64-301-1

- Crystal oscillator with an operating range of 1 MHz to 25 MHz.
- 12 MHz Internal RC (IRC) oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
- PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
- Clock output function with divider that can reflect the system oscillator clock, IRC clock, main clock, and Watchdog clock.
- Real-Time Clock (RTC).

- Digital peripherals
  - Micro DMA controller with 21 channels.
  - CRC engine.
  - Two UARTs with fractional baud rate generation and internal FIFO. One UART with RS-485 and modem support and one standard UART with IrDA.
  - SSP/SPI controller with FIFO and multi-protocol capabilities.
  - I^2C-bus interface supporting full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode. I^2C-bus pins have programmable glitch filter.
  - Up to 55 General Purpose I/O (GPIO) pins with programmable pull-up resistor, open-drain mode, programmable digital input glitch filter, and programmable input inverter.
  - Programmable output drive on all GPIO pins. Four pins support high-current output drivers.
  - All GPIO pins can be used as edge and level sensitive interrupt sources.
  - Four general purpose counter/timers with four capture inputs and four match outputs (32-bit timers) or two capture inputs and two match outputs (16-bit timers).
  - Windowed WatchDog Timer (WWDT); IEC-60335 Class B certified.
- Analog peripherals
  - One 8-channel, 10-bit ADC.
  - Two highly flexible analog comparators. Comparator outputs can be programmed to trigger a timer match signal or can be used to emulate 555 timer behavior.
- Power
  - Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.
  - Processor wake-up from Deep-sleep mode via start logic using 12 port pins.
  - Processor wake-up from Deep-power down and Deep-sleep modes via the RTC.
  - Brownout detect with three separate thresholds each for interrupt and forced reset.
  - Power-On Reset (POR).
  - Integrated PMU (Power Management Unit).
- Unique device serial number for identification.
- 3.3 V power supply.
- Available as 64-pin and 48-pin LQFP package.

3. Applications

- eMetering
- Lighting
- Industrial networking
- Alarm systems
- White goods

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1227FBD64/301	LQFP64	LQFP64: plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1226FBD64/301	LQFP64	LQFP64: plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1225FBD64/321	LQFP64	LQFP64: plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1225FBD64/301	LQFP64	LQFP64: plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1224FBD64/121	LQFP64	LQFP64: plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1224FBD64/101	LQFP64	LQFP64: plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1227FBD48/301	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1226FBD48/301	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1225FBD48/321	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1225FBD48/301	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1224FBD48/121	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1224FBD48/101	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

Table 3. LPC122x pin description *…continued*

Symbol	Pin LQFP48	Pin LQFP64		Start logic input	Type	Reset state [1]	Description
PIO0_7/$\overline{\text{CTS0}}$/ CT32B1_CAP1/ CT32B1_MAT1	22	26	[2] [3]	yes	I/O	I; PU	**PIO0_7 —** General purpose digital input/output pin.
					I	-	**$\overline{\text{CTS0}}$ —** Clear To Send input for UART0.
					I	-	**CT32B1_CAP1 —** Capture input, channel 1 for 32-bit timer 1.
					O	-	**CT32B1_MAT1 —** Match output, channel 1 for 32-bit timer 1.
PIO0_8/RXD1/ CT32B1_CAP2/ CT32B1_MAT2	23	27	[2] [3]	yes	I/O	I; PU	**PIO0_8 —** General purpose digital input/output pin.
					I	-	**RXD1 —** Receiver input for UART1.
					I	-	**CT32B1_CAP2 —** Capture input, channel 2 for 32-bit timer 1.
					O	-	**CT32B1_MAT2 —** Match output, channel 2 for 32-bit timer 1.
PIO0_9/TXD1/ CT32B1_CAP3/ CT32B1_MAT3	24	28	[2] [3]	yes	I/O	I; PU	**PIO0_9 —** General purpose digital input/output pin.
					O	-	**TXD1 —** Transmitter output for UART1.
					I	-	**CT32B1_CAP3 —** Capture input, channel 3 for 32-bit timer 1.
					O	-	**CT32B1_MAT3 —** Match output, channel 3 for 32-bit timer 1.
PIO0_10/SCL	25	37	[4]	yes	I/O	I; IA	**PIO0_10 —** General purpose digital input/output pin.
					I/O	-	**SCL —** I^2C-bus clock input/output.
PIO0_11/SDA/ CT16B0_CAP0/ CT16B0_MAT0	26	38	[4]	yes	I/O	I; IA	**PIO0_11 —** General purpose digital input/output pin.
					I/O	-	**SDA —** I^2C-bus data input/output.
					I	-	**CT16B0_CAP0 —** Capture input, channel 0 for 16-bit timer 0.
					O	-	**CT16B0_MAT0 —** Match output, channel 0 for 16-bit timer 0.
PIO0_12/CLKOUT/ CT16B0_CAP1/ CT16B0_MAT1	27	39	[9]	no	I/O	I; PU	**PIO0_12 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler. High-current output driver.
					O	-	**CLKOUT —** Clock out pin.
					I	-	**CT16B0_CAP1 —** Capture input, channel 1 for 16-bit timer 0.
					O	-	**CT16B0_MAT1 —** Match output, channel 1 for 16-bit timer 0.
$\overline{\text{RESET}}$/PIO0_13	28	40	[5] [3]	no	I	I; PU	**$\overline{\text{RESET}}$ —** External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
					I/O	-	**PIO0_13 —** General purpose digital input/output pin.
PIO0_14/SCK	29	41	[2] [3]	no	I/O	I; PU	**PIO0_14 —** General purpose digital input/output pin.
					I/O	-	**SCK —** Serial clock for SSP/SPI.
PIO0_15/SSEL/ CT16B1_CAP0/ CT16B1_MAT0	30	42	[2] [3]	no	I/O	I; PU	**PIO0_15 —** General purpose digital input/output pin.
					I/O	-	**SSEL —** Slave select for SSP/SPI.
					I	-	**CT16B1_CAP0 —** Capture input, channel 0 for 16-bit timer 1.
					O	-	**CT16B1_MAT0 —** Match output, channel 0 for 16-bit timer 1.
PIO0_16/MISO/ CT16B1_CAP1/ CT16B1_MAT1	31	43	[2] [3]	no	I/O	I; PU	**PIO0_16 —** General purpose digital input/output pin.
					I/O	-	**MISO —** Master In Slave Out for SSP/SPI.
					I	-	**CT16B1_CAP1 —** Capture input, channel 1 for 16-bit timer 1.
					O	-	**CT16B1_MAT1 —** Match output, channel 1 for 16-bit timer 1.

Table 3. LPC122x pin description *…continued*

Symbol	Pin LQFP48	Pin LQFP64		Start logic input	Type	Reset state [1]	Description
PIO0_17/MOSI	32	44	[2] [3]	no	I/O	I; PU	**PIO0_17 —** General purpose digital input/output pin.
					I/O	-	**MOSI —** Master Out Slave In for SSP/SPI.
PIO0_18/SWCLK/ CT32B0_CAP0/ CT32B0_MAT0	33	45	[2] [3]	no	I/O	I; PU	**PIO0_18 —** General purpose digital input/output pin.
					I	-	**SWCLK —** Serial wire clock, alternate location.
					I	-	**CT32B0_CAP0 —** Capture input, channel 0 for 32-bit timer 0.
					O	-	**CT32B0_MAT0 —** Match output, channel 0 for 32-bit timer 0.
PIO0_19/ACMP0_I0/ CT32B0_CAP1/ CT32B0_MAT1	4	4	[6] [7]	no	I/O	I; PU	**PIO0_19 —** General purpose digital input/output pin.
					I	-	**ACMP0_I0 —** Input 0 for comparator 0.
					I	-	**CT32B0_CAP1 —** Capture input, channel 1 for 32-bit timer 0.
					O	-	**CT32B0_MAT1 —** Match output, channel 1 for 32-bit timer 0
PIO0_20/ACMP0_I1/ CT32B0_CAP2/ CT32B0_MAT2	5	5	[6] [7]	no	I/O	I; PU	**PIO0_20 —** General purpose digital input/output pin.
					I	-	**ACMP0_I1 —** Input 1 for comparator 0.
					I	-	**CT32B0_CAP2 —** Capture input, channel 2 for 32-bit timer 0.
					O	-	**CT32B0_MAT2 —** Match output, channel 2 for 32-bit timer 0.
PIO0_21/ACMP0_I2/ CT32B0_CAP3/ CT32B0_MAT3	6	6	[6] [7]	no	I/O	I; PU	**PIO0_21 —** General purpose digital input/output pin.
					I	-	**ACMP0_I2 —** Input 2 for comparator 0.
					I	-	**CT32B0_CAP3 —** Capture input, channel 3 for 32-bit timer 0.
					O	-	**CT32B0_MAT3 —** Match output, channel 3 for 32-bit timer 0.
PIO0_22/ACMP0_I3	7	7	[6] [7]	no	I/O	I; PU	**PIO0_22 —** General purpose digital input/output pin.
					I	-	**ACMP0_I3 —** Input 3 for comparator 0.
PIO0_23/ ACMP1_I0/ CT32B1_CAP0/ CT32B1_MAT0	8	8	[6] [7]	no	I/O	I; PU	**PIO0_23 —** General purpose digital input/output pin.
					I	-	**ACMP1_I0 —** Input 0 for comparator 1.
					I	-	**CT32B1_CAP0 —** Capture input, channel 0 for 32-bit timer 1.
					O	-	**CT32B1_MAT0 —** Match output, channel 0 for 32-bit timer 1.
PIO0_24/ACMP1_I1/ CT32B1_CAP1/ CT32B1_MAT1	9	9	[6] [7]	no	I/O	I; PU	**PIO0_24 —** General purpose digital input/output pin.
					I	-	**ACMP1_I1 —** Input 1 for comparator 1.
					I	-	**CT32B1_CAP1 —** Capture input, channel 1 for 32-bit timer 1.
					O	-	**CT32B1_MAT1 —** Match output, channel 1 for 32-bit timer 1.
SWDIO/ACMP1_I2/ CT32B1_CAP2/ CT32B1_MAT2/ PIO0_25	10	10	[6] [7]	no	I/O	I; PU	**SWDIO —** Serial wire debug input/output, default location.
					I	-	**ACMP1_I2 —** Input 2 for comparator 1.
					I	-	**CT32B1_CAP2 —** Capture input, channel 2 for 32-bit timer 1.
					O	-	**CT32B1_MAT2 —** Match output, channel 2 for 32-bit timer 1.
					I/O	-	**PIO0_25 —** General purpose digital input/output pin.
SWCLK/ACMP1_I3/ CT32B1_CAP3/ CT32B1_MAT3/ PIO0_26	11	11	[6] [7]	no	I	I; PU	**SWCLK —** Serial wire clock, default location.
					I	-	**ACMP1_I3 —** Input 3 for comparator 1.
					I	-	**CT32B1_CAP3 —** Capture input, channel 3 or 32-bit timer 1.
					O	-	**CT32B1_MAT3 —** Match output, channel 3 for 32-bit timer 1.
					I/O		**PIO0_26 —** General purpose digital input/output pin.

Table 4. Pin multiplexing

Peripheral	Function	Type	Available on ports:		
ADC	AD0	I	PIO0_30	-	-
	AD1	I	PIO0_31	-	-
	AD2	I	PIO1_0	-	-
	AD3	I	PIO1_1	-	-
	AD4	I	PIO1_2	-	-
	AD5	I	PIO1_3	-	-
	AD6	I	PIO1_4	-	-
	AD7	I	PIO1_5	-	-
CT16B0	CT16B0_CAP0	I	PIO0_11	PIO0_28	PIO2_0
	CT16B0_CAP1	I	PIO0_12	PIO0_29	PIO2_1
	CT16B0_MAT0	O	PIO0_11	PIO0_28	PIO2_0
	CT16B0_MAT1	O	PIO0_12	PIO0_29	PIO2_1
CT16B1	CT16B1_CAP0	I	PIO0_15	PIO1_5	PIO2_2
	CT16B1_CAP1	I	PIO0_16	PIO1_6	PIO2_3
	CT16B1_MAT0	O	PIO0_15	PIO1_5	PIO2_2
	CT16B1_MAT1	O	PIO0_16	PIO1_6	PIO2_3
CT32B0	CT32B0_CAP0	I	PIO0_1	PIO0_18	PIO2_4
	CT32B0_CAP1	I	PIO0_2	PIO0_19	PIO2_5
	CT32B0_CAP2	I	PIO0_3	PIO0_20	PIO2_6
	CT32B0_CAP3	I	PIO0_4	PIO0_21	PIO2_7
	CT32B0_MAT0	O	PIO0_1	PIO0_18	PIO2_4
	CT32B0_MAT1	O	PIO0_2	PIO0_19	PIO2_5
	CT32B0_MAT2	O	PIO0_3	PIO0_20	PIO2_6
	CT32B0_MAT3	O	PIO0_4	PIO0_21	PIO2_7
CT32B1	CT32B1_CAP0	I	PIO0_6	PIO0_23	PIO2_8
	CT32B1_CAP1	I	PIO0_7	PIO0_24	PIO2_9
	CT32B1_CAP2	I	PIO0_8	PIO0_25	PIO2_10
	CT32B1_CAP3	I	PIO0_9	PIO0_26	PIO2_11
	CT32B1_MAT0	O	PIO0_6	PIO0_23	PIO2_8
	CT32B1_MAT1	O	PIO0_7	PIO0_24	PIO2_9
	CT32B1_MAT2	O	PIO0_8	PIO0_25	PIO2_10
	CT32B1_MAT3	O	PIO0_9	PIO0_26	PIO2_11
UART0	RXD0	I	PIO0_1	PIO2_1	-
	TXD0	O	PIO0_2	PIO2_2	-
	$\overline{\text{CTS0}}$	I	PIO0_7	PIO2_4	-
	$\overline{\text{DCD0}}$	I	PIO0_5	PIO2_6	-
	$\overline{\text{DSR0}}$	I	PIO0_4	PIO2_7	-
	$\overline{\text{DTR0}}$	O	PIO0_3	PIO2_3	-
	$\overline{\text{RI0}}$	I	PIO0_6	PIO2_5	-
	$\overline{\text{RTS0}}$	O	PIO0_0	PIO2_0	-

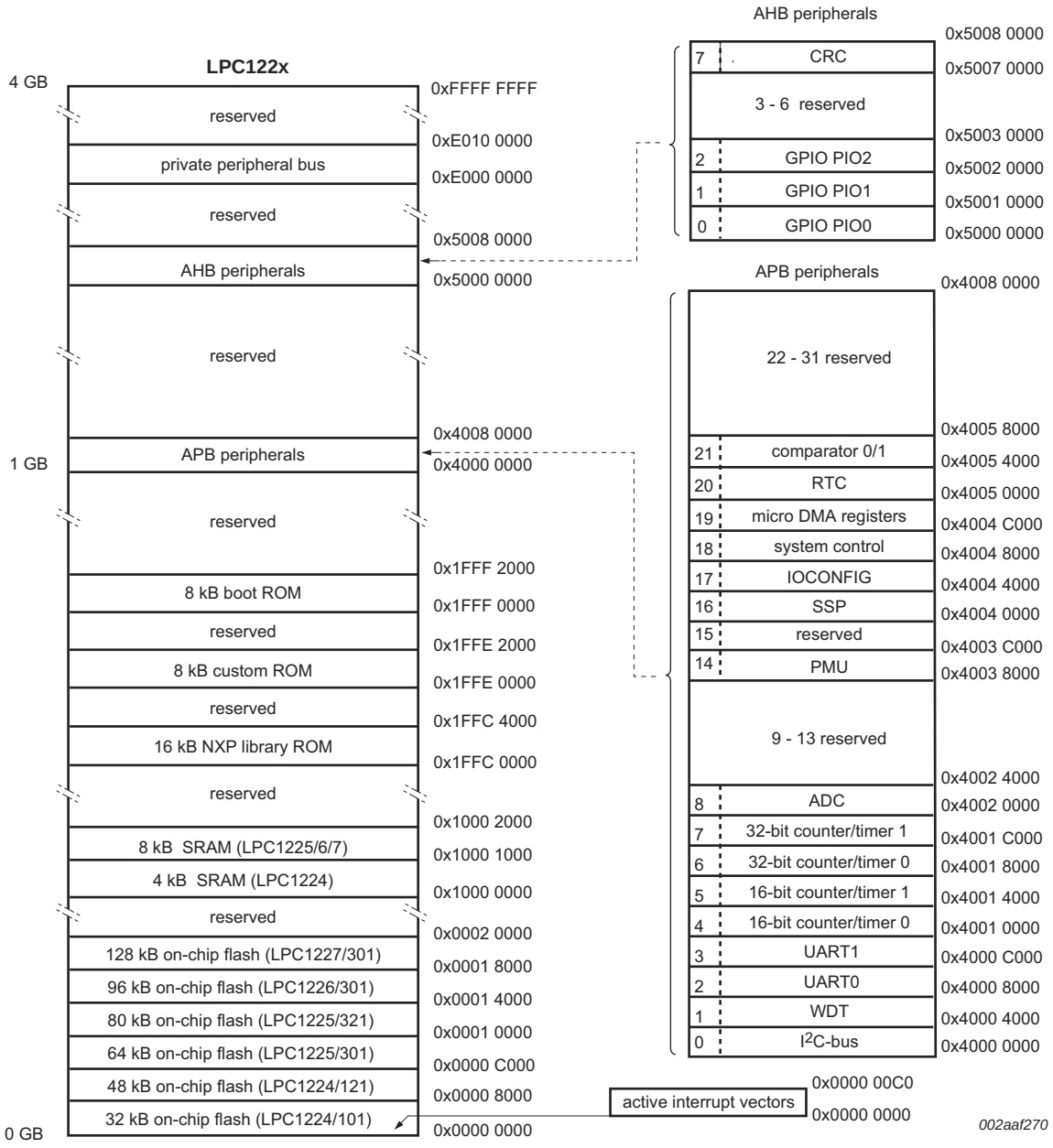


Fig 4. LPC122x memory map

7.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.

- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- The I^2C-bus controller supports multiple address recognition and a bus monitor mode.

7.13 10-bit ADC

The LPC122x contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

7.13.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to $V_{DD(3V3)}$.
- 10-bit conversion time of 257 kHz.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or counter/timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

7.14 Comparator block

The comparator block consists of two analog comparators.

7.14.1 Features

- Up to six selectable external sources per comparator; fully configurable on either positive or negative comparator input channels.
- BOD 0.9 V internal reference voltage selectable on both comparators; configurable on either positive or negative comparator input channels.
- 32-stage voltage ladder internal reference voltage selectable on both comparators; configurable on either positive or negative comparator input channels.
- Voltage ladder source voltage is selectable from an external pin or an internal 3.3 V voltage rail if external power source is not available.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Relaxation oscillator circuitry output for a feedback 555-style timer application.
- Common interrupt connected to NVIC.
- Comparator outputs selectable as synchronous or asynchronous.

- Comparator outputs connect to two timers, allowing for the recording of comparison event time stamps.

7.15 General purpose external event counter/timers

The LPC122x includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes up to four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.15.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- Up to four capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Supports timed DMA requests.

7.16 Windowed WatchDog timer (WWDT)

The purpose of the watchdog is to reset the microcontroller within a windowed amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to ‘feed’ (or reload) the watchdog within a predetermined amount of time.

7.16.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Safe operation: can be locked by software to be always on.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.

- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the Internal RC oscillator (IRC) or the Watchdog oscillator. This gives a wide range of potential timing choices of Watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring for increased reliability.

7.17 Real-time clock (RTC)

The RTC provides a basic alarm function or can be used as a long time base counter. The RTC generates an interrupt after counting for a programmed number of cycles of the RTC clock input.

7.17.1 Features

- Uses dedicated 32 kHz ultra low-power oscillator.
- Selectable clock inputs: RTC oscillator (1 Hz, delayed 1 Hz, or 1 kHz clock) or main clock with programmable clock divider.
- 32-bit counter.
- Programmable 32-bit match/compare register.
- Software maskable interrupt when counter and compare registers are identical.
- Generates wake-up from Deep-sleep and Deep power-down modes.

7.18 Clocking and power control

7.18.1 Crystal oscillators

The LPC122x include four independent oscillators. These are the system oscillator, the Internal RC oscillator (IRC), the RTC 32 kHz oscillator (for the RTC only), and the Watchdog oscillator. Except for the RTC oscillator, each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC122x will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 5 for an overview of the LPC122x clock generation.

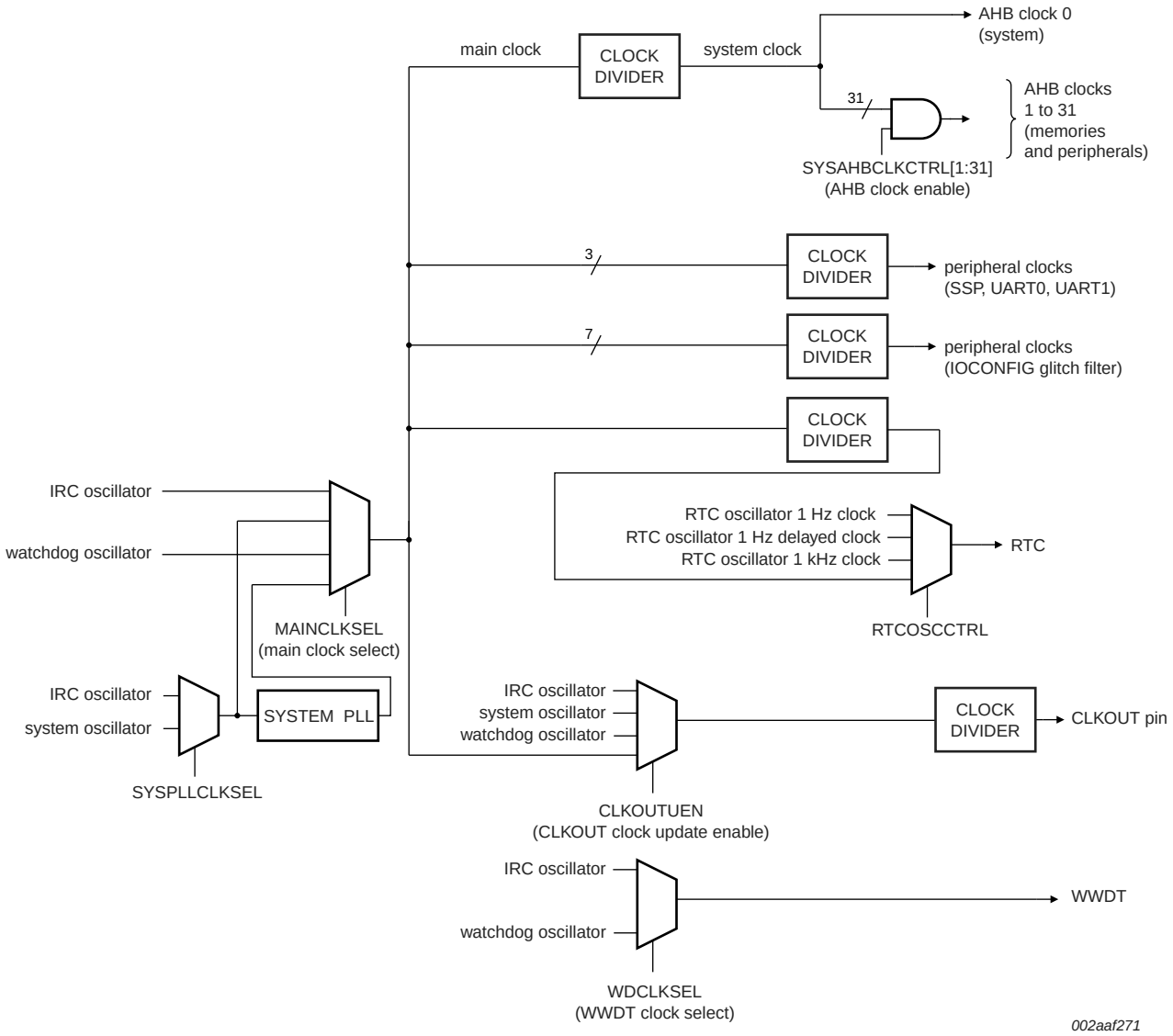


Fig 5. LPC122x clocking generation block diagram

7.18.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC122x use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.18.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL. The ARM processor clock frequency is referred to as CCLK elsewhere in this document.

7.18.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 7.8 kHz and 1.7 MHz. The frequency spread over processing and temperature is ±40 %.

7.18.2 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.18.3 Clock output

The LPC122x features a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.18.4 Wake-up process

The LPC122x begin operation at power-up and when awakened from Deep power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

7.18.5 Power control

The LPC122x support a variety of power control features. There are three special modes of processor power reduction: Sleep mode, Deep-sleep mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.18.5.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

10. Static characteristics

Table 7. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{DD(IO)}$	input/output supply voltage	on pin $V_{DD(IO)}$	3.0	3.3	3.6	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		3.0	3.3	3.6	V
I_{DD}	supply current	Active mode; $V_{DD(3V3)}$ = 3.3 V; T_{amb} = 25 °C; code `while(1){}` executed from flash				
		all peripherals disabled:				
		CCLK = 12 MHz	-	4.6	-	mA
		CCLK = 24 MHz	-	9	-	mA
		CCLK = 33 MHz	-	12.2	-	mA
		all peripherals enabled:				
		CCLK = 12 MHz	-	6.6	-	mA
		CCLK = 24 MHz	-	10.9	-	mA
		CCLK = 33 MHz	-	14.1	-	mA
		Sleep mode; $V_{DD(3V3)}$ = 3.3 V; T_{amb} = 25 °C; all peripherals disabled				
		CCLK = 12 MHz	-	1.8	-	mA
		CCLK = 24 MHz	-	3.3	-	mA
		CCLK = 33 MHz	-	4.4	-	mA
		Deep-sleep mode; $V_{DD(3V3)}$ = 3.3 V; T_{amb} = 25 °C	-	30	-	μA
		Deep power-down mode; $V_{DD(3V3)}$ = 3.3 V; T_{amb} = 25 °C	-	720	-	nA
Normal-drive output pins (Standard port pins, RESET)						
I_{IL}	LOW-level input current	V_I = 0 V;	-	-	100	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD(IO)}$;	-	-	100	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(IO)}$;	-	-	100	nA
V_I	input voltage	pin configured to provide a digital function [2][3][4]	0	-	$V_{DD(IO)}$	V
V_O	output voltage	output active	0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD(IO)}$	-	-	V

Table 7. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	low mode; I_{OH} = −2 mA		$V_{DD(IO)}$ − 0.4	-	-	V
		high mode; I_{OH} = −4 mA		$V_{DD(IO)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	low mode; I_{OL} = 2 mA		-	-	0.4	V
		high mode; I_{OL} = 4 mA				0.4	
I_{OH}	HIGH-level output current	low mode; $V_{OH} = V_{DD(IO)}$ − 0.4 V		−2	-	-	mA
		high mode; $V_{OH} = V_{DD(IO)}$ − 0.4 V		−4	-	-	mA
I_{OL}	LOW-level output current	low mode; V_{OL} = 0.4 V		2	-	-	mA
		high mode; V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[5]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DDA}$	[5]	-	-	50	mA
I_{pu}	pull-up current	V_I = 0 V		−50	−80	−100	μA
High-drive output pins (PIO0_27, PIO0_28, PIO0_29, PIO0_12)							
I_{IL}	LOW-level input current	V_I = 0 V;		-	-	100	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD(IO)}$;		-	-	100	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(IO)}$;		-	-	100	nA
V_I	input voltage	pin configured to provide a digital function	[2][3] [4]	0	-	$V_{DD(IO)}$	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD(IO)}$	-	-
V_{hys}	hysteresis voltage				-	-	V
V_{OH}	HIGH-level output voltage	low mode; I_{OH} = −20 mA		$V_{DD(IO)}$ − 0.7	-	-	V
		high mode; I_{OH} = −28 mA		$V_{DD(IO)}$ − 0.7	-	-	V
V_{OL}	LOW-level output voltage	low mode; I_{OL} = 12 mA		-	-	0.4	V
		high mode; I_{OL} = 18 mA		-	-	0.4	V

10.1 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C and $V_{DD(3V3)}$ = 3.3 V.

Table 8. Peripheral power consumption

Peripheral	Typical current consumption I_{DD} in mA				
	Frequency independent	24 MHz		12 MHz	
		system oscillator + PLL	IRC + PLL	system oscillator	IRC
IRC	0.29	-	-	-	-
PLL (PLL output frequency = 24 MHz)	1.87	-	-	-	-
WDosc (WDosc output frequency = 500 kHz)	0.25	-	-	-	-
BOD	0.06	-	-	-	-
Analog comparator 0/1	-	0.05	0.05	0.03	0.02
ADC	-	1.86	1.85	1.61	1.61
CRC engine	-	0.04	0.04	0.02	0.02
16-bit timer 0 (CT16B0)	-	0.09	0.09	0.04	0.04
16-bit timer 1 (CT16B1)	-	0.09	0.09	0.04	0.04
32-bit timer 0 (CT32B0)	-	0.08	0.08	0.04	0.04
32-bit timer 1 (CT32B1)	-	0.08	0.08	0.04	0.04
GPIO0	-	0.34	0.34	0.17	0.17
GPIO1	-	0.34	0.34	0.17	0.17
GPIO2	-	0.36	0.37	0.18	0.18
I2C	-	0.09	0.09	0.05	0.05
IOCON	-	0.09	0.10	0.05	0.05
RTC	-	0.10	0.10	0.05	0.05
SSP	-	0.30	0.29	0.15	0.15
UART0	-	0.52	0.51	0.26	0.26
UART1	-	0.52	0.51	0.26	0.26
DMA	-	0.18	0.18	0.09	0.09
WWDT	-	0.06	0.06	0.03	0.03

10.2 Power consumption

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC122x user manual*):

- Active mode: all GPIO pins set to input with external pull-up resistors.
- Sleep and Deep-sleep modes: all GPIO pins set to output driving LOW.
- Deep power-down mode: all GPIO pins set to input with external pull-up resistors.

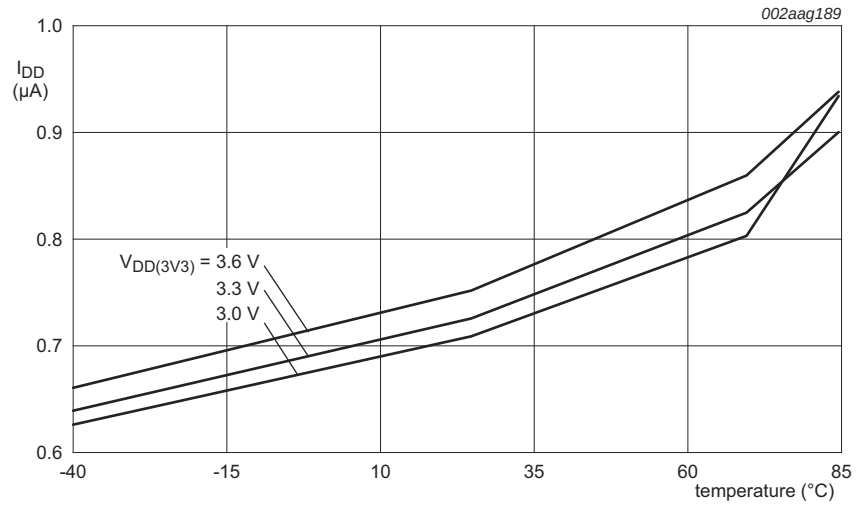
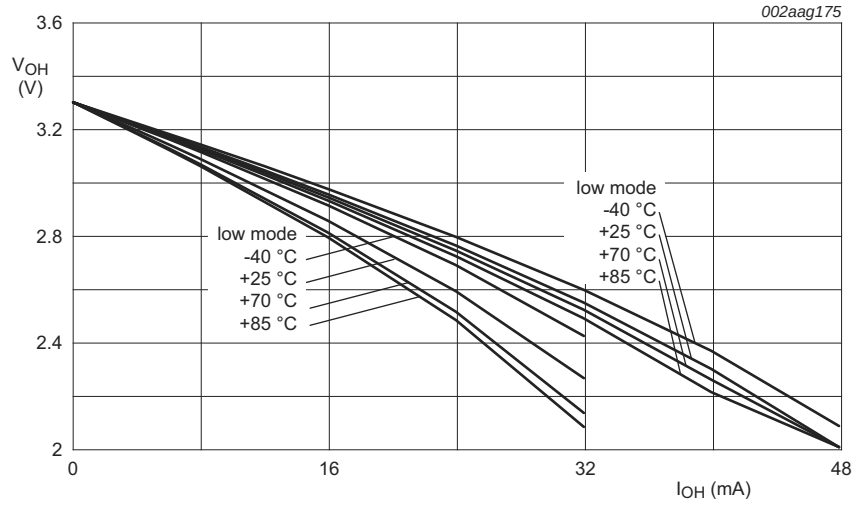


Fig 12. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages $V_{DD(3V3)}$

10.3 Electrical pin characteristics



Conditions: $V_{DD(IO)}$ = 3.3 V

Fig 13. High-drive pins: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}

10.4 ADC characteristics

Table 9. ADC static characteristics

T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 9 MHz, $V_{DD(3V3)}$ = 3.0 V to 3.6 V.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IA}	analog input voltage		0	-	$V_{DD(3V3)}$	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[2][3][4]	-	-	± 1	LSB
$E_{L(adj)}$	integral non-linearity	[2][5]	-	-	± 2.5	LSB
E_O	offset error	[2][6]	-	-	± 1	LSB
E_G	gain error	[2][7]	-	-	± 3	LSB
E_T	absolute error	[2][8]	-	-	± 3	LSB
$f_{c(ADC)}$	ADC conversion frequency		-	-	257	kHz
R_i	input resistance	[9][10]	-	-	3.9	MΩ

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Conditions: V_{SS} = 0 V, $V_{DD(3V3)}$ = 3.3 V.

[3] The ADC is monotonic, there are no missing codes.

[4] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 19.

[5] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 19.

[6] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 19.

[7] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 19.

[8] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 19.

[9] T_{amb} = 25 °C; maximum sampling frequency f_s = 257 kHz and analog input capacitance C_{ia} = 1 pF.

[10] Input resistance R_i depends on the sampling frequency fs: $R_i = 1 / (f_s \times C_{ia})$.

10.5 BOD static characteristics

Table 10. BOD static characteristics[1]
T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1				
		assertion	-	2.25	-	V
		de-assertion	-	2.39	-	V
		interrupt level 2				
		assertion	-	2.54	-	V
		de-assertion	-	2.67	-	V
		interrupt level 3				
		assertion	-	2.83	-	V
		de-assertion	-	2.93	-	V
		reset level 1				
		assertion	-	2.04	-	V
		de-assertion	-	2.18	-	V
		reset level 2				
		assertion	-	2.34	-	V
		de-assertion	-	2.47	-	V
		reset level 3				
		assertion	-	2.62	-	V
		de-assertion	-	2.76	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC122x user manual*.

11.2 Flash memory

Table 12. Dynamic characteristic: flash memory
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.

Symbol	Parameter	Conditions		Min	Max	Unit
t_{er}	erase time	for one page (512 byte)	[1]	-	20	ms
		for one sector (4 kB)	[1]		162	ms
		for all sectors; mass erase	[1]	-	20	ms
t_{prog}	programming time	one word (4 bytes)	[1]	-	49	µs
		four sequential words	[1]	-	194	µs
		128 bytes (one row of 32 words)	[1]	-	765	µs
N_{endu}	endurance		[2]	20000	-	cycles
t_{ret}	retention time			10	-	years

[1] Erase and programming times are valid over the lifetime of the device (minimum 20000 cycles).

[2] Number of program/erase cycles.

11.3 External clock

Table 13. Dynamic characteristic: external clock
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

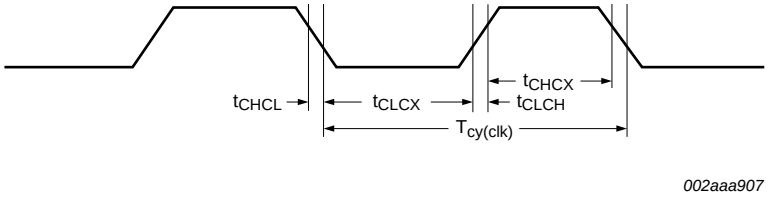
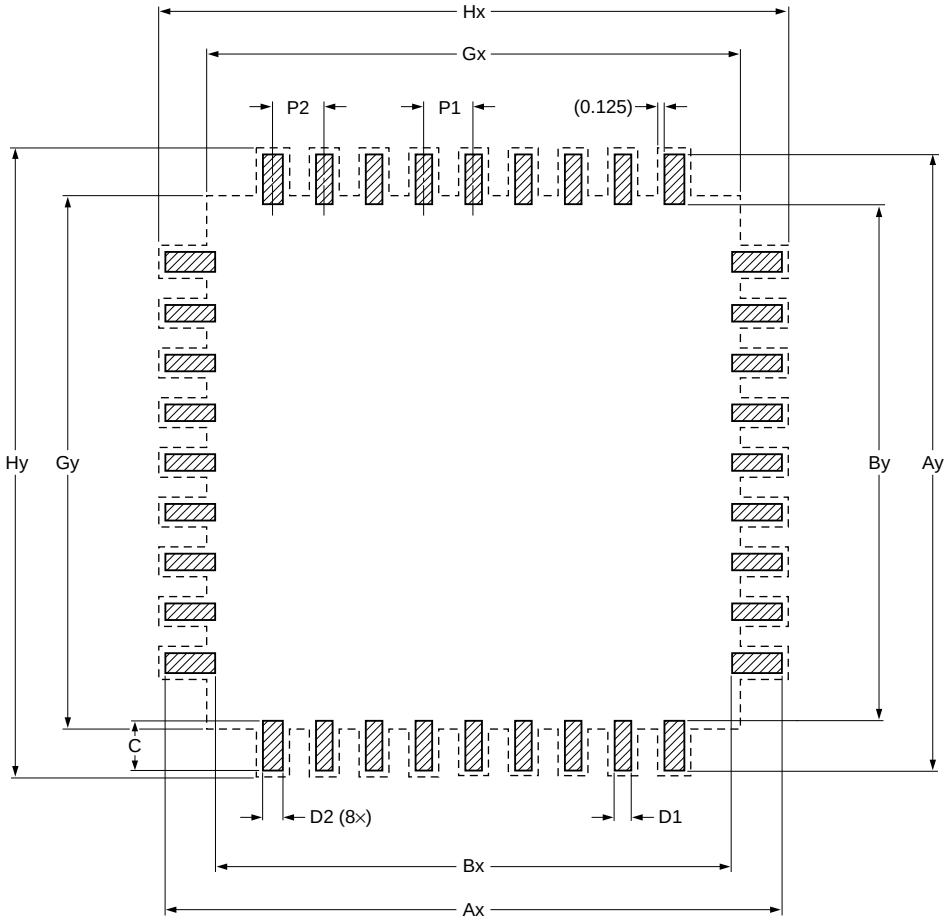


Fig 21. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2_fr

Fig 28. Reflow soldering of the LQFP64 package

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

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