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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

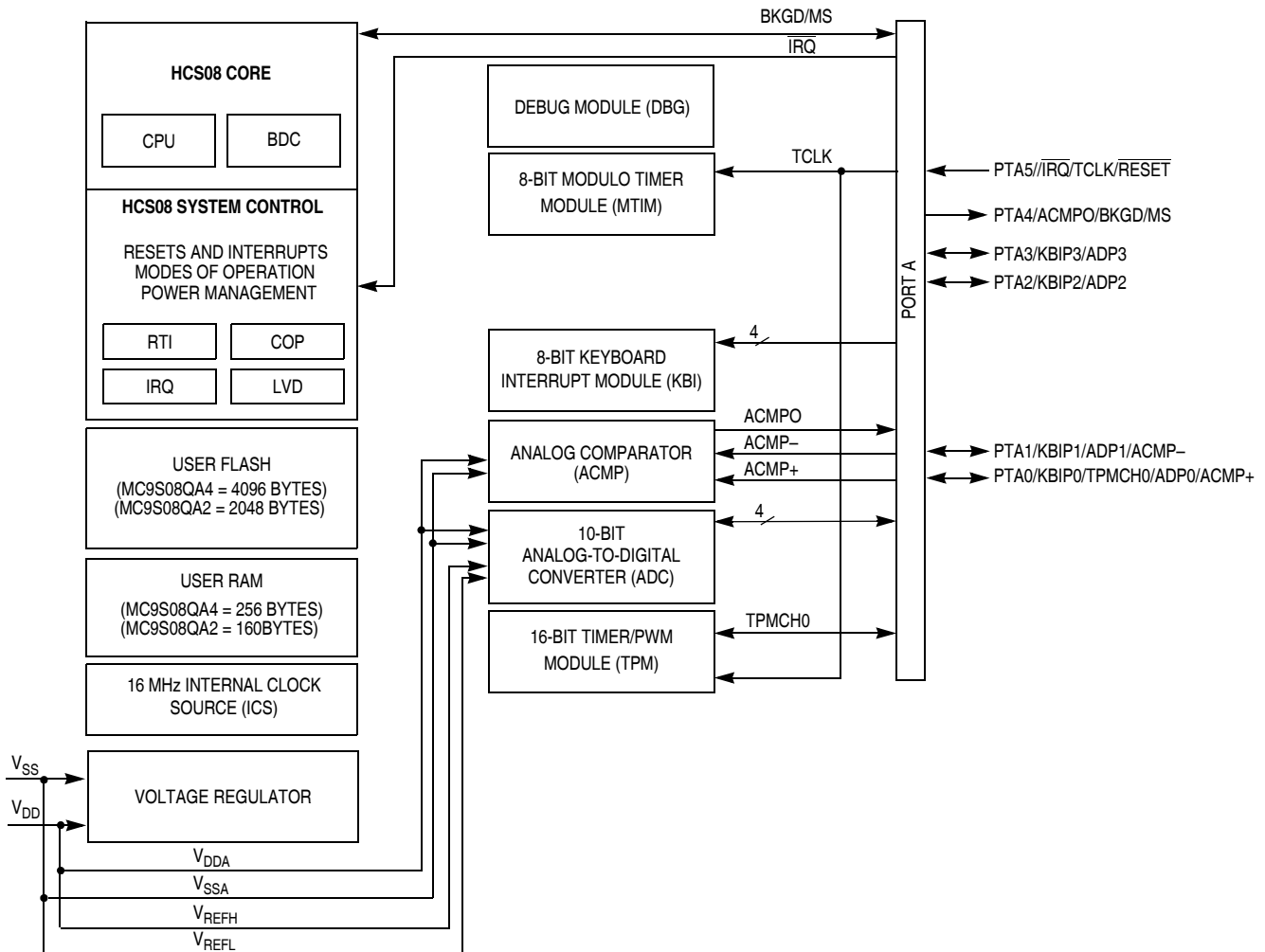
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	4
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN-EP (4x4)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mc9s08qa4cfqe">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mc9s08qa4cfqe</a>

# 1 MCU Block Diagram

The block diagram, [Figure 1](#), shows the structure of the MC9S08QA4 MCU.



**NOTES:**

- 1 Port pins are software configurable with pullup device if input port.
- 2 Port pins are software configurable for output drive strength.
- 3 Port pins are software configurable for output slew rate control.
- 4  $\overline{IRQ}$  contains a software configurable (IRQPDD) pullup device if PTA5 enabled as  $\overline{IRQ}$  pin function (IRQPE = 1).
- 5  $\overline{RESET}$  contains integrated pullup device if PTA5 enabled as reset pin function (RSTPE = 1).
- 6 PTA4 contains integrated pullup device if BKGD enabled (BKGDPE = 1).
- 7 When pin functions as KBI (KBIPEn = 1) and associated pin is configured to enable the pullup device, KBEDGn can be used to reconfigure the pullup as a pulldown device.

**Figure 1. MC9S08QA4 Series Block Diagram**

# 2 Pin Assignments

This section shows the pin assignments in the packages available for the MC9S08QA4 series.

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

**Table 4. ESD and Latch-up Test Conditions**

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	$\Omega$
	Storage capacitance	C	100	pF
	Number of pulses per pin		3	
Machine	Series resistance	R1	0	$\Omega$
	Storage capacitance	C	200	pF
	Number of pulses per pin		3	
Latch-up	Minimum input voltage limit		-2.5	V
	Maximum input voltage limit		7.5	V

**Table 5. ESD and Latch-Up Protection Characteristics**

No.	Rating <sup>1</sup>	Symbol	Min	Max	Unit
1	Human body model (HBM)	$V_{HBM}$	$\pm 2000$	—	V
2	Machine model (MM)	$V_{MM}$	$\pm 200$	—	V
3	Charge device model (CDM)	$V_{CDM}$	$\pm 500$	—	V
4	Latch-up current at $T_A = 85^\circ\text{C}$	$I_{LAT}$	$\pm 100$	—	mA

<sup>1</sup> Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

### 3.5 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

**Table 6. DC Characteristics (Temperature Range = -40 to 85°C Ambient)**

Parameter	Symbol	Min	Typical	Max	Unit
Supply voltage (run, wait, and stop modes)	$V_{DD}$ (V <sub>DD</sub> falling)	1.8	—	3.6	V
	$V_{DD}$ (V <sub>DD</sub> rising)	$V_{LVDL}$ (rising)	—	3.6	
Minimum RAM retention supply voltage applied to $V_{DD}$	$V_{RAM}$	$V_{por}^{1,2}$	—	—	V
Low-voltage detection threshold	$V_{LVD}$ (V <sub>DD</sub> falling)	1.80	1.82	1.91	V
	$V_{LVD}$ (V <sub>DD</sub> rising)	1.88	1.90	1.99	
Low-voltage warning threshold	$V_{LVW}$ (V <sub>DD</sub> falling)	2.08	2.1	2.2	V

## Electrical Characteristics

**Table 6. DC Characteristics (Temperature Range = –40 to 85°C Ambient) (continued)**

Parameter ( $V_{DD}$ rising)	Symbol	Min	Typical	Max	Unit
		2.16	2.19	2.27	
Power on reset (POR) re-arm voltage	$V_{por}$	—	1.4	—	V
Bandgap voltage reference	$V_{BG}$	1.18	1.20	1.21	V
Input high voltage ( $V_{DD} > 2.3$ V) (all digital inputs)	$V_{IH}$	$0.70 \times V_{DD}$	—	—	V
Input high voltage ( $1.8$ V $\leq V_{DD} \leq 2.3$ V) (all digital inputs)		$0.85 \times V_{DD}$	—	—	
Input low voltage ( $V_{DD} > 2.3$ V) (all digital inputs)	$V_{IL}$	—	—	$0.35 \times V_{DD}$	V
Input low voltage ( $1.8$ V $\leq V_{DD} \leq 2.3$ V) (all digital inputs)		—	—	$0.30 \times V_{DD}$	
Input hysteresis (all digital inputs)	$V_{hys}$	$0.06 \times V_{DD}$	—	—	V
Input leakage current (per pin) $V_{In} = V_{DD}$ or $V_{SS}$ , all input-only pins	$I_{In}$	—	0.025	1.0	$\mu$ A
High impedance (off-state) leakage current (per pin) $V_{In} = V_{DD}$ or $V_{SS}$ , all input/output	$I_{OZ}$	—	0.025	1.0	$\mu$ A
Internal pullup resistors <sup>3,4</sup>	$R_{PU}$	17.5	—	52.5	k $\Omega$
Internal pulldown resistor (KBI)	$R_{PD}$	17.5	—	52.5	k $\Omega$
Output high voltage — low drive (PTxDSn = 0) $I_{OH} = -2$ mA ( $V_{DD} \geq 1.8$ V)	$V_{OH}$	$V_{DD} - 0.5$	—	—	V
Output high voltage — high drive (PTxDSn = 1) $I_{OH} = -10$ mA ( $V_{DD} \geq 2.7$ V) $I_{OH} = -6$ mA ( $V_{DD} \geq 2.3$ V) $I_{OH} = -3$ mA ( $V_{DD} \geq 1.8$ V)		$V_{DD} - 0.5$	—	—	
Maximum total $I_{OH}$ for all port pins	$I_{OHT}$	—	—	60	mA
Output low voltage — low drive (PTxDSn = 0) $I_{OL} = 2.0$ mA ( $V_{DD} \geq 1.8$ V)	$V_{OL}$	—	—	0.5	V
Output low voltage — high drive (PTxDSn = 1) $I_{OL} = 10.0$ mA ( $V_{DD} \geq 2.7$ V) $I_{OL} = 6$ mA ( $V_{DD} \geq 2.3$ V) $I_{OL} = 3$ mA ( $V_{DD} \geq 1.8$ V)		—	—	0.5	
		—	—	0.5	
Maximum total $I_{OL}$ for all port pins	$I_{OLT}$	—	—	60	mA
DC injection current <sup>2, 5, 6, 7</sup> $V_{In} < V_{SS}$ , $V_{In} > V_{DD}$ Single pin limit Total MCU limit, includes sum of all stressed pins	$I_{IC}$	-0.2 -5	— —	0.2 5	mA mA
Input capacitance (all non-supply pins)	$C_{In}$	—	—	7	pF

<sup>1</sup> RAM will retain data down to POR voltage. RAM data not guaranteed to be valid following a POR.

<sup>2</sup> This parameter is characterized and not tested on each device.

<sup>3</sup> Measurement condition for pull resistors:  $V_{In} = V_{SS}$  for pullup and  $V_{In} = V_{DD}$  for pulldown.

<sup>4</sup> PTA5/ $\overline{IRQ}$ / $\overline{TCLK}$ / $\overline{RESET}$  pullup resistor may not pull up to the specified minimum  $V_{IH}$ . However, all ports are functionally tested to guarantee that a logic 1 will be read on any port input when the pullup is enabled and no DC load is present on the pin.

<sup>5</sup> All functional non-supply pins are internally clamped to  $V_{SS}$  and  $V_{DD}$ .

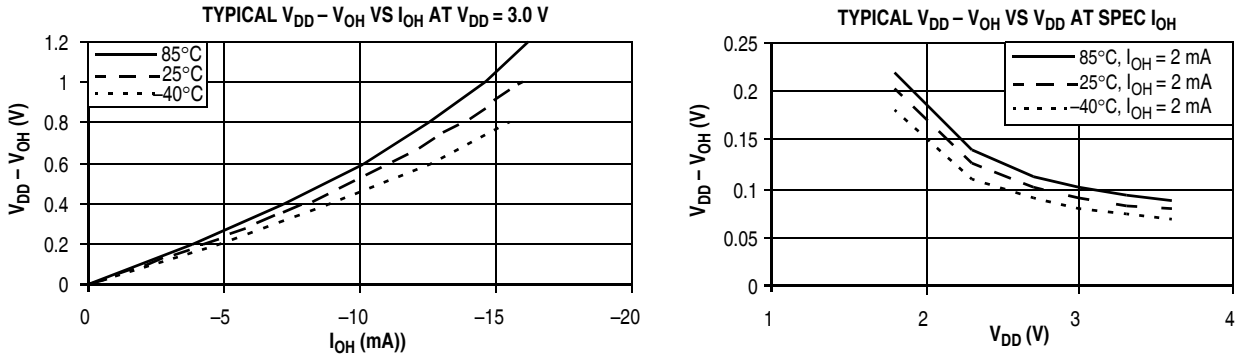


Figure 6. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

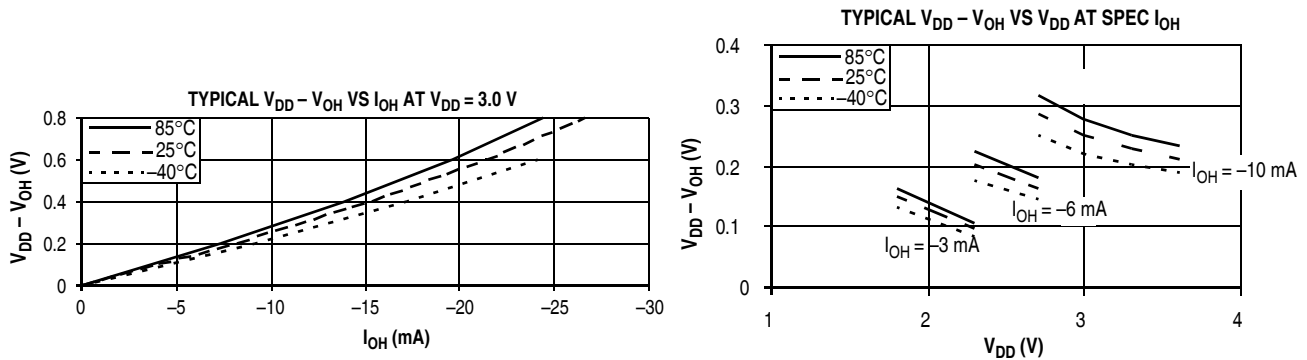


Figure 7. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

### 3.6 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 7. Supply Current Characteristics

Parameter	Symbol	$V_{DD}$ (V) <sup>1</sup>	Typical <sup>2</sup>	Max	T (°C)
Run supply current <sup>3</sup> measured in FBE mode at $f_{Bus} = 8$ MHz	$R1_{DD}$	3	3.5 mA	5 mA	85
		2	2.6 mA	—	85
Run supply current <sup>3</sup> measured in FBE mode at $f_{Bus} = 1$ MHz	$R1_{DD}$	3	490 $\mu$ A	1 mA	85
		2	370 $\mu$ A	—	85
Wait mode supply current <sup>4</sup> measured in FBE at 8 MHz	$W1_{DD}$	3	1 mA	1.5 mA	85
Stop1 mode supply current	$S11_{DD}$	3	475 nA	1.2 $\mu$ A	85
		2	470 nA	—	85
Stop2 mode supply current	$S21_{DD}$	3	600 nA	2 $\mu$ A	85
		2	550 nA	—	85
Stop3 mode supply current	$S31_{DD}$	3	750 nA	6 $\mu$ A	85
		2	680 nA	—	85
RT1 adder to stop1, stop2, or stop3 <sup>4</sup>	—	3	300 nA	—	85
		2	300 nA	—	85
LVD adder to stop3 (LVDE = LVDSE = 1) <sup>4</sup>	—	3	70 $\mu$ A	—	85
		2	60 $\mu$ A	—	85

- <sup>1</sup> 3 V values are 100% tested; 2 V values are characterized but not tested.  
<sup>2</sup> Typical values are measured at 25 °C.  
<sup>3</sup> Does not include any DC loads on port pins.  
<sup>4</sup> Most customers are expected to find that auto-wakeup from a stop mode can be used instead of the higher current wait mode.

### 3.7 Internal Clock Source (ICS) Characteristics

Table 8. ICS Specifications (Temperature Range = -40 to 85°C Ambient)

Characteristic	Symbol	Min	Typical <sup>1</sup>	Max	Unit
Internal reference start-up time	$t_{IRST}$	—	60	100	$\mu$ s
Average internal reference frequency — untrimmed	$f_{int\_ut}$	25	32.7	41.66	kHz
Average internal reference frequency — trimmed	$f_{int\_t}$	31.25	—	39.06	kHz
DCO output frequency range — untrimmed	$f_{dco\_ut}$	12.8	16.8	21.33	MHz
DCO output frequency range — trimmed	$f_{dco\_t}$	16	—	20	MHz
Resolution of trimmed DCO output frequency at fixed voltage and temperature <sup>2</sup>	$\Delta f_{dco\_res\_t}$	—	$\pm 0.1$	$\pm 0.2$	% $f_{dco}$
Total deviation of DCO output from trimmed frequency <sup>2</sup> At 8 MHz over full voltage and temperature range At 8 MHz and 3.6 V from 0 to 70 °C	$\Delta f_{dco\_t}$	—	-1.0 to 0.5 $\pm 0.5$	$\pm 2$ $\pm 1$	% $f_{dco}$
FLL acquisition time <sup>2,3</sup>	$t_{Acquire}$	—	—	1.5	ms
Long term jitter of DCO output clock (averaged over 2 ms interval)	$C_{Jitter}$	—	0.02	0.2	% $f_{dco}$

<sup>1</sup> Data in Typical column was characterized at 3.0 V, 25 °C, or is typical recommended value.

<sup>2</sup> This parameter is characterized and not tested on each device.

<sup>3</sup> This specification applies to any time the FLL reference source or reference divider is changed, trim value changed.

## Electrical Characteristics

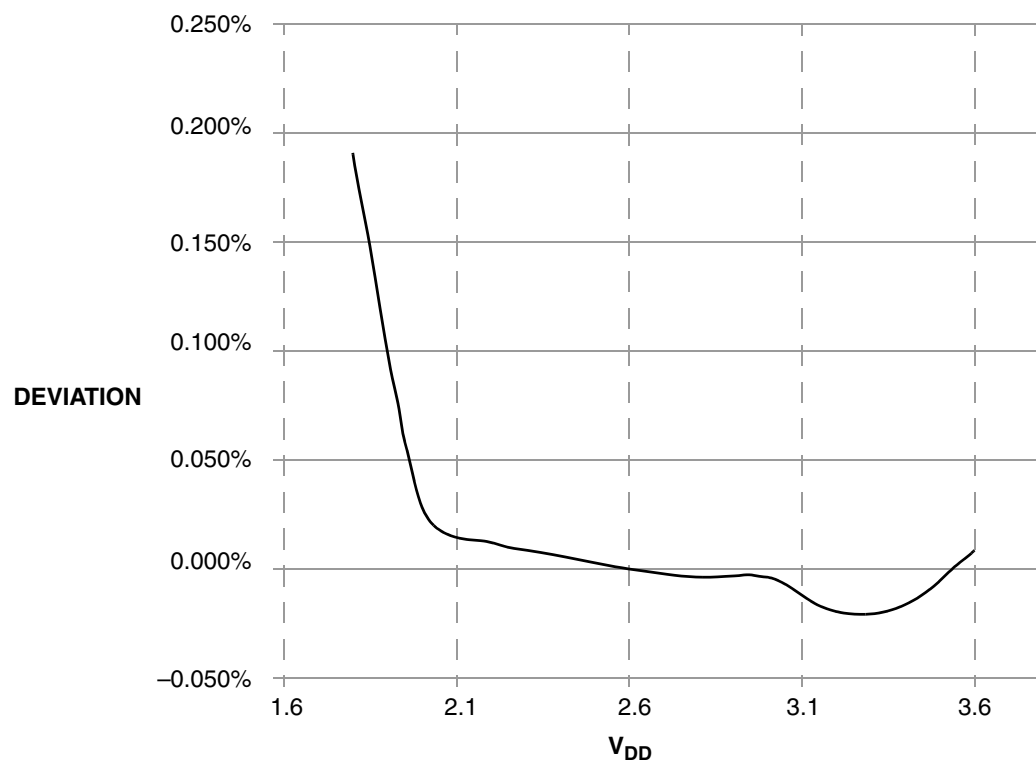


Figure 8. Deviation of DCO Output from Trimmed Frequency (8 MHz, 25 °C)

## 3.8 AC Characteristics

This section describes timing characteristics for each peripheral system.

### 3.8.1 Control Timing

**Table 9. Control Timing**

Parameter	Symbol	Min	Typical <sup>1</sup>	Max	Unit
Bus frequency ( $t_{cyc} = 1/f_{Bus}$ )	$f_{Bus}$	0	—	10	MHz
Real-time interrupt internal oscillator period (see Table 9)	$t_{RTI}$	700	1000	1300	$\mu s$
External reset pulse width <sup>2</sup>	$t_{extrst}$	100	—	—	ns
$\overline{IRQ}$ pulse width Asynchronous path <sup>2</sup> Synchronous path <sup>3</sup>	$t_{LIH}$	100 1.5 $t_{cyc}$	—	—	ns
KBIPx pulse width Asynchronous path <sup>2</sup> Synchronous path <sup>3</sup>	$t_{LIH}, t_{HIL}$	100 1.5 $t_{cyc}$	—	—	ns
Port rise and fall time (load = 50 pF) <sup>4</sup> Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	$t_{Rise}, t_{Fall}$	— —	3 30	— —	ns
BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	$t_{MSSU}$	500	—	—	ns
BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes <sup>5</sup>	$t_{MSH}$	100	—	—	$\mu s$

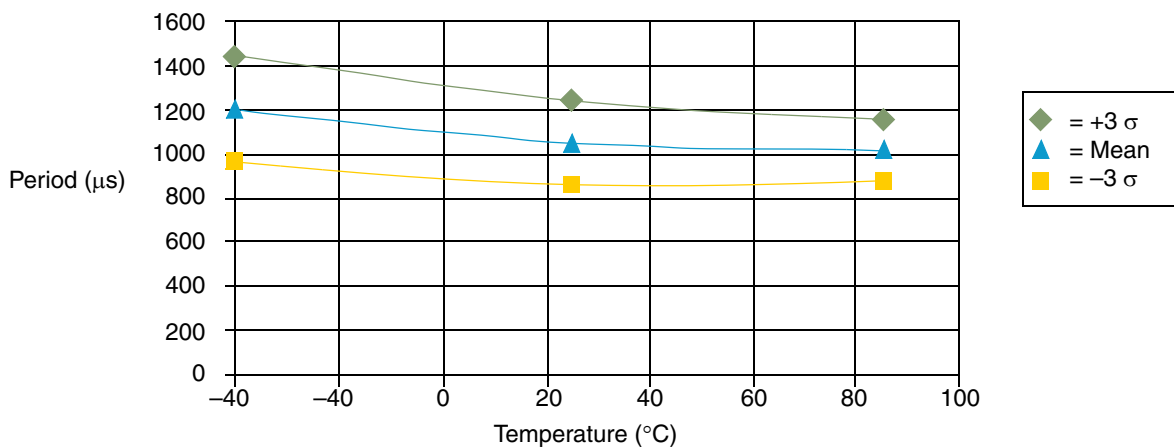
<sup>1</sup> Data in Typical column was characterized at 3.0 V, 25°C.

<sup>2</sup> This is the shortest pulse that is guaranteed to be recognized.

<sup>3</sup> This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

<sup>4</sup> Timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$  levels. Temperature range -40°C to 85°C.

<sup>5</sup> To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of  $t_{MSH}$  after  $V_{DD}$  rises above  $V_{LVD}$ .


**Figure 9. Typical RTI Clock Period vs. Temperature**



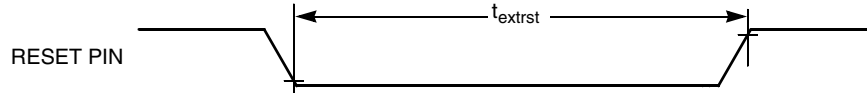


Figure 10. Reset Timing

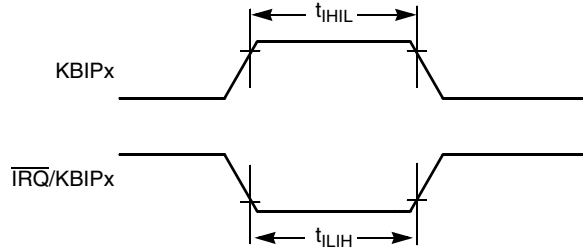


Figure 11.  $\overline{IRQ}/KBIPx$  Timing

### 3.8.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 10. TPM/MTIM Input Timing

Function	Symbol	Min	Max	Unit
External clock frequency	$f_{TCLK}$	0	$f_{Bus}/4$	Hz
External clock period	$t_{TCLK}$	4	—	$t_{cyc}$
External clock high time	$t_{clkh}$	1.5	—	$t_{cyc}$
External clock low time	$t_{clkl}$	1.5	—	$t_{cyc}$
Input capture pulse width	$t_{ICPW}$	1.5	—	$t_{cyc}$

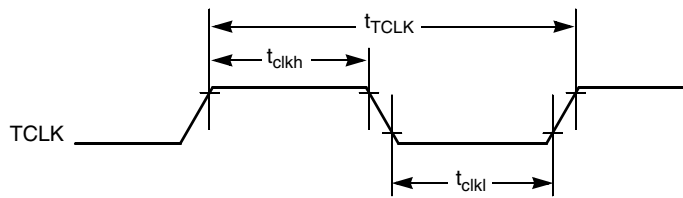


Figure 12. Timer External Clock

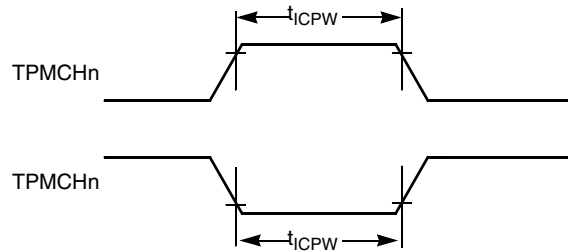


Figure 13. Timer Input Capture Pulse

### 3.9 Analog Comparator (ACMP) Electricals

Table 11. Analog Comparator Electrical Specifications

Characteristic	Symbol	Min	Typical	Max	Unit
Supply voltage	$V_{DD}$	1.80	—	3.60	V
Supply current (active)	$I_{DDAC}$	—	20	—	$\mu\text{A}$
Analog input voltage	$V_{AIN}$	$V_{SS} - 0.3$	—	$V_{DD}$	V
Analog input offset voltage	$V_{AIO}$	—	20	40	mV
Analog comparator hysteresis	$V_H$	3.0	9.0	15.0	mV
Analog input leakage current	$I_{ALKG}$	—	—	1.0	$\mu\text{A}$
Analog comparator initialization delay	$t_{AINIT}$	—	—	1.0	$\mu\text{s}$

### 3.10 ADC Characteristics

Table 12. 3 V 10-Bit ADC Operating Conditions

Characteristic	Conditions	Symbol	Min	Typical <sup>1</sup>	Max	Unit	Comment
Supply voltage	Absolute	$V_{DD}$	1.8	—	3.6	V	
Input voltage		$V_{ADIN}$	$V_{SS}$	—	$V_{DD}$	V	
Input capacitance		$C_{ADIN}$	—	4.5	5.5	pF	
Input resistance		$R_{ADIN}$	—	5	7	$k\Omega$	
Analog source resistance	10 bit mode $f_{ADCK} > 4 \text{ MHz}$ $f_{ADCK} < 4 \text{ MHz}$	$R_{AS}$	—	—	5	$k\Omega$	External to MCU
	8 bit mode (all valid $f_{ADCK}$ )		—	—	10		
ADC conversion clock frequency	High Speed (ADLPC=0)	$f_{ADCK}$	0.4	—	8.0	MHz	
	Low Power (ADLPC=1)		0.4	—	4.0		

<sup>1</sup> Typical values assume  $V_{DD} = 3.0 \text{ V}$ ,  $\text{Temp} = 25^\circ\text{C}$ ,  $f_{ADCK} = 1.0 \text{ MHz}$  unless otherwise stated. Typical values are for reference only and are not tested in production.

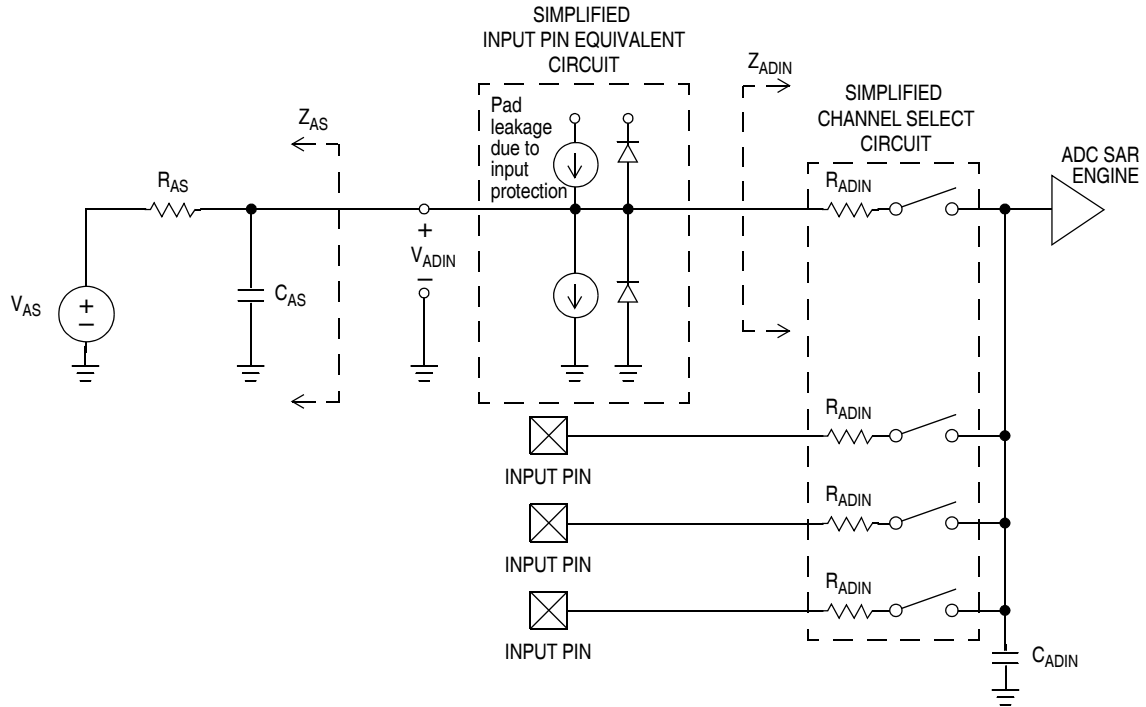


Figure 14. ADC Input Impedance Equivalency Diagram

Table 13. 3 V 10-Bit ADC Characteristics

Characteristic	Conditions	Symbol	Min	Typical <sup>1</sup>	Max	Unit	Comment
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		I <sub>DDAD</sub>	—	120	—	μA	
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		I <sub>DDAD</sub>	—	202	—	μA	
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		I <sub>DDAD</sub>	—	288	—	μA	
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		I <sub>DDAD</sub>	—	532	646	μA	
ADC asynchronous clock source	High speed (ADLPC=0)	f <sub>ADACK</sub>	2	3.3	5	MHz	t <sub>ADACK</sub> = 1/f <sub>ADACK</sub>
	Low power (ADLPC=1)		1.25	2	3.3		

Table 13. 3 V 10-Bit ADC Characteristics (continued)

Characteristic	Conditions	Symbol	Min	Typical <sup>1</sup>	Max	Unit	Comment	
Conversion time (including sample time)	Short sample (ADLSMP=0)	$t_{ADC}$	—	20	—	ADCK cycles	See MC9S08QA4 Series <i>Reference Manual</i> for conversion time variances	
	Long sample (ADLSMP=1)		—	40	—			
Sample time	Short sample (ADLSMP=0)	$t_{ADS}$	—	3.5	—	ADCK cycles		
	Long sample (ADLSMP=1)		—	23.5	—			
Total unadjusted error	10-bit mode	$E_{TUE}$	—	$\pm 1.5$	$\pm 3.5$	LSB <sup>2</sup>		
	8-bit mode		—	$\pm 0.7$	$\pm 1.5$			
Differential non-linearity	10-bit mode	DNL	—	$\pm 0.5$	$\pm 1.0$	LSB <sup>2</sup>		Monotonicity and no missing codes guaranteed
	8-bit mode		—	$\pm 0.3$	$\pm 0.5$			
Integral non-linearity	10-bit mode	INL	—	$\pm 0.5$	$\pm 1.0$	LSB <sup>2</sup>		
	8-bit mode		—	$\pm 0.3$	$\pm 0.5$			
Zero-scale error	10-bit mode	$E_{ZS}$	—	$\pm 1.5$	$\pm 2.1$	LSB <sup>2</sup>	$V_{ADIN} = V_{SS}$	
	8-bit mode		—	$\pm 0.5$	$\pm 0.7$			
Full-scale error	10-bit mode	$E_{FS}$	0	$\pm 1.0$	$\pm 1.5$	LSB <sup>2</sup>	$V_{ADIN} = V_{DD}$	
	8-bit mode		0	$\pm 0.5$	$\pm 0.5$			
Quantization error	10-bit mode	$E_Q$	—	—	$\pm 0.5$	LSB <sup>2</sup>		
	8-bit mode		—	—	$\pm 0.5$			
Input leakage error	10-bit mode	$E_{IL}$	0	$\pm 0.2$	$\pm 4$	LSB <sup>2</sup>	Pad leakage <sup>3*</sup> $R_{AS}$	
	8-bit mode		0	$\pm 0.1$	$\pm 1.2$			
Temp sensor slope	-40°C – 25°C	m	—	1.646	—	mV/°C		
	25°C – 85°C		—	1.769	—			
Temp sensor voltage	25°C	$V_{TEMP25}$	—	701.2	—	mV		

<sup>1</sup> Typical values assume  $V_{DD} = 3.0$  V, Temp = 25°C,  $f_{ADCK} = 1.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

<sup>2</sup>  $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$

<sup>3</sup> Based on input pad leakage current. Refer to pad electricals.

### 3.11 Flash Specifications

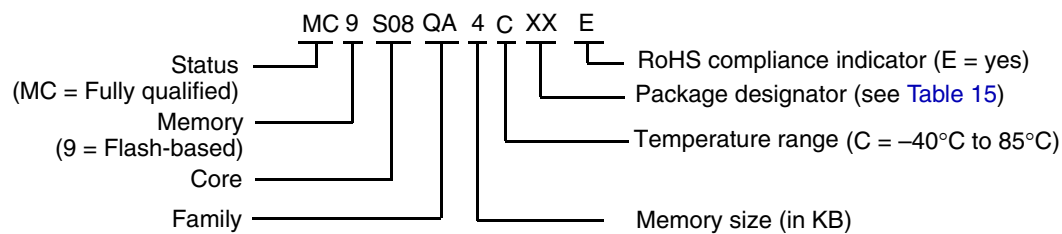
This section provides details about program/erase times and program-erase endurance for the flash memory.

## 4 Ordering Information

This section contains ordering numbers for MC9S08QA4 series devices. See below for an example of the device numbering system.

**Table 15. Device Numbering System**

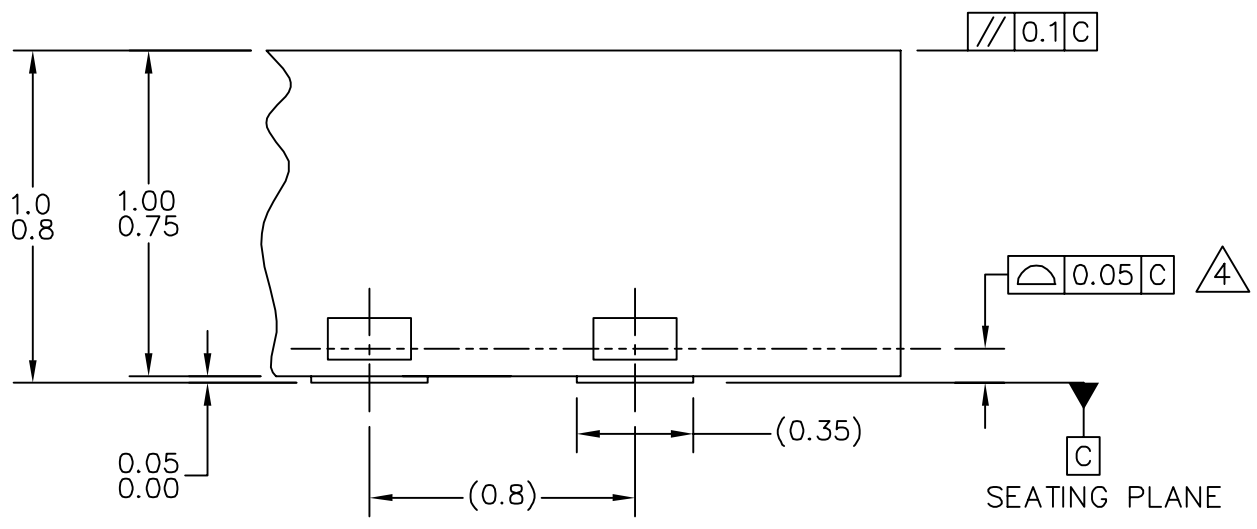
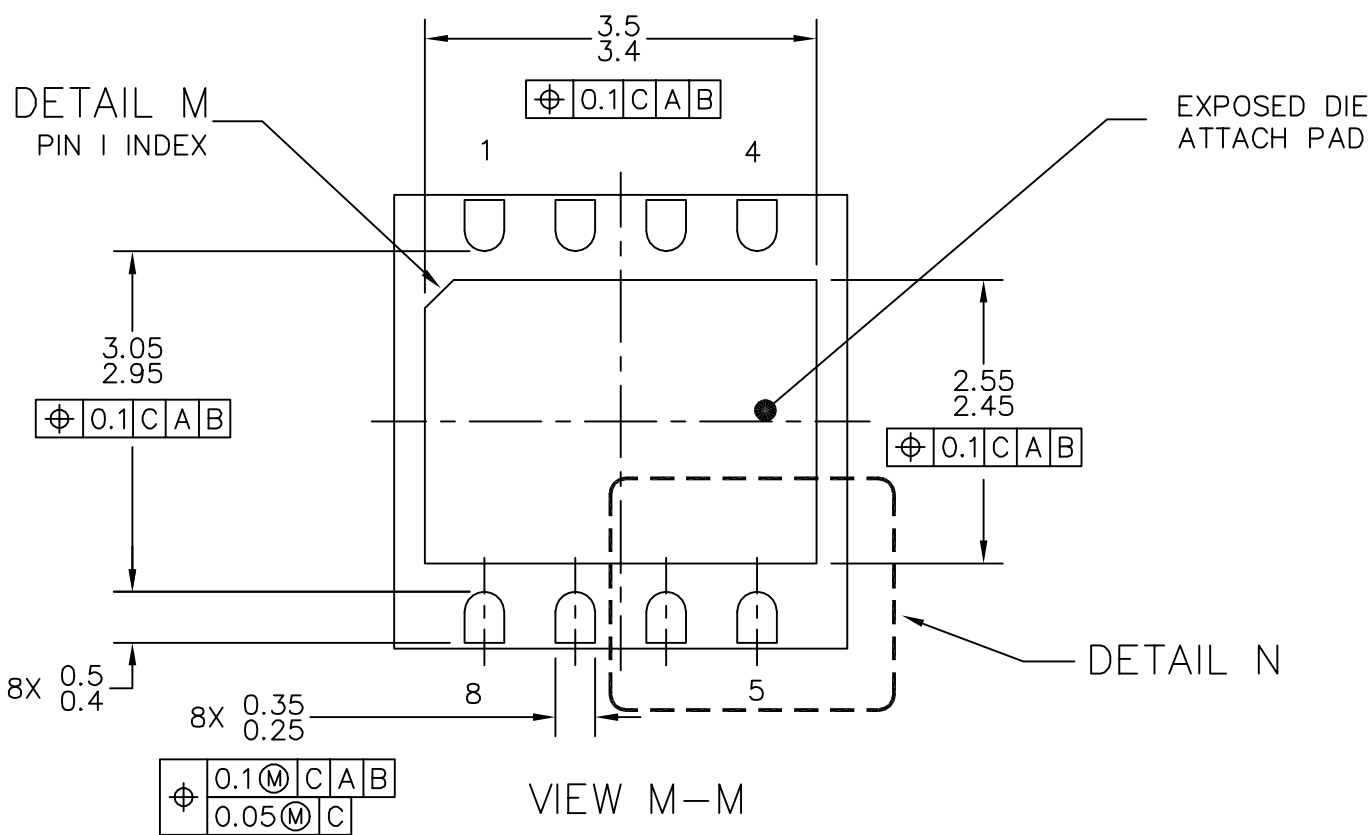
Device Number	Memory		Package		
	Flash	RAM	Type	Designator	Document No.
MC9S08QA4	4 KB	256 bytes	8 DFN 8 PDIP	FQ PA	98ARL10557D 98ASB42420B
MC9S08QA2	2 KB	160 bytes	8 NB SOIC	DN	98ASB42564B



## 5 Mechanical Drawings

The following pages contain mechanical specifications for MC9S08QA4 series package options.


- 8-pin DFN (plastic dual in-line pin)
- 8-pin NB SOIC (narrow body small outline integrated circuit)
- 8-pin PDIP (plastic dual in-line pin)



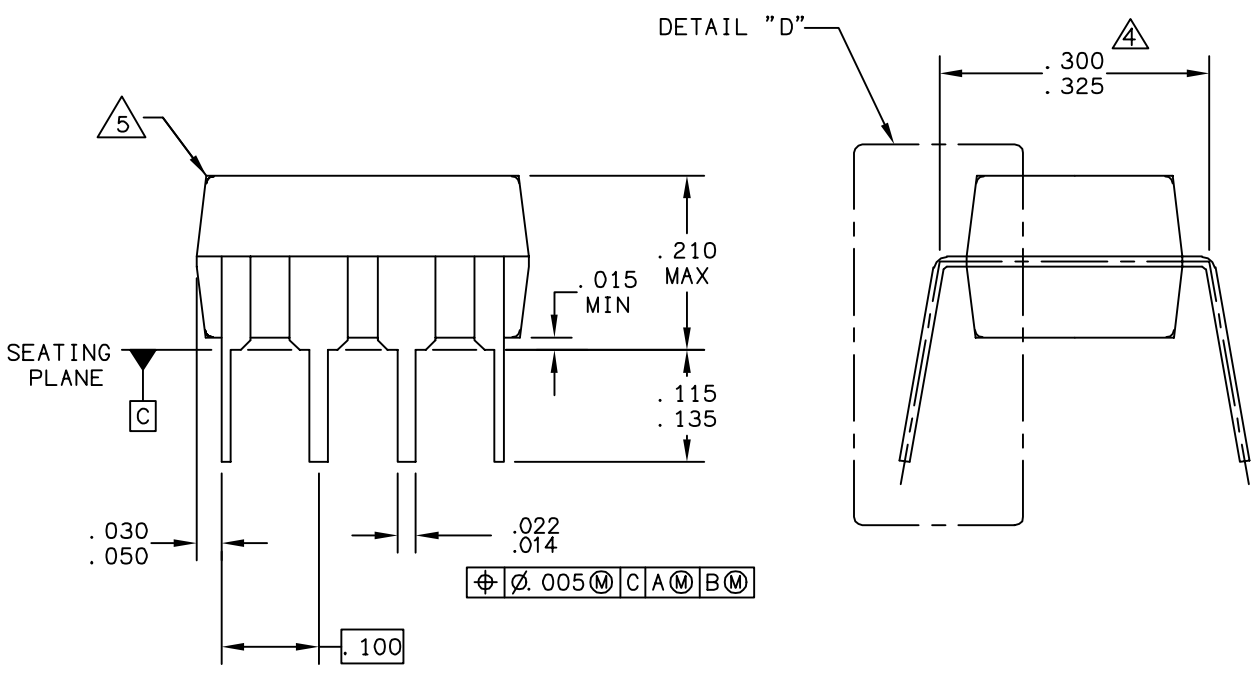
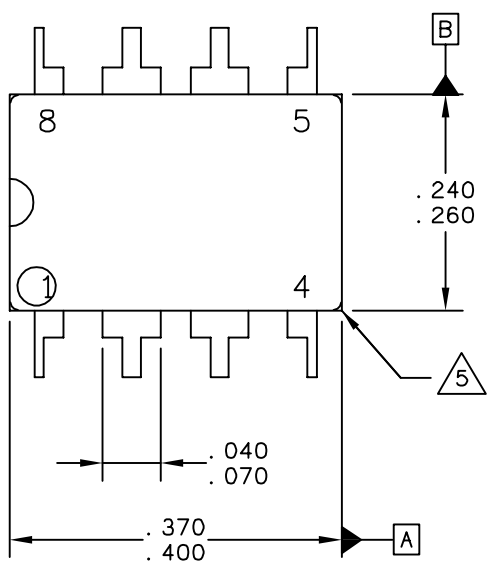
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	<b>MECHANICAL OUTLINE</b>	PRINT VERSION NOT TO SCALE	
TITLE: THERMALLY ENHANCED DUAL FLAT NO LEAD PACKAGE (DFN) 8 TERMINAL, 0.8 PITCH (4 X 4 X 1)	DOCUMENT NO: 98ARL10557D	REV: B	
	CASE NUMBER: 1452-02	28 DEC 2005	
	STANDARD: NON-JEDEC		



NOTES:

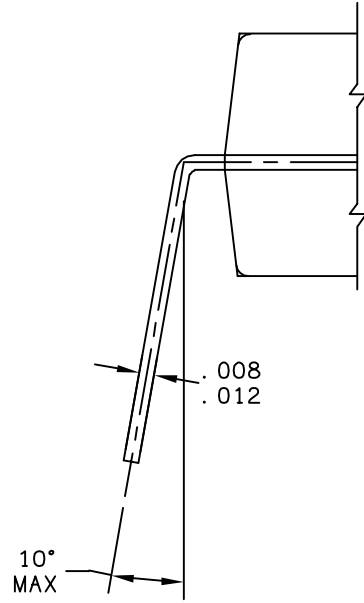
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HP-VDFDP-N.
4.  COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.
5. MIN. METAL GAP SHOULD BE 0.2MM.

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TITLE:THERMALLY ENHANCED DUAL FLAT NO LEAD PACKAGE (DFN) 8 TERMINAL, 0.8 PITCH(4 X 4 X 1)	DOCUMENT NO: 98ARL10557D	REV: B	
	CASE NUMBER: 1452-02	28 DEC 2005	
	STANDARD: NON-JEDEC		



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TITLE:  <div style="text-align: center; font-size: 1.2em;">8 LD PDIP</div>	DOCUMENT NO: 98ASB42420B	REV: N	
	CASE NUMBER: 626-06	19 MAY 2005	
	STANDARD: NON-JEDEC		





DETAIL "D"

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TITLE:  8 LD PDIP	DOCUMENT NO: 98ASB42420B	REV: N	
	CASE NUMBER: 626-06	19 MAY 2005	
	STANDARD: NON-JEDEC		



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
2. ALL DIMENSIONS ARE IN INCHES.
3. 626-03 TO 626-06 OBSOLETE. NEW STANDARD 626-07.
4. DIMENSION TO CENTER OF LEAD WHEN FORMED PARALLEL.
5. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CONERS).

STYLE 1:

PIN	1.	AC IN	5.	GROUND
	2.	DC + IN	6.	OUTPUT
	3.	DC - IN	7.	AUXILIARY
	4.	AC IN	8.	VCC

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TITLE:  8 LD PDIP		DOCUMENT NO: 98ASB42420B		REV: N	
		CASE NUMBER: 626-06		19 MAY 2005	
		STANDARD: NON-JEDEC			



STYLE 1:

- PIN 1. EMITTER
- 2. COLLECTOR
- 3. COLLECTOR
- 4. EMITTER
- 5. EMITTER
- 6. BASE
- 7. BASE
- 8. EMITTER

STYLE 2:

- PIN 1. COLLECTOR, DIE #1
- 2. COLLECTOR, #1
- 3. COLLECTOR, #2
- 4. COLLECTOR, #2
- 5. BASE, #2
- 6. EMITTER, #2
- 7. BASE, #1
- 8. EMITTER, #1

STYLE 3:

- PIN 1. DRAIN, DIE #1
- 2. DRAIN, #1
- 3. DRAIN, #2
- 4. DRAIN, #2
- 5. GATE, #2
- 6. SOURCE, #2
- 7. GATE, #1
- 8. SOURCE, #1

STYLE 4:

- PIN 1. ANODE
- 2. ANODE
- 3. ANODE
- 4. ANODE
- 5. ANODE
- 6. ANODE
- 7. ANODE
- 8. COMMON CATHODE

STYLE 5:

- PIN 1. DRAIN
- 2. DRAIN
- 3. DRAIN
- 4. DRAIN
- 5. GATE
- 6. GATE
- 7. SOURCE
- 8. SOURCE

STYLE 6:

- PIN 1. SOURCE
- 2. DRAIN
- 3. DRAIN
- 4. SOURCE
- 5. SOURCE
- 6. GATE
- 7. GATE
- 8. SOURCE

STYLE 7:

- PIN 1. INPUT
- 2. EXTERNAL BYPASS
- 3. THIRD STAGE SOURCE
- 4. GROUND
- 5. DRAIN
- 6. GATE 3
- 7. SECOND STAGE Vd
- 8. FIRST STAGE Vd

STYLE 8:

- PIN 1. COLLECTOR, DIE #1
- 2. BASE, #1
- 3. BASE, #2
- 4. COLLECTOR, #2
- 5. COLLECTOR, #2
- 6. EMITTER, #2
- 7. EMITTER, #1
- 8. COLLECTOR, #1

STYLE 9:

- PIN 1. EMITTER, COMMON
- 2. COLLECTOR, DIE #1
- 3. COLLECTOR, DIE #2
- 4. EMITTER, COMMON
- 5. EMITTER, COMMON
- 6. BASE, DIE #2
- 7. BASE, DIE #1
- 8. EMITTER, COMMON

STYLE 10:

- PIN 1. GROUND
- 2. BIAS 1
- 3. OUTPUT
- 4. GROUND
- 5. GROUND
- 6. BIAS 2
- 7. INPUT
- 8. GROUND

STYLE 11:

- PIN 1. SOURCE 1
- 2. GATE 1
- 3. SOURCE 2
- 4. GATE 2
- 5. DRAIN 2
- 6. DRAIN 2
- 7. DRAIN 1
- 8. DRAIN 1

STYLE 12:

- PIN 1. SOURCE
- 2. SOURCE
- 3. SOURCE
- 4. GATE
- 5. DRAIN
- 6. DRAIN
- 7. DRAIN
- 8. DRAIN

STYLE 13:

- PIN 1. N. C.
- 2. SOURCE
- 3. SOURCE
- 4. GATE
- 5. DRAIN
- 6. DRAIN
- 7. DRAIN
- 8. DRAIN

STYLE 14:

- PIN 1. N-SOURCE
- 2. N-GATE
- 3. P-SOURCE
- 4. P-GATE
- 5. P-DRAIN
- 6. P-DRAIN
- 7. N-DRAIN
- 8. N-DRAIN

STYLE 15:

- PIN 1. ANODE 1
- 2. ANODE 1
- 3. ANODE 1
- 4. ANODE 1
- 5. CATHODE, COMMON
- 6. CATHODE, COMMON
- 7. CATHODE, COMMON
- 8. CATHODE, COMMON

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TITLE:  8LD SOIC NARROW BODY		DOCUMENT NO: 98ASB42564B		REV: U	
		CASE NUMBER: 751-07		07 APR 2005	
		STANDARD: JEDEC MS-012AA			



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