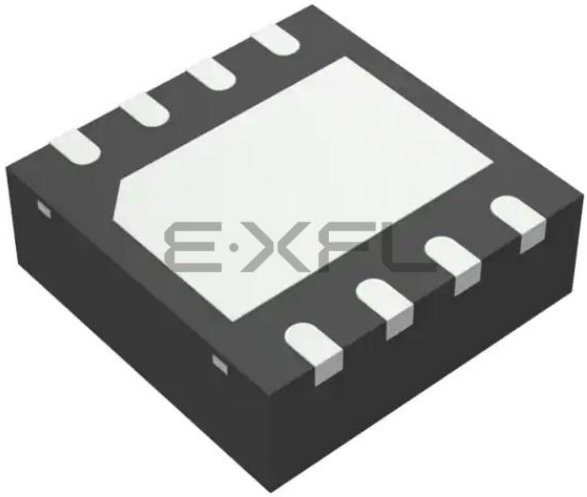

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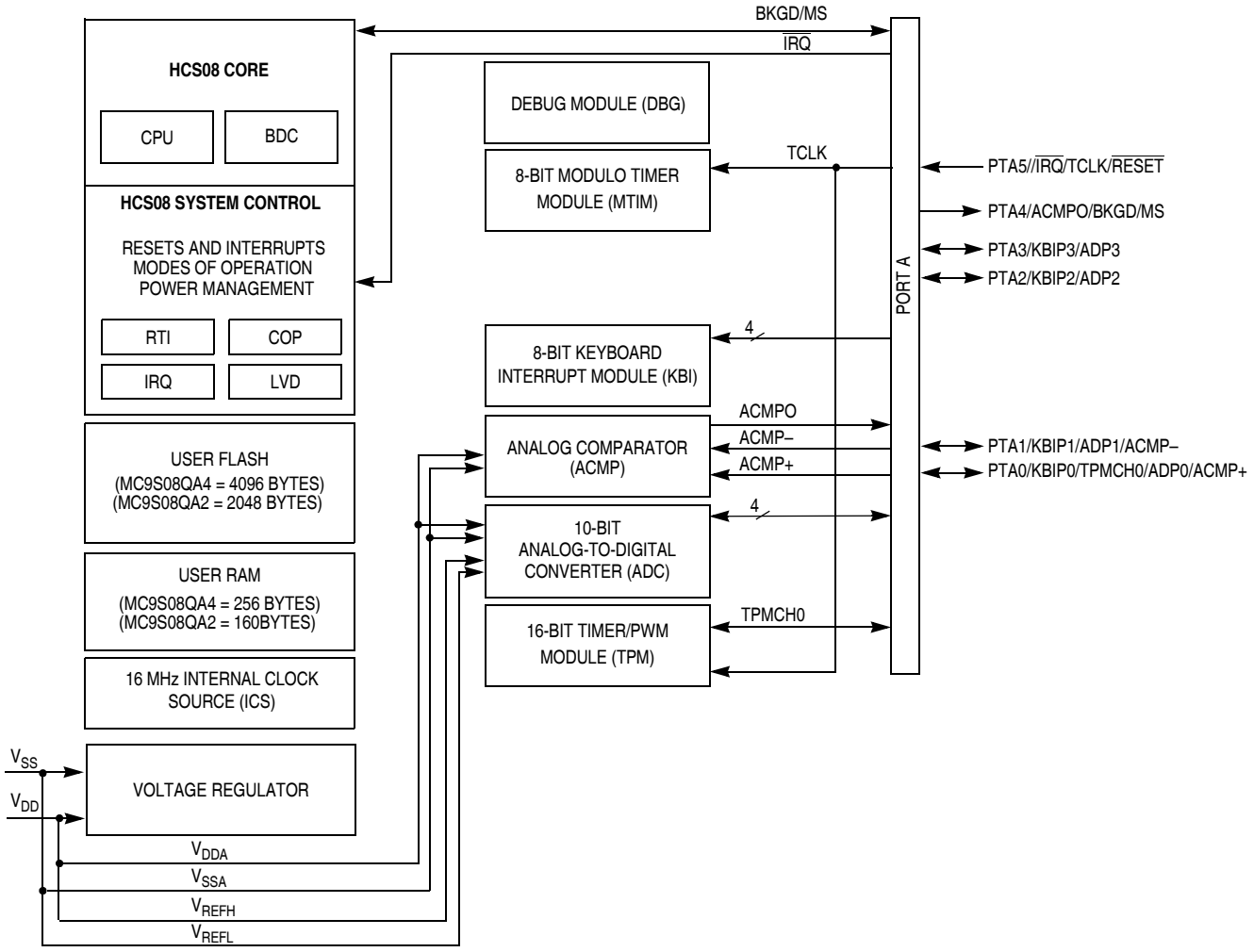
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	4
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN-EP (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08qa4cfqer

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of the MC9S08QA4 MCU.



NOTES:

1. Port pins are software configurable with pullup device if input port.
2. Port pins are software configurable for output drive strength.
3. Port pins are software configurable for output slew rate control.
4. $\overline{IRQ}$ contains a software configurable (IRQPDD) pullup device if PTA5 enabled as $\overline{IRQ}$ pin function (IRQPE = 1).
5. $\overline{RESET}$ contains integrated pullup device if PTA5 enabled as reset pin function (RSTPE = 1).
6. PTA4 contains integrated pullup device if BKGD enabled (BKGDPE = 1).
7. When pin functions as KBI (KBIPEn = 1) and associated pin is configured to enable the pullup device, KBEDGn can be used to reconfigure the pullup as a pulldown device.

Figure 1. MC9S08QA4 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments in the packages available for the MC9S08QA4 series.

Table 1. Pin Sharing Priority

PIN	Priority (Lowest → Highest)				
8-Pin	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	PTA5[1]	$\overline{\text{IRQ}}$	TCLK		$\overline{\text{RESET}}$
2	PTA4		ACMPO	BKGD	MS
3					V_{DD}
4					V_{SS}
5	PTA3	KBIP3	ADP3		
6	PTA2	KBIP2	ADP2		
7	PTA1	KBIP1		ADP1[2]	ACMP–[2]
8	PTA0	KBIP0	TPMCH0	ADP0[2]	ACMP+[2]

1 Pin does not contain a clamp diode to V_{DD} and must not be driven above V_{DD}. The voltage measured on the internally pulled-up $\overline{\text{RESET}}$ pin will not be pulled to V_{DD}. The internal gates connected to this pin are pulled to V_{DD}.

2 If ACMP and ADC are both enabled, both will have access to the pin.

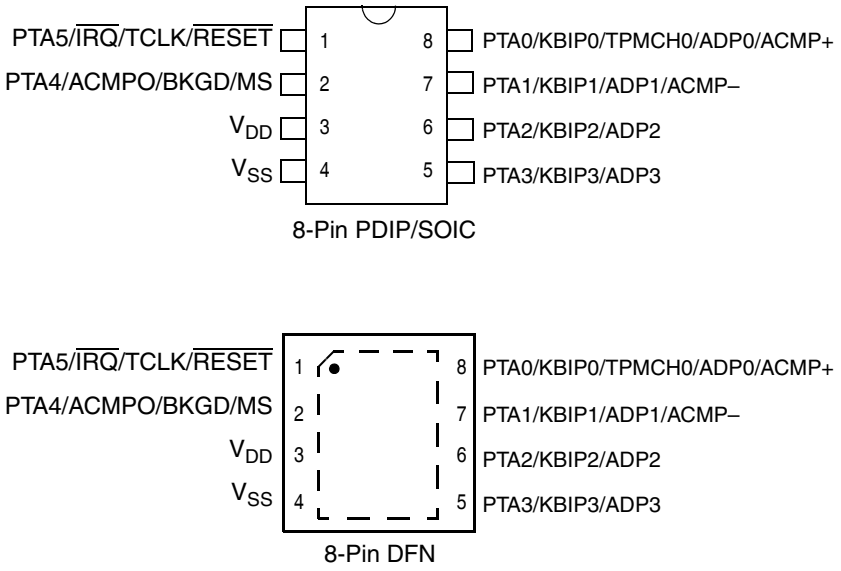


Figure 2. MC9S08QA4 Series in 8-Pin Packages

Table 3. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Thermal resistance Single-layer board			
8-pin PDIP	θ_{JA}	113	°C/W
8-pin NB SOIC		150	
8-pin DFN		179	
Thermal resistance Four-layer board			
8-pin PDIP	θ_{JA}	72	°C/W
8-pin NB SOIC		87	
8-pin DFN		41	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

- T_A = Ambient temperature, °C
- θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
- $P_D = P_{int} + P_{I/O}$
- $P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
- $P_{I/O}$ = Power dissipation on input and output pins — user-determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.4 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

Table 6. DC Characteristics (Temperature Range = –40 to 85°C Ambient) (continued)

Parameter	Symbol	Min	Typical	Max	Unit
(V_{DD} rising)		2.16	2.19	2.27	
Power on reset (POR) re-arm voltage	V_{por}	—	1.4	—	V
Bandgap voltage reference	V_{BG}	1.18	1.20	1.21	V
Input high voltage (V_{DD} > 2.3 V) (all digital inputs)	V_{IH}	0.70 × V_{DD}	—	—	V
Input high voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)		0.85 × V_{DD}	—	—	
Input low voltage (V_{DD} > 2.3 V) (all digital inputs)	V_{IL}	—	—	0.35 × V_{DD}	V
Input low voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)		—	—	0.30 × V_{DD}	
Input hysteresis (all digital inputs)	V_{hys}	0.06 × V_{DD}	—	—	V
Input leakage current (per pin) V_{In} = V_{DD} or V_{SS}, all input-only pins	$\lvert I_{In}\rvert$	—	0.025	1.0	µA
High impedance (off-state) leakage current (per pin) V_{In} = V_{DD} or V_{SS}, all input/output	$\lvert I_{OZ}\rvert$	—	0.025	1.0	µA
Internal pullup resistors[3,4]	R_{PU}	17.5	—	52.5	kΩ
Internal pulldown resistor (KBI)	R_{PD}	17.5	—	52.5	kΩ
Output high voltage — low drive (PTxDSn = 0) I_{OH} = –2 mA (V_{DD} ≥ 1.8 V)	V_{OH}	V_{DD} – 0.5	—	—	V
Output high voltage — high drive (PTxDSn = 1) I_{OH} = –10 mA (V_{DD} ≥ 2.7 V) I_{OH} = –6 mA (V_{DD} ≥ 2.3 V) I_{OH} = –3 mA (V_{DD} ≥ 1.8 V)		V_{DD} – 0.5	— — —	— — —	
Maximum total I_{OH} for all port pins	$\lvert I_{OHT}\rvert$	—	—	60	mA
Output low voltage — low drive (PTxDSn = 0) I_{OL} = 2.0 mA (V_{DD} ≥ 1.8 V)	V_{OL}	—	—	0.5	V
Output low voltage — high drive (PTxDSn = 1) I_{OL} = 10.0 mA (V_{DD} ≥ 2.7 V) I_{OL} = 6 mA (V_{DD} ≥ 2.3 V) I_{OL} = 3 mA (V_{DD} ≥ 1.8 V)		— — —	— — —	0.5 0.5 0.5	
Maximum total I_{OL} for all port pins	I_{OLT}	—	—	60	mA
DC injection current [2, 5, 6, 7] V_{In} < V_{SS}, V_{In} > V_{DD} Single pin limit Total MCU limit, includes sum of all stressed pins	I_{IC}	 –0.2 –5	 — —	 0.2 5	 mA mA
Input capacitance (all non-supply pins)	C_{In}	—	—	7	pF

1 RAM will retain data down to POR voltage. RAM data not guaranteed to be valid following a POR.

2 This parameter is characterized and not tested on each device.

3 Measurement condition for pull resistors: V_{In} = V_{SS} for pullup and V_{In} = V_{DD} for pulldown.

4 PTA5/$\overline{\text{IRQ}}$/TCLK/$\overline{\text{RESET}}$ pullup resistor may not pull up to the specified minimum V_{IH}. However, all ports are functionally tested to guarantee that a logic 1 will be read on any port input when the pullup is enabled and no DC load is present on the pin.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

6 Input must be current-limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

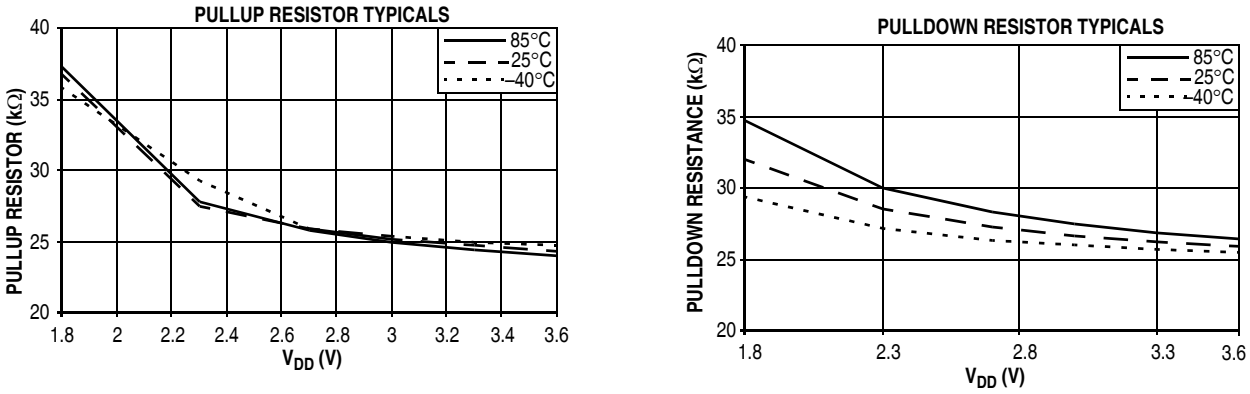


Figure 3. Pullup and Pulldown Typical Resistor Values (V_{DD} = 3.0 V)

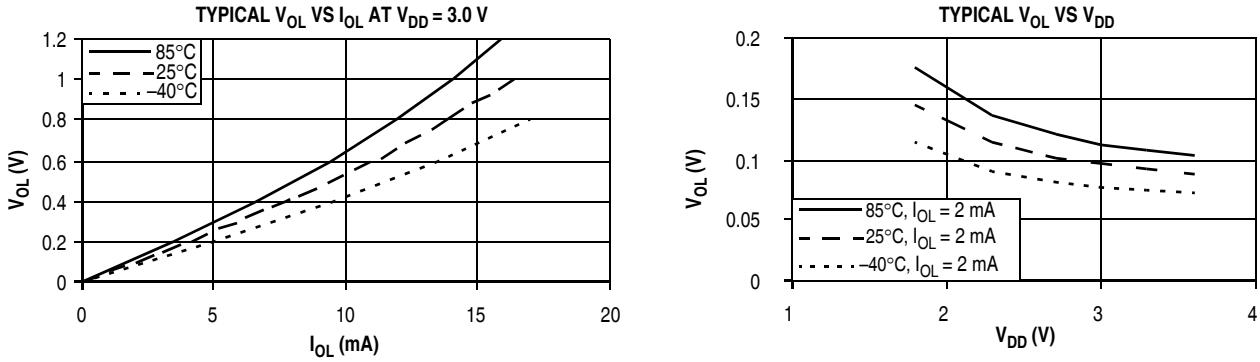


Figure 4. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)

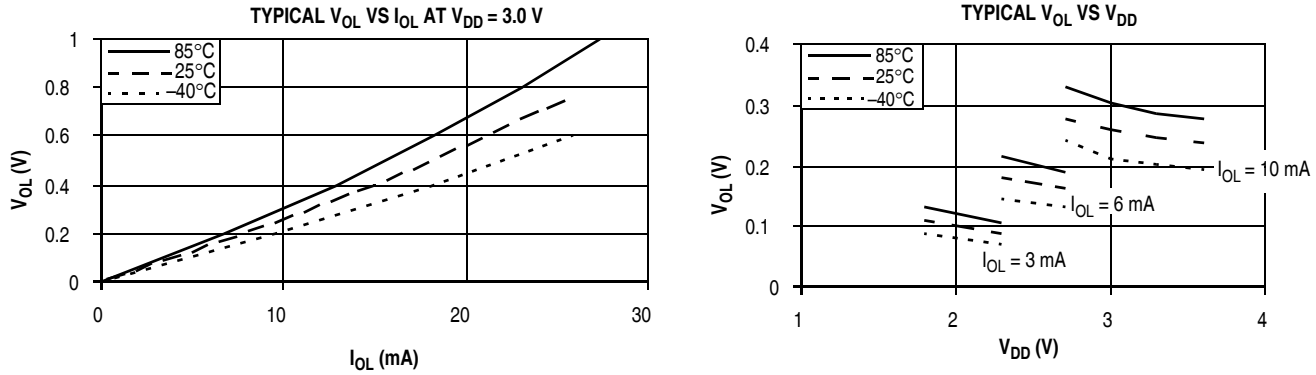


Figure 5. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)

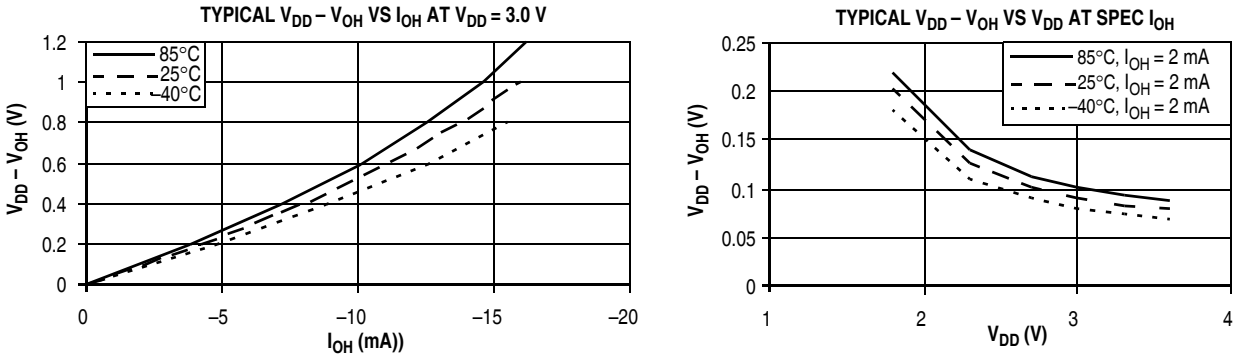


Figure 6. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

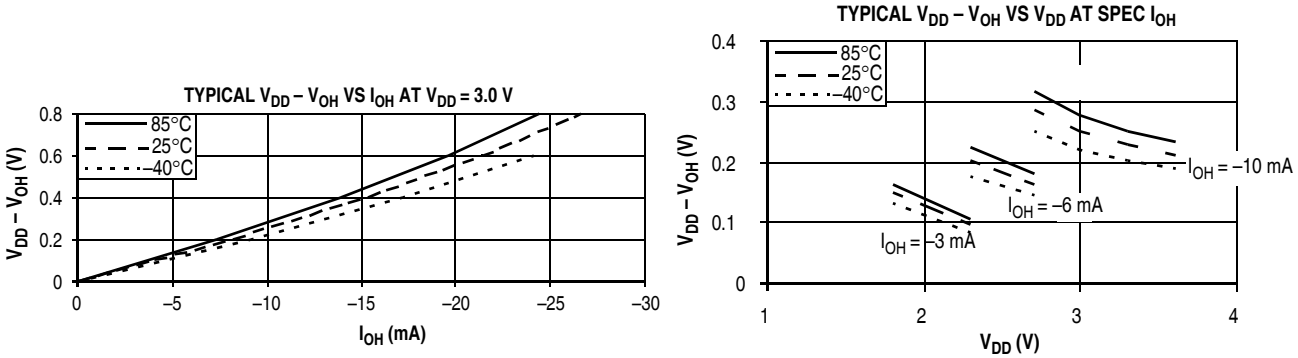


Figure 7. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

3.6 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 7. Supply Current Characteristics

Parameter	Symbol	V_{DD} (V)[1]	Typical[2]	Max	T (°C)
Run supply current[3] measured in FBE mode at f_{Bus} = 8 MHz	RI_{DD}	3	3.5 mA	5 mA	85
		2	2.6 mA	—	85
Run supply current[3] measured in FBE mode at f_{Bus} = 1 MHz	RI_{DD}	3	490 µA	1 mA	85
		2	370 µA	—	85
Wait mode supply current[4] measured in FBE at 8 MHz	WI_{DD}	3	1 mA	1.5 mA	85
Stop1 mode supply current	$S1I_{DD}$	3	475 nA	1.2 µA	85
		2	470 nA	—	85
Stop2 mode supply current	$S2I_{DD}$	3	600 nA	2 µA	85
		2	550 nA	—	85
Stop3 mode supply current	$S3I_{DD}$	3	750 nA	6 µA	85
		2	680 nA	—	85
RTI adder to stop1, stop2, or stop3[4]	—	3	300 nA	—	85
		2	300 nA	—	85
LVD adder to stop3 (LVDE = LVDSE = 1)[4]	—	3	70 µA	—	85
		2	60 µA	—	85

1 3 V values are 100% tested; 2 V values are characterized but not tested.
2 Typicals are measured at 25 °C.
3 Does not include any DC loads on port pins.
4 Most customers are expected to find that auto-wakeup from a stop mode can be used instead of the higher current wait mode.

3.7 Internal Clock Source (ICS) Characteristics

Table 8. ICS Specifications (Temperature Range = –40 to 85°C Ambient)

Characteristic	Symbol	Min	Typical[1]	Max	Unit
Internal reference start-up time	t_{IRST}	—	60	100	µs
Average internal reference frequency — untrimmed	f_{int_ut}	25	32.7	41.66	kHz
Average internal reference frequency — trimmed	f_{int_t}	31.25	—	39.06	kHz
DCO output frequency range — untrimmed	f_{dco_ut}	12.8	16.8	21.33	MHz
DCO output frequency range — trimmed	f_{dco_t}	16	—	20	MHz
Resolution of trimmed DCO output frequency at fixed voltage and temperature[2]	$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
Total deviation of DCO output from trimmed frequency[2] At 8 MHz over full voltage and temperature range At 8 MHz and 3.6 V from 0 to 70 °C	Δf_{dco_t}	—	–1.0 to 0.5 ±0.5	±2 ±1	$\%f_{dco}$
FLL acquisition time [2,3]	$t_{Acquire}$	—	—	1.5	ms
Long term jitter of DCO output clock (averaged over 2 ms interval)	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25 °C, or is typical recommended value.
2 This parameter is characterized and not tested on each device.
3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed.

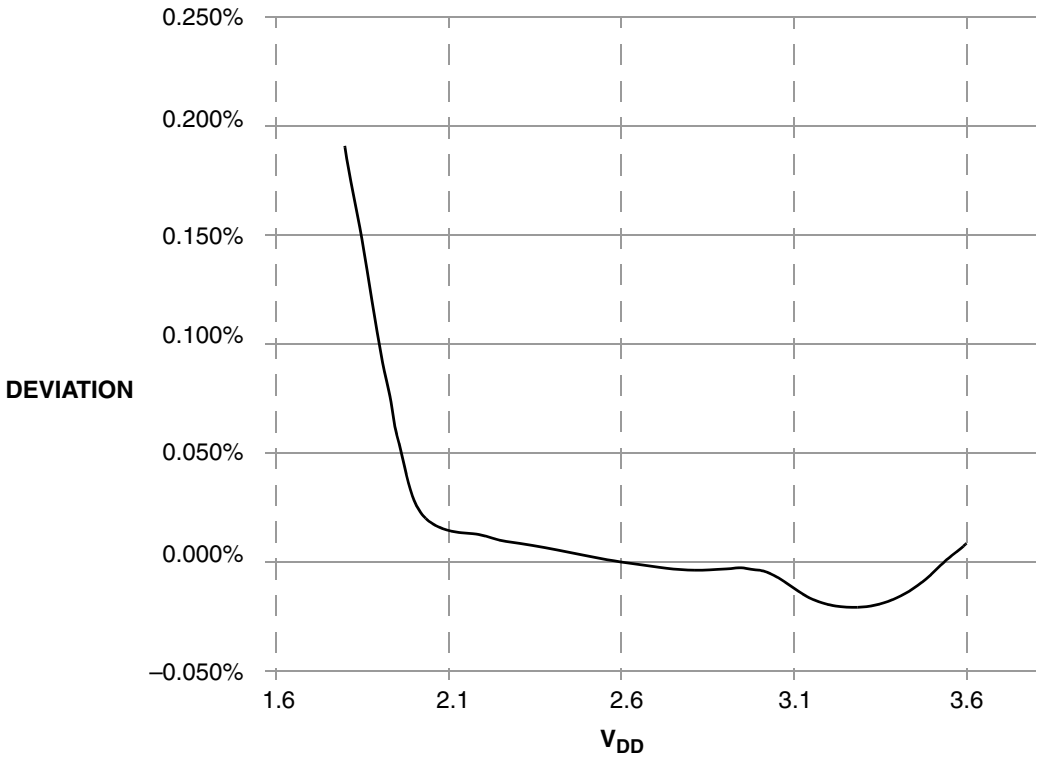


Figure 8. Deviation of DCO Output from Trimmed Frequency (8 MHz, 25 °C)

3.8 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.8.1 Control Timing

Table 9. Control Timing

Parameter	Symbol	Min	Typical[1]	Max	Unit
Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	0	—	10	MHz
Real-time interrupt internal oscillator period (see Table 9)	t_{RTI}	700	1000	1300	µs
External reset pulse width[2]	t_{extrst}	100	—	—	ns
$\overline{IRQ}$ pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}	 100 1.5 t_{cyc}	—	—	ns
KBIPx pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	 100 1.5 t_{cyc}	—	—	ns
Port rise and fall time (load = 50 pF)[4] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 3 30	 — —	ns
BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes[5]	t_{MSH}	100	—	—	µs

1 Data in Typical column was characterized at 3.0 V, 25°C.

2 This is the shortest pulse that is guaranteed to be recognized.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

5 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

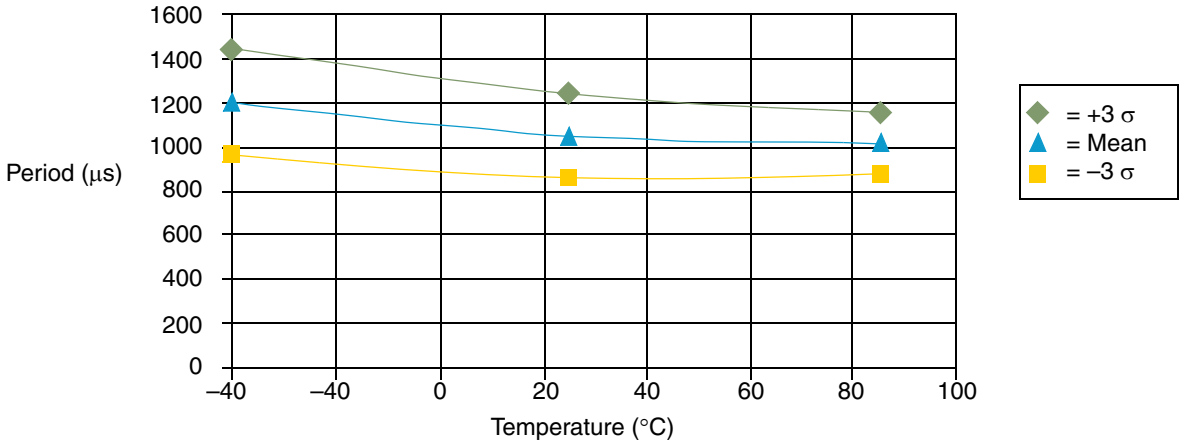


Figure 9. Typical RTI Clock Period vs. Temperature

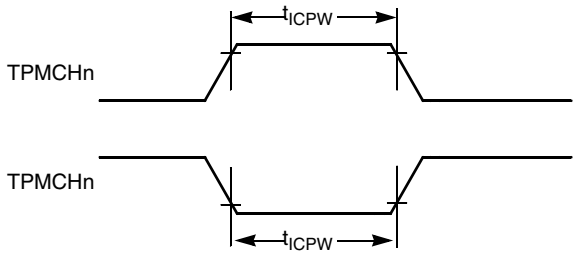


Figure 13. Timer Input Capture Pulse

3.9 Analog Comparator (ACMP) Electricals

Table 11. Analog Comparator Electrical Specifications

Characteristic	Symbol	Min	Typical	Max	Unit
Supply voltage	V_{DD}	1.80	—	3.60	V
Supply current (active)	I_{DDAC}	—	20	—	μA
Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
Analog input offset voltage	V_{AIO}	—	20	40	mV
Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
Analog input leakage current	I_{ALKG}	—	—	1.0	μA
Analog comparator initialization delay	t_{AINIT}	—	—	1.0	μs

3.10 ADC Characteristics

Table 12. 3 V 10-Bit ADC Operating Conditions

Characteristic	Conditions	Symbol	Min	Typical[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DD}	1.8	—	3.6	V	
Input voltage		V_{ADIN}	V_{SS}	—	V_{DD}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	5	7	kΩ	
Analog source resistance	10 bit mode f_{ADCK} > 4 MHz f_{ADCK} < 4 MHz	R_{AS}	 — —	 — —	 5 10	kΩ	External to MCU
	8 bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High Speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low Power (ADLPC=1)		0.4	—	4.0		

[1] Typical values assume V_{DD} = 3.0 V, Temp = 25°C, f_{ADCK} =1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

Table 13. 3 V 10-Bit ADC Characteristics (continued)

Characteristic	Conditions	Symbol	Min	Typical[1]	Max	Unit	Comment
Conversion time (including sample time)	Short sample (ADLSMP=0)	t_{ADC}	—	20	—	ADCK cycles	See MC9S08QA4 Series *Reference Manual* for conversion time variances
	Long sample (ADLSMP=1)		—	40	—		
Sample time	Short sample (ADLSMP=0)	t_{ADS}	—	3.5	—	ADCK cycles	
	Long sample (ADLSMP=1)		—	23.5	—		
Total unadjusted error	10-bit mode	E_{TUE}	—	±1.5	±3.5	LSB[2]	Includes quantization
	8-bit mode		—	±0.7	±1.5		
Differential non-linearity	10-bit mode	DNL	—	±0.5	±1.0	LSB[2]	Monotonicity and no missing codes guaranteed
	8-bit mode		—	±0.3	±0.5		
Integral non-linearity	10-bit mode	INL	—	±0.5	±1.0	LSB[2]	
	8-bit mode		—	±0.3	±0.5		
Zero-scale error	10-bit mode	E_{ZS}	—	±1.5	±2.1	LSB[2]	$V_{ADIN} = V_{SS}$
	8-bit mode		—	±0.5	±0.7		
Full-scale error	10-bit mode	E_{FS}	0	±1.0	±1.5	LSB[2]	$V_{ADIN} = V_{DD}$
	8-bit mode		0	±0.5	±0.5		
Quantization error	10-bit mode	E_Q	—	—	±0.5	LSB[2]	
	8-bit mode		—	—	±0.5		
Input leakage error	10-bit mode	E_{IL}	0	±0.2	±4	LSB[2]	Pad leakage[3] * R_{AS}
	8-bit mode		0	±0.1	±1.2		
Temp sensor slope	–40°C – 25°C	m	—	1.646	—	mV/°C	
	25°C – 85°C		—	1.769	—		
Temp sensor voltage	25°C	V_{TEMP25}	—	701.2	—	mV	

1 Typical values assume V_{DD} = 3.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Based on input pad leakage current. Refer to pad electricals.

3.11 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see *MC9S08QA4 Series Reference Manual*.

Table 14. Flash Characteristics

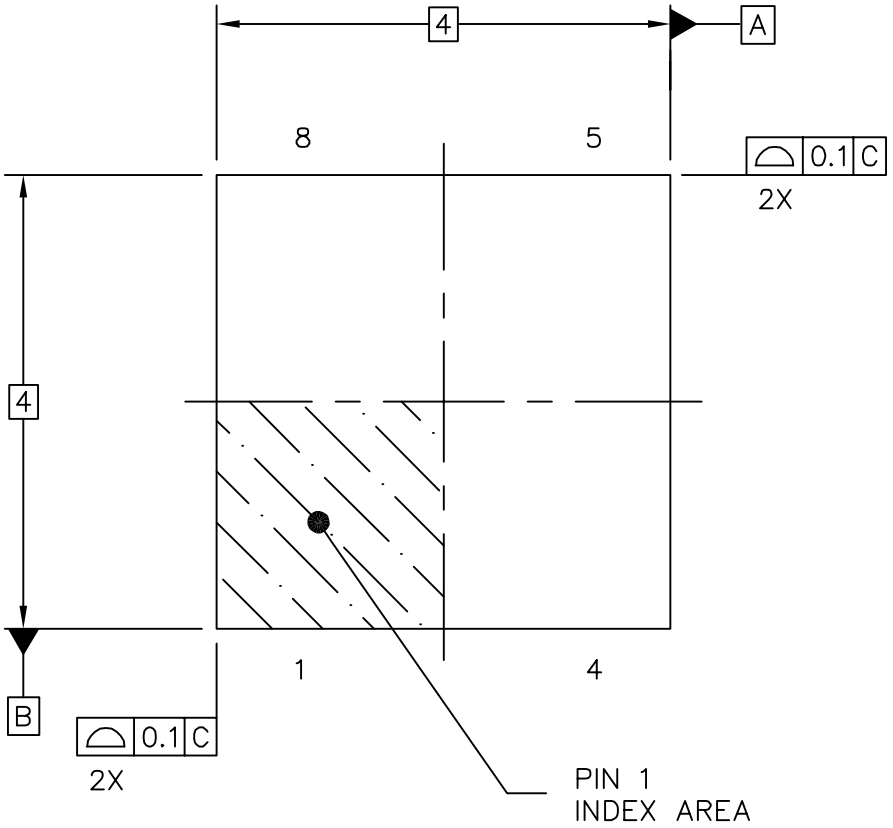
Characteristic	Symbol	Min	Typical	Max	Unit
Supply voltage for program/erase –40°C to 85°C	$V_{prog/erase}$	1.8	—	3.6	V
Supply voltage for read operation	V_{Read}	1.8	—	3.6	V
Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz
Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs
Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}
Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
Page erase time[2]	t_{Page}	4000			t_{Fcyc}
Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
Program/erase endurance[3] T_L to T_H = –40°C to + 85°C T = 25°C		10,000	— 100,000	— —	cycles
Data retention[4]	t_{D_ret}	15	100	—	years

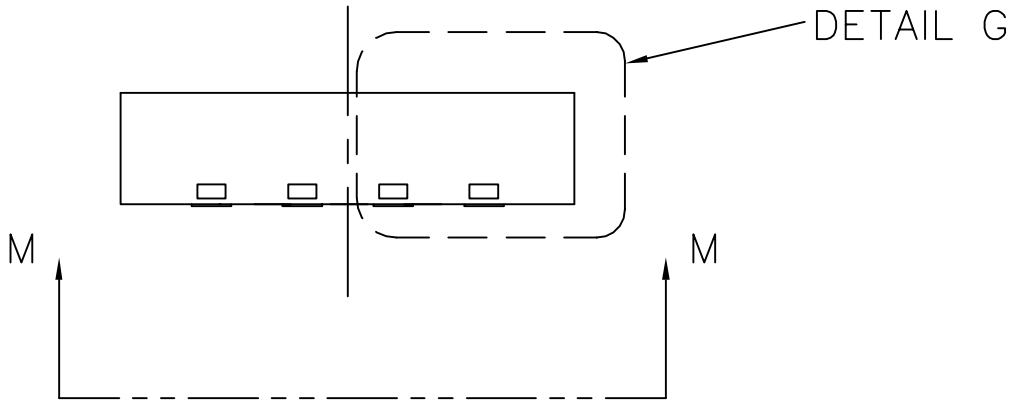
1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

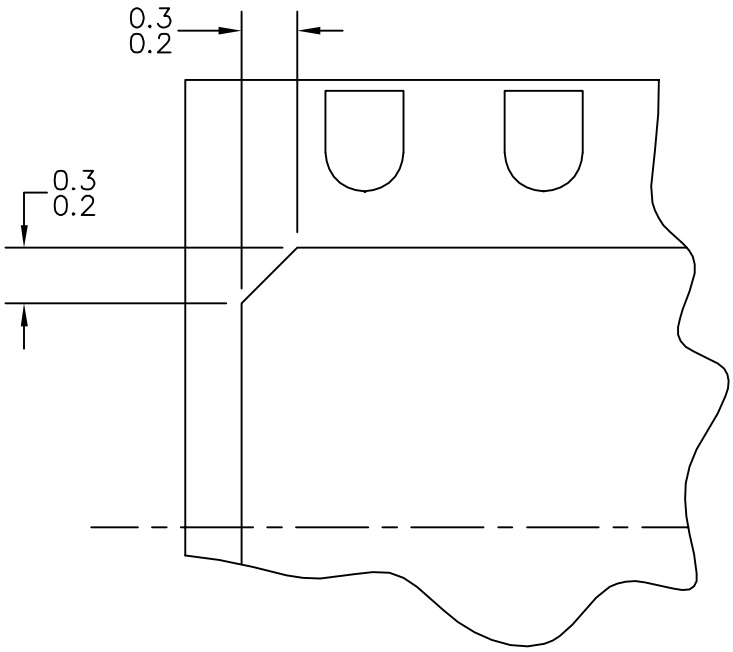
3 **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Motorola defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory.*

4 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory.*

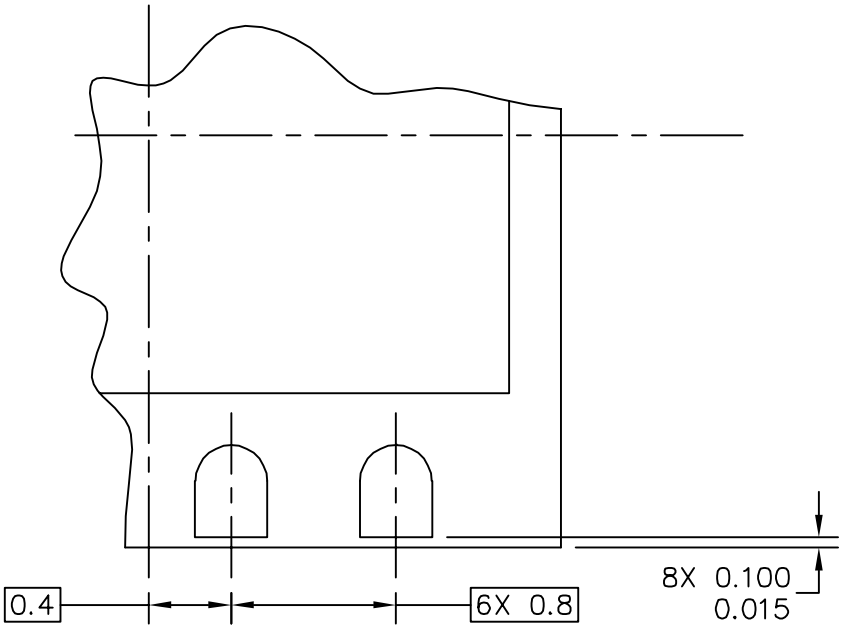




	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: THERMALLY ENHANCED DUAL FLAT NO LEAD PACKAGE (DFN) 8 TERMINAL, 0.8 PITCH (4 X 4 X 1)	DOCUMENT NO: 98ARL10557D	REV: B
	CASE NUMBER: 1452–02	28 DEC 2005
	STANDARD: NON–JEDEC	



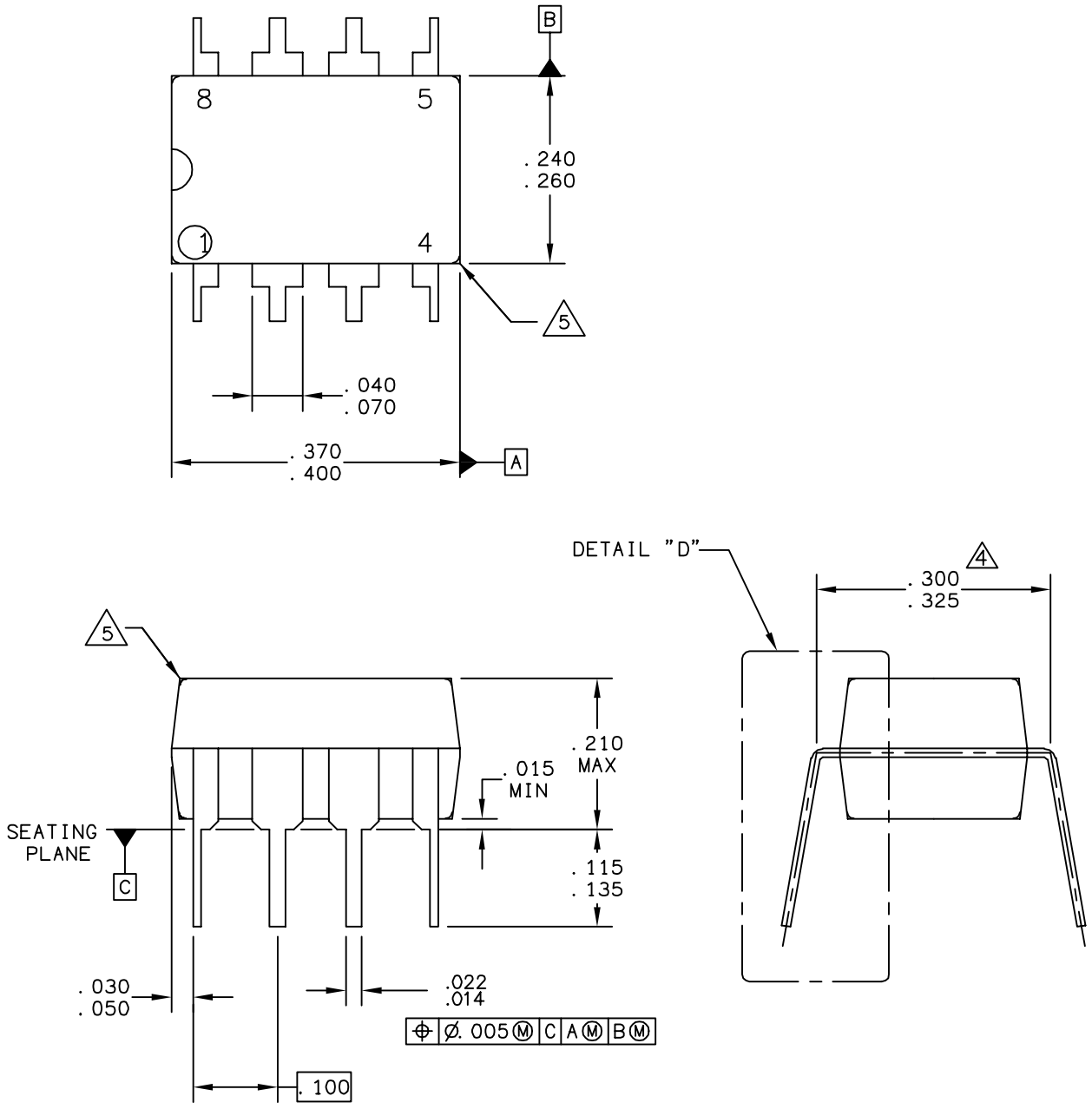
DETAIL M
BACKSIDE PIN 1 INDEX



DETAIL N

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: THERMALLY ENHANCED DUAL FLAT NO LEAD PACKAGE (DFN) 8 TERMINAL, 0.8 PITCH (4 X 4 X 1)	DOCUMENT NO: 98ARL10557D	REV: B
	CASE NUMBER: 1452-02	28 DEC 2005
	STANDARD: NON-JEDEC	



	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 8 LD PDIP	DOCUMENT NO: 98ASB42420B	REV: N
	CASE NUMBER: 626-06	19 MAY 2005
	STANDARD: NON-JEDEC	

NOTES:

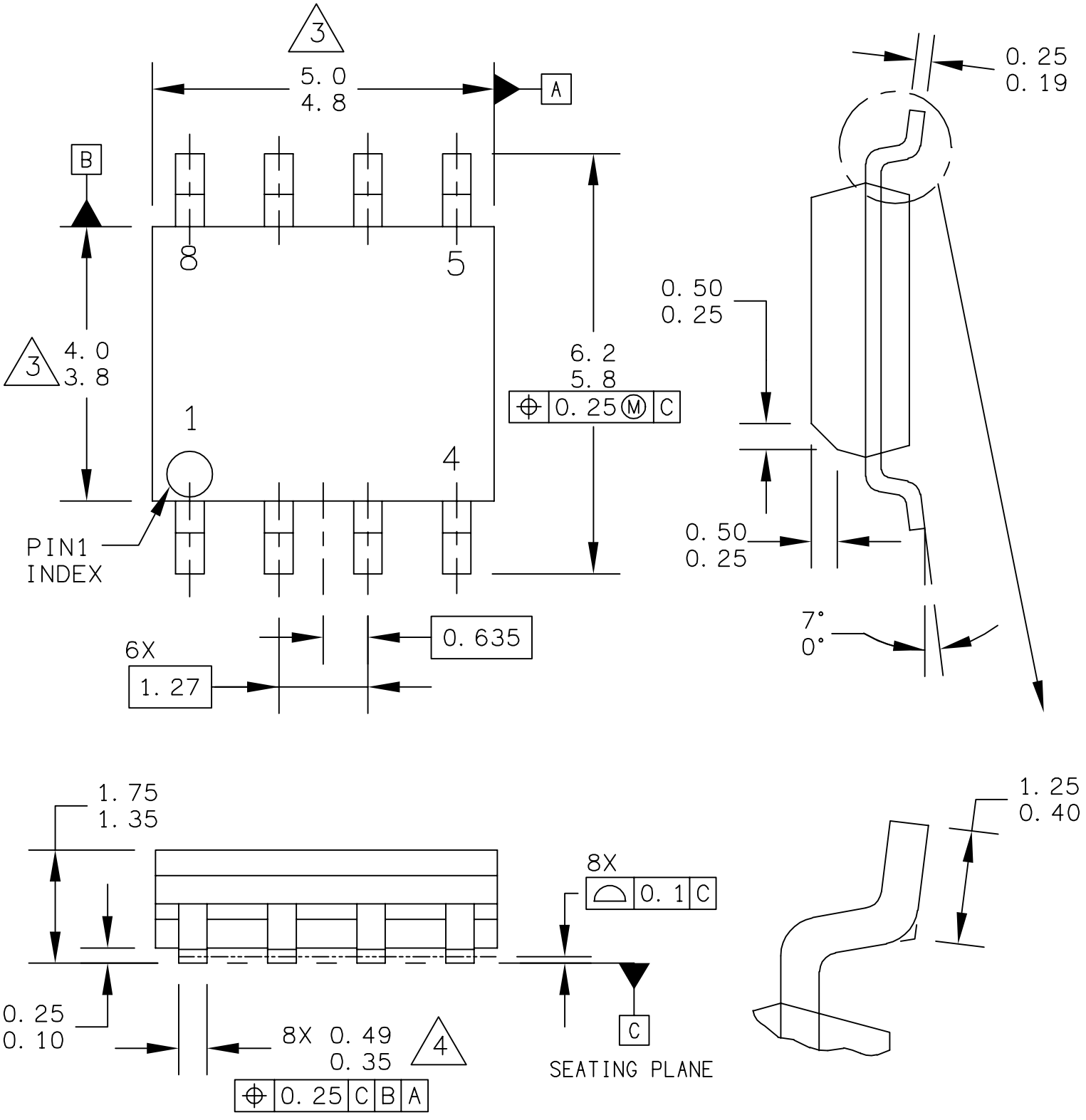
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN INCHES.
3. 626-03 TO 626-06 OBSOLETE. NEW STANDARD 626-07.
4. DIMENSION TO CENTER OF LEAD WHEN FORMED PARALLEL.
5. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CONERS).

STYLE 1:

PIN	1.	AC IN	5.	GROUND
	2.	DC + IN	6.	OUTPUT
	3.	DC – IN	7.	AUXILIARY
	4.	AC IN	8.	VCC

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42420B	REV: N
8 LD PDIP	CASE NUMBER: 626-06	19 MAY 2005
	STANDARD: NON-JEDEC	



MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42564B	REV: U
8LD SOIC NARROW BODY	CASE NUMBER: 751-07	07 APR 2005
	STANDARD: JEDEC MS-012AA	

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42564B	REV: U
8LD SOIC NARROW BODY	CASE NUMBER: 751-07	07 APR 2005
	STANDARD: JEDEC MS-012AA	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42564B	REV: U
8LD SOIC NARROW BODY	CASE NUMBER: 751–07	07 APR 2005
	STANDARD: JEDEC MS–012AA	