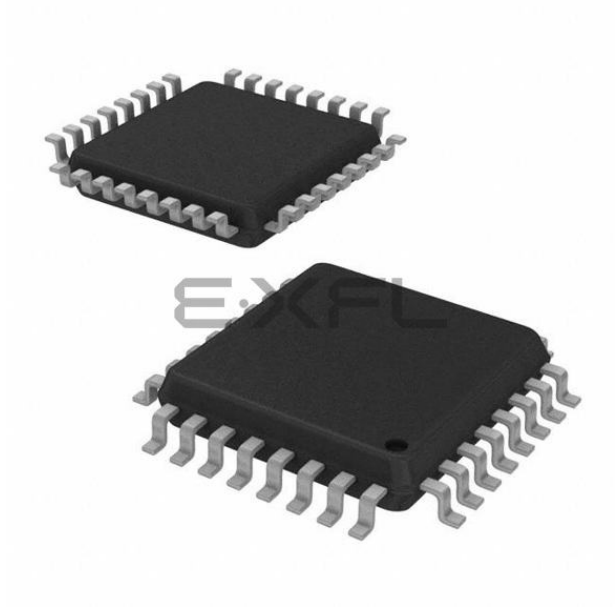

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	LINbusSCI
Peripherals	LVD, Motor Control PWM, POR, PWM, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7fmc1k2tce

Table 3. Hardware register map (continued)

Address	Block	Register label	Register name	Reset status	Remarks
0050h	MTC (page 0)	MTIM	Timer counter high register	00h	R/W
0051h		MTIML	Timer counter low register	00h	R/W
0052h		MZPRV	Capture Z_{n-1} register	00h	R/W
0053h		MZREG	Capture Z_n register	00h	R/W
0054h		MCOMP	Compare C_{n+1} register	00h	R/W
0055h		MDREG	Demagnetization register	00h	R/W
0056h		MWGHT	A_n weight register	00h	R/W
0057h		MPRSR	Prescaler and sampling register	00h	R/W
0058h		MIMR	Interrupt mask register	00h	R/W
0059h		MISR	Interrupt status register	00h	R/W
005Ah		MCRA	Control register A	00h	R/W
005Bh		MCRB	Control register B	00h	R/W
005Ch		MCRC	Control register C	00h	R/W
005Dh		MPHST	Phase state register	00h	R/W
005Eh		MDFR	D event filter register	0Fh	R/W
005Fh		MCFR	Current feedback filter register	00h	R/W
0060h		MREF	Reference register	00h	R/W
0061h		MPCR	PWM control register	00h	R/W
0062h		MREP	Repetition counter register	00h	R/W
0063h		MCPWH	Compare phase W preload register high	00h	R/W
0064h		MCPWL	Compare phase W preload register low	00h	R/W
0065h		MCPVH	Compare phase V preload register high	00h	R/W
0066h		MCPVL	Compare phase V preload register low	00h	R/W
0067h		MCPUH	Compare phase U preload register high	00h	R/W
0068h		MCPUL	Compare phase U preload register low	00h	R/W
0069h		MCP0H	Compare phase 0 preload register high	0Fh	R/W
006Ah		MCP0L	Compare phase 0 preload register low	FFh	R/W
0050h	MTC (page 1)	MDTG	deadtime generator enable	FFh	see MTC description
0051h		MPOL	Polarity register	3Fh	
0052h		MPWME	PWM register	00h	
0053h		MCONF	Configuration register	02h	
0054h		MPAR	Parity register	00h	
0055h		MZRF	Z event filter register	0Fh	
0056h		MSCR	Sampling clock register	00h	
0057h to 006Ah		Reserved area (4 bytes)			
006Bh	DM	DMCR	Debug control register	00h	R/W
006Ch		DMSR	Debug status register	10h	Read only
006Dh		DMBK1H	Debug Breakpoint 1 MSB Register	FFh	R/W
006Eh		DMBK1L	Debug Breakpoint 1 LSB Register	FFh	R/W
006Fh		DMBK2H	Debug Breakpoint 2 MSB Register	FFh	R/W
0070h		DMBK2L	Debug Breakpoint 2 LSB Register	FFh	R/W

6.5.2 Auxiliary voltage detector (AVD)

The voltage detector function (AVD) is based on an analog comparison between a $V_{IT-(AVD)}$ and $V_{IT+(AVD)}$ reference value and the V_{DD} main supply. The V_{IT-} reference value for falling voltage is lower than the V_{IT+} reference value for rising voltage in order to avoid parasitic detection (hysteresis).

The output of the AVD comparator is directly readable by the application software through a real time status bit (AVDF) in the SICSR register. This bit is read only.

Caution: The AVD function is active only if the LVD is enabled through the option byte (see *Section 14.1 on page 356*).

Monitoring the V_{DD} main supply

If the AVD interrupt is enabled, an interrupt is generated when the voltage crosses the $V_{IT+(AVD)}$ or $V_{IT-(AVD)}$ threshold (AVDF bit toggles).

In the case of a drop in voltage, the AVD interrupt acts as an early warning, allowing software to shut down safely before the LVD resets the microcontroller. See *Figure 14*.

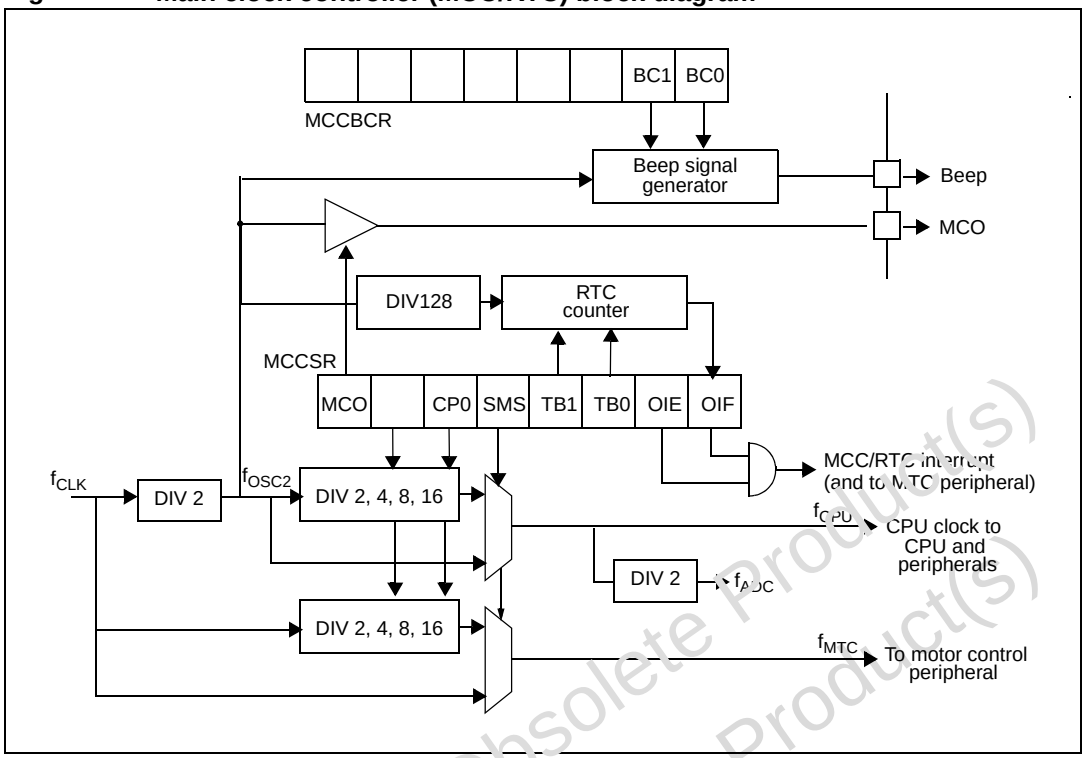
The interrupt on the rising edge is used to inform the application that the V_{DD} warning state is over.

If the voltage rise time t_{rv} is less than 256 or 4096 CPU cycles (depending on the reset delay selected by option byte), no AVD interrupt is generated when $V_{IT+(AVD)}$ is reached.

If t_{rv} is greater than 256 or 4096 cycles then:

- If the AVD interrupt is enabled before the $V_{IT+(AVD)}$ threshold is reached, then two AVD interrupts are received: the first when the AVDIE bit is set, and the second when the threshold is reached.
- If the AVD interrupt is enabled after the $V_{IT+(AVD)}$ threshold is reached then only one AVD interrupt occurs.

Figure 15. Main clock controller (MCC/RTC) block diagram



6.6.5 Low power modes

Table 11. Effect of low power modes on MCC/RTC

Mode	Description
Wait	No effect on MCC/RTC peripheral. MCC/RTC interrupt cause the device to exit from Wait mode.
Active Halt	No effect on MCC/RTC counter (OIE bit is set), the registers are frozen. MCC/RTC interrupt cause the device to exit from Active Halt mode.
Halt	MCC/RTC counter and registers are frozen. MCC/RTC operation resumes when the MCU is woken up by an interrupt with 'exit from HALT' capability.

Caution: If the I1_x and I0_x bits are modified while the interrupt x is executed the following behavior has to be considered: If the interrupt x is still pending (new interrupt or flag not cleared) and the new software priority is higher than the previous one, the interrupt x is re-entered. Otherwise, the software priority stays unchanged up to the next interrupt request (after the IRET of the interrupt x).

7.6 Interrupt instructions

Table 19. Dedicated interrupt instruction set(1)

Instruction	New description	Function/example	I1	H	I0	N	Z	C
HALT	Entering Halt mode		1		0			
IRET	Interrupt routine return	Pop CC, A, X, PC	I1	H	I0	N	Z	C
JRM	Jump if I1:0 = 11 (level 3)	I1:0 = 11 ?						
JRNM	Jump if I1:0 <> 11	I1:0 <> 11 ?						
Pop CC	Pop CC from the stack	Mem => CC	I1	H	I0	N	Z	C
RIM	Enable interrupt (level 0 set)	Load 10 in I1:0 of CC	1		0			
SIM	Disable interrupt (level 3 set)	Load 11 in I1:0 of CC	1		1			
TRAP	Software TRAP	Software IMI	1		1			
WFI	Wait for interrupt		1		0			

1. During the execution of an interrupt routine, the HALT, popCC, RIM, SIM and WFI instructions change the current software priority up to the next IRET instruction or one of the previously mentioned instructions.

7.7 External interrupts

The pending interrupts are cleared writing a different value in the ISx[1:0], IPA or IPB bits of the EICR.

Note: External interrupts are masked when an I/O (configured as input interrupt) of the same interrupt vector is forced to V_{SS}.

7.7.1 I/O port interrupt sensitivity

The external interrupt sensitivity is controlled by the IPA, IPB and ISxx bits of the EICR register (*Figure 20*). This control allows to have up to four fully independent external interrupt source sensitivities.

Each external interrupt source can be generated on four (or five) different events on the pin:

- Falling edge
- Rising edge
- Falling and rising edge
- Falling edge and low level
- Rising edge and high level (only for ei0 and ei2)

To guarantee correct functionality, the sensitivity bits in the EICR register can be modified only when the I1 and I0 bits of the CC register are both set to 1 (level 3).

8 Power saving modes

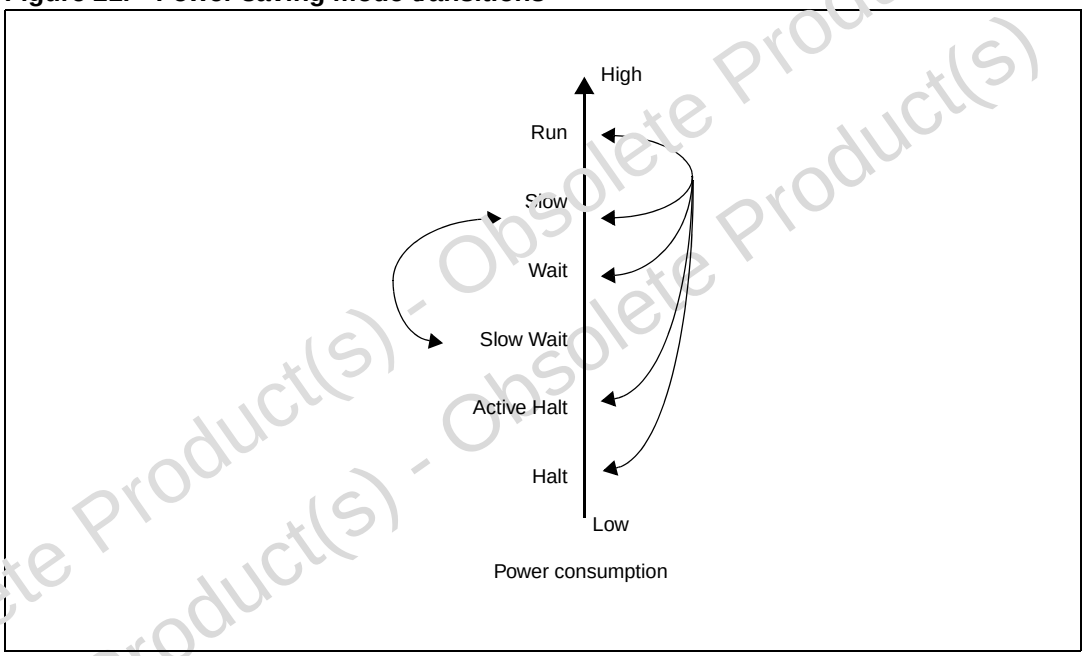
8.1 Introduction

To give a large measure of flexibility to the application in terms of power consumption, four main power saving modes are implemented in the ST7 (see *Figure 21*): Slow, Wait (Slow Wait), Active Halt and Halt.

After a reset the normal operating mode is selected by default (Run mode). This mode drives the device (CPU and embedded peripherals) by means of a master clock which is based on the main oscillator frequency divided or multiplied by 2 (f_{OSC2}).

From Run mode, the different power saving modes may be selected by setting the relevant register bits or by calling the specific ST7 software instruction whose action depends on the oscillator status.

Figure 21. Power saving mode transitions



Slave mode operation

In slave mode, the serial clock is received on the SCK pin from the master device.

To operate the SPI in slave mode:

1. Write to the SPICSR register to perform the following actions:
   - Select the clock polarity and clock phase by configuring the CPOL and CPHA bits (see *Figure 58*).

Note: The slave must have the same CPOL and CPHA settings as the master.

   - Manage the $\overline{SS}$ pin as described in *Slave select management on page 129* and *Figure 56*. If CPHA = 1 $\overline{SS}$ must be held low continuously. If CPHA = 0 $\overline{SS}$ must be held low during byte transmission and pulled up between each byte to let the slave write in the shift register.
2. Write to the SPICR register to clear the MSTR bit and set the SPE bit to enable the SPI I/O functions.

Slave mode transmit sequence

When software writes to the SPIDR register, the data byte is loaded into the 8-bit shift register and then shifted out serially to the MISO pin most significant bit first.

The transmit sequence begins when the slave device receives the clock signal and the most significant bit of the data on its MOSI pin.

When data transfer is complete:

- The SPIF bit is set by hardware.
- An interrupt request is generated if SPIE bit is set and interrupt mask in the CCR register is cleared.

Clearing the SPIF bit is performed by the following software sequence:

1. An access to the SPICSR register while the SPIF bit is set
2. A write or a read to the SPIDR register

Note: While the SPIF bit is set, all writes to the SPIDR register are inhibited until the SPICSR register is read.

The SPIF bit can be cleared during a second transmission; however, it must be cleared before the second SPIF bit in order to prevent an overrun condition (see *Overrun condition (OVR) on page 133*).

10.4.4 Clock phase and clock polarity

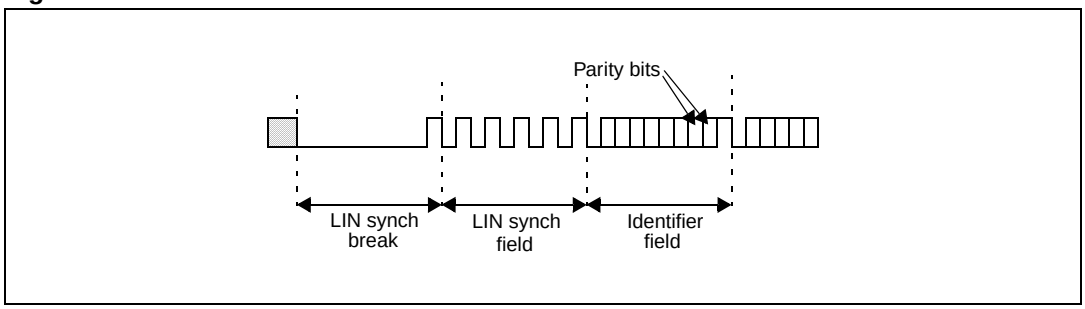
Four possible timing relationships may be chosen by software, using the CPOL and CPHA bits (see *Figure 58*).

Note: The idle state of SCK must correspond to the polarity selected in the SPICSR register (by pulling up SCK if CPOL = 1 or pulling down SCK if CPOL = 0).

The combination of the CPOL clock polarity and CPHA (clock phase) bits selects the data capture clock edge.

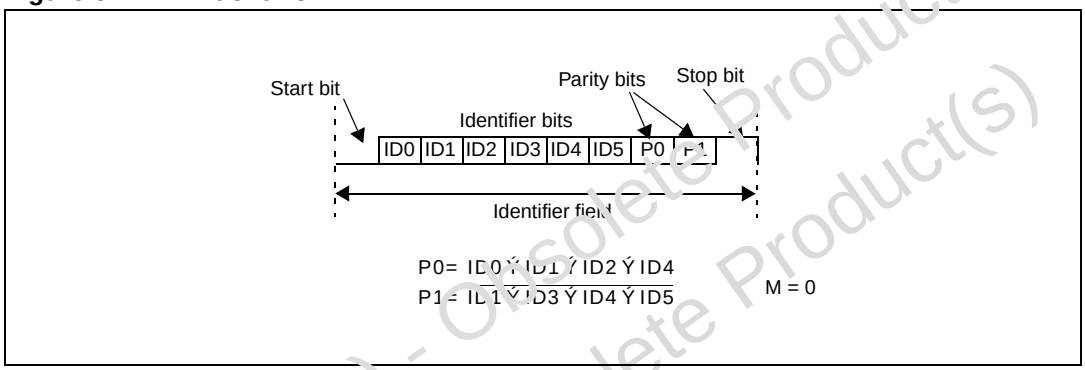
Figure 58 shows an SPI transfer with the four combinations of the CPHA and CPOL bits. The diagram may be interpreted as a master or slave timing diagram where the SCK pin, the MISO pin and the MOSI pin are directly connected between the master and the slave device.

Figure 66. LIN header



The bits involved are the two MSB positions (7th and 8th bits if M = 0; 8th and 9th bits if M = 0) of the identifier character. The check is performed as specified in *Figure 67* by the LIN specification.

Figure 67. LIN identifier



LIN error detection

LIN header error flag

The LIN header error flag indicates that an invalid LIN header has been detected.

When a LIN header error occurs:

- The LHE flag is set.
- An interrupt is generated if the RIE bit is set and the I[1:0] bits are cleared in the CCR register.

If autosynchronization is enabled (LASE bit = 1), this can mean that the LIN synch field is corrupted, and that the SCI is in a blocked state (LSF bit is set). The only way to recover is to reset the LSF bit and then to clear the LHE bit.

- The LHE bit is reset by an access to the SCISR register followed by a read of the SCIDR register.

LHE/OVR error conditions

When auto resynchronization is disabled (LASE bit = 0), the LHE flag detects the following:

- The received LIN synch field is not equal to 55h.
- An overrun has occurred (as in standard SCI mode).

Furthermore, if LHDM is set it also detects that a LIN header reception timeout occurred (only if LHDM is set).

Table 68. SCISR register description(1)

Bit	Name	Function
7	TDRE	Transmit data register empty This bit is set by hardware when the content of the TDR register has been transferred into the shift register. An interrupt is generated if the TIE = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a write to the SCIDR register). 0: Data is not transferred to the shift register 1: Data is transferred to the shift register
6	TC	Transmission complete This bit is set by hardware when transmission of a character containing data is complete. An interrupt is generated if TCIE = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a write to the SCIDR register). 0: Transmission is not complete 1: Transmission is complete *Note: TC is not set after the transmission of a preamble or a break.*
5	RDRF	Received data ready flag This bit is set by hardware when the content of the RDR register has been transferred to the SCIDR register. An interrupt is generated if RIE = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register). 0: Data is not received 1: Received data is ready to be read
4	IDLE	Idle line detected This bit is set by hardware when an idle line is detected. An interrupt is generated if the ILIE = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register). 0: No idle line is detected 1: Idle line is detected *Note: The idle bit is not set again until the RDRF bit has been set itself (that is, a new idle line occurs).*
3	LHE	LIN header error During LIN header this bit signals three error types: The LIN synch field is corrupted and the SCI is blocked in LIN Synch state (LSF bit = 1). A timeout occurred during LIN header reception. An overrun error was detected on one of the header field (see OR bit description in *SCI status register (SCISR) on page 152*). An interrupt is generated if RIE = 1 in the SCICR2 register. If blocked in the LIN synch state, the LSF bit must first be reset (to exit LIN synch field state and then to be able to clear LHE flag). Then it is cleared by the following software sequence: An access to the SCISR register followed by a read to the SCIDR register. 0: No LIN Header error 1: LIN Header error detected *Note: Apart from the LIN header this bit signals an overrun error as in SCI mode, (see description in SCI status register (SCISR) on page 152).*

10.5.11 LIN divider (LDIV) registers

LDIV is coded using the two registers LPR and LPFR. In LIN slave mode, the LPR register is accessible at the address of the SCIBRR register and the LPFR register is accessible at the address of the SCIETPR register.

LIN prescaler register (LPR)

LPR — Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
LPR[7:0]							
R/W							

Table 72. LPR register description

Bit	Name	Function
7:0	LPR[7:0]	LIN prescaler (mantissa of LDIV) These 8 bits define the value of the mantissa of the LDIV (see *Table 73*).

Table 73. LIN mantissa rounded values

LPR[7:0]	Rounded mantissa (LDIV)
00h	SCI clock disabled
01h	1
-	-
FEh	254
FFh	255

Caution: LPR and LPFR registers have different meanings when reading or writing to them. Consequently bit manipulation instructions (BRES or BSET) should never be used to modify the LPR[7:0] bits, or the LPFR[3:0] bits.

LIN prescaler fraction register (LPFR)

LPFR — Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
Reserved				LPFR[3:0]			
-				R/W			

Table 74. LPFR register description

Bit	Name	Function
7:4	-	Reserved
3:0	LPFR[3:0]	Fraction of LDIV These 4 bits define the fraction of the LDIV (see *Table 75*).

There is no minimum off time required for current control PWM in sensor mode so the minimum off time is set automatically to 0µs as soon as the SR bit is set in the MCRA register and a true 100% duty cycle can be set in the PWM compare U register for the PWM generation in voltage mode.

In sensor mode, the ZEF[3:0] bits in the MZFR register are active and can be used to define the number of consecutive Z samples needed to generate the active event.

Procedure for reading sensor inputs in direct access mode

In direct access mode, the sensors can be read either when the clock is enabled or disabled (depending on the CKE bit in the MCRA register). To read the sensor data the following steps have to be performed:

1. Select direct access mode (DAC bit in MCRA register)
2. Select the appropriate MCIx input pin by means of the IS[1:0] bits in the MPHST register
3. Read the comparator output (HST bit in the MREF register)

Sampling block

For a full digital solution, the phase comparator output sampling frequency is the frequency of the PWM signal applied to the switches and the sampling for the Z event detection in sensorless mode is done at the end of the off time of the PWM signal to avoid to have to re-create a virtual ground because when the PWM signal is off, the star point is at ground due to the free-wheeling diode. That's why, the sampling for Z event detection is done by default during the OFF-state of the PWM signal and therefore at the PWM frequency.

In current mode, this PWM signal is generated by a combination of the output of the measurement window generator (SA[3:0] bits), the output of the current comparator and a minimum OFF time set by the OT[3:0] bits for system stabilization.

In voltage mode, this PWM signal is generated by the 12-bit PWM generator signal in the compare U register with still a minimum OFF time required if the sampling is done at the end of the OFF time of the PWM signal for system stabilization. The PWM signal is put OFF as soon as the current feedback reaches the current input limitation. This can add an OFF time to the one programmed with the 12-bit Timer.

For D event detection in sensorless mode, no specific PWM configuration is needed and the sampling frequency (f_{SCF}, see *Table 166*) is completely independent from the PWM signal.

In sensor mode, the D event detection is not needed as the MCIA, MCIB and MCIC pins are the digital signals coming from the hall sensors so no specific PWM configuration is needed and the sampling for the Z detection event is done at f_{SCF}, completely independent from the PWM signal.

In sensorless mode, if a virtual ground is created by the addition of an external circuit, sampling for the Z event detection can be completely independent from the PWM signal applied to the switches. Setting the SPLG bit in the MCRC register allows a sampling frequency of f_{SCF} for Z event detection independent from the PWM signal after getting the D (end of demagnetization) event. This means that the sampling order is given whatever the PWM signal (during the ON time or the OFF time). As soon as the SPLG bit is set in the MCRC register, the minimum OFF time needed for the PWM signal in current mode is set to 0µs and a true 100% duty cycle can be set in the 12-bit PWM generator compare register in voltage mode.

Encoder mode (IS[1:0] = 11)

Figure 91 shows the signals delivered by a standard digital incremental encoder and associated information:

- Two 90° phased square signals with variable frequency proportional to the speed; they must be connected to MCIA and MCIB input pins,
- Clock derived from incoming signal edges,
- Direction information determined by the relative phase shift of input signals (+/-90°).

The incremental encoder interface block aims at extracting these signals. As input logic is both rising and falling edge sensitive (independently from TES[1:0] bits setting), resulting clock frequency is four times the one of the input signals, thus increasing resolution for measurements.

It may be noticed that direction bit (EDIR bit in MCRC register) is read only and that it does not affect counting direction of clocked timer (see *Section 10.6.7: Delay manager*). As a result, one cannot extract position information from encoder inputs during speed reversal.

Figure 90. Tacho capture events configured by the TES[1:0] bits

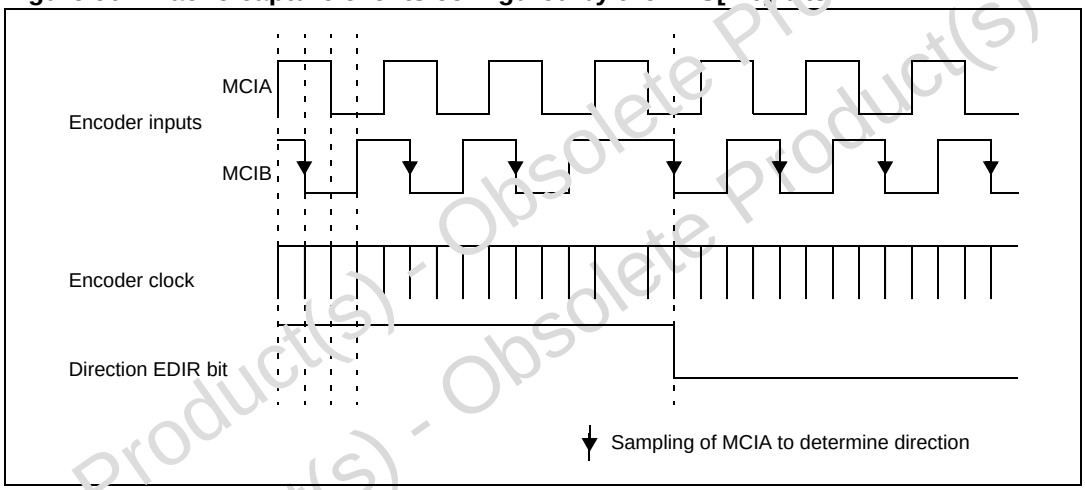
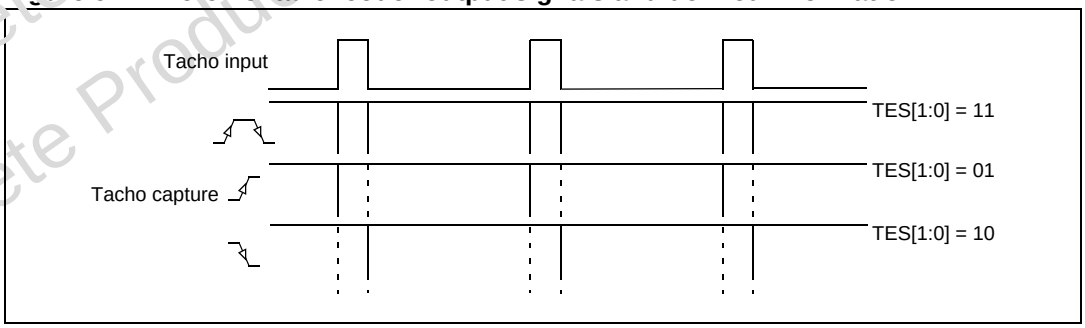


Figure 91. Incremental encoder output signals and derived information



Note: If only one encoder output is available, it may be input either on MCIA or MCIB and an encoder clock signal is still generated (in this case the frequency is 50% less than with two inputs.

The state of EDIR bit depends on signals present on MCIA and MCIB pins, the result is given by sampling the falling edges of MCIA with MCIB.

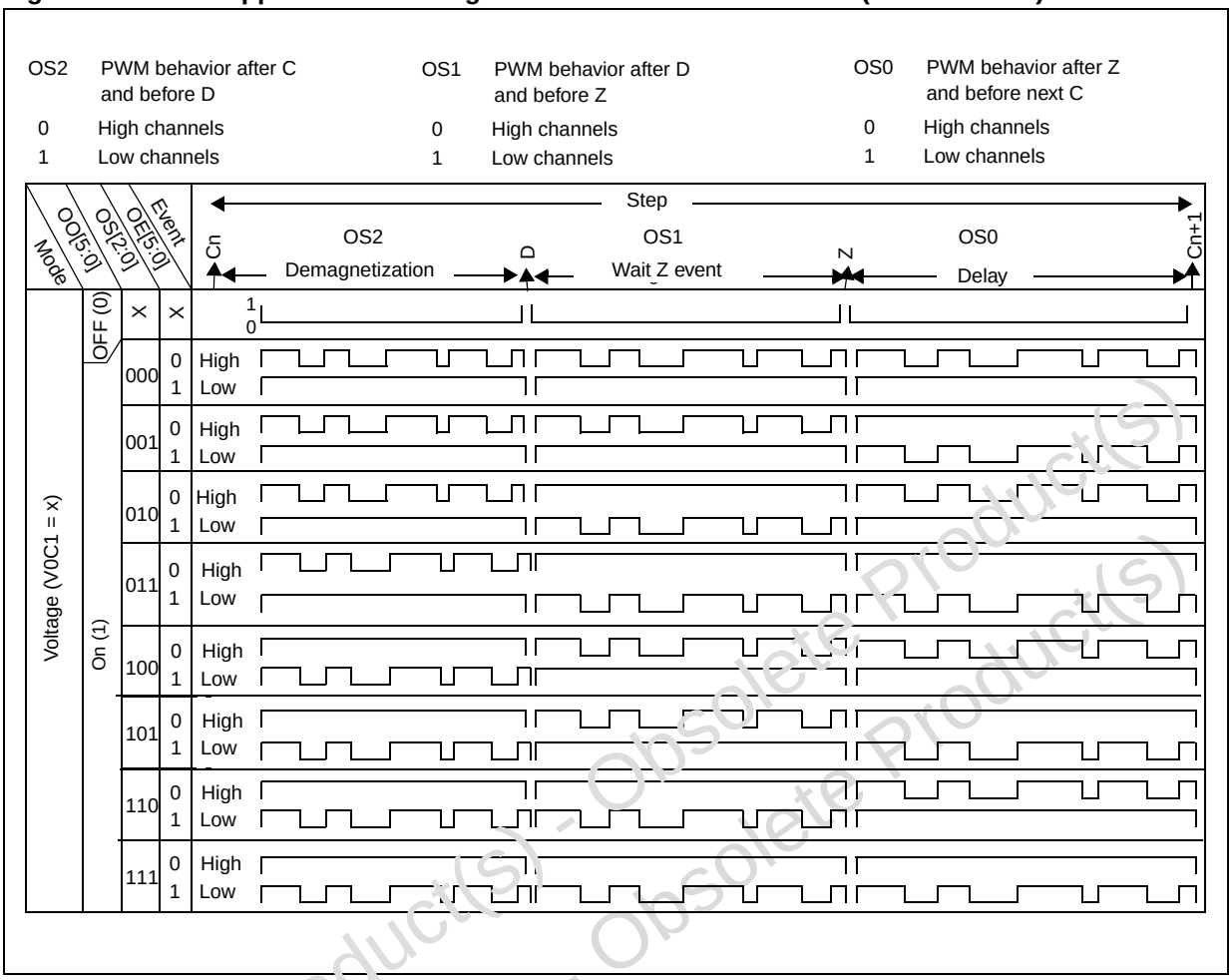
Note on using the three MCIx pins as standard I/Os: When none of the MCIx pins are needed in the application (for instance when driving an induction motor in open loop), they can be used as standard I/O ports, by configuring the motor controller as follows: PCN = 1, TES ≠ 0 and IS = 11. This disables the MCIx alternate functions and switches off the phase comparator. The state of the MCIx pins is summarized in *Table 94 on page 212*.

Table 94. MCIx pin configuration summary(1)

PCN	TES	SR	IS[1:0]	MCIA	MCIB	MCIC	Input detection block mode	Comments
0	00	0	00	Analog input(2)	Hi-Z or GND	Hi-Z or GND	Sensorless	All MCIx pins are reserved for the MTC peripheral.
			01	Hi-Z or GND	Analog input(2)	Hi-Z or GND		
			10	Hi-Z or GND	Hi-Z or GND	Analog input(2)		
			11	NA	NA	NA	NA	
		1	00	Analog input(2)	Standard I/O	Standard I/O	Position sensor	From 1 to 3 MCIx pins reserved depending on sensor
			01	Standard I/O	Analog input(2)	Standard I/O		
			10	Standard I/O	Standard I/O	Analog input(2)		
			11	Standard I/O	Standard I/O	Standard I/O	-	All MCIx pins are standard I/Os. Phase comparator is OFF
	≠ 0	x	xx	NA	NA	NA	NA	
1	00	x	00	Analog input(2)	Standard I/O	Standard I/O	-	Phase comparator is ON. The IS[1:0] bits must not be modified to avoid spurious event detection in motor controller
			01	Standard I/O	Analog input(2)	Standard I/O		
			10	Standard I/O	Standard I/O	Analog input(2)		
			11	Standard I/O	Standard I/O	Standard I/O	-	All MCIx pins are standard I/Os. Recommended configuration: phase comparator OFF
	≠ 00	x	00	Digital input(3)	Standard I/O	Standard I/O	Speed sensor tachogenerator	Phase comparator is OFF
			01	Standard I/O	Digital input(3)	Standard I/O		
			10	Standard I/O	Standard I/O	Digital input(3)		
			11	Digital input(3)	Digital input(3)	Standard I/O	Speed sensor encoder	

1. When PCN = 0, TES = 0 SR = 0, inputs in OFF-state are put in HiZ or grounded depending on the value of the DISS bit in the MSCR register.
2. Analog input: based on analog comparator and analog voltage reference. The corresponding digital I/O is disabled and data in the DR register is not representative of data on the input.
3. Digital input: use of standard V_{IL}, V_{IH} I/O level. This input can also be read via the associated I/O port.

Figure 110. PWM application in voltage or current sensorless mode (see *Table 133*)



Programmable chopper

Depending on the application hardware (use of a pulse transformer, for example), a chopper may be needed for the PWM signal. The MREF register allows the chopping frequency and mode to be programmed.

The HFE[1:0] bits program the channels on which chopping is to be applied. The chopped PWM signal may be needed for high side switches only, low side switches or both of them in the same time (see *Table 112*).

Table 112. Chopping mode

HFE[1:0] bits		Chopping mode	
HFE1	HFE0	PCN bit = 0	PCN bit = 1
0	0	OFF	OFF
0	1	Low channels only	Low side switches MCO1, 3, 5
1	0	High channels only	High side switches MCO0, 2, 4
1	1	Both low and high channels	Both high and low sides

The chopping frequency can be any of the eight values from 100 kHz to 2 MHz selected by the HFRQ[2:0] bits in the MREF register (see *Table 113*).

Table 113. Chopping frequency

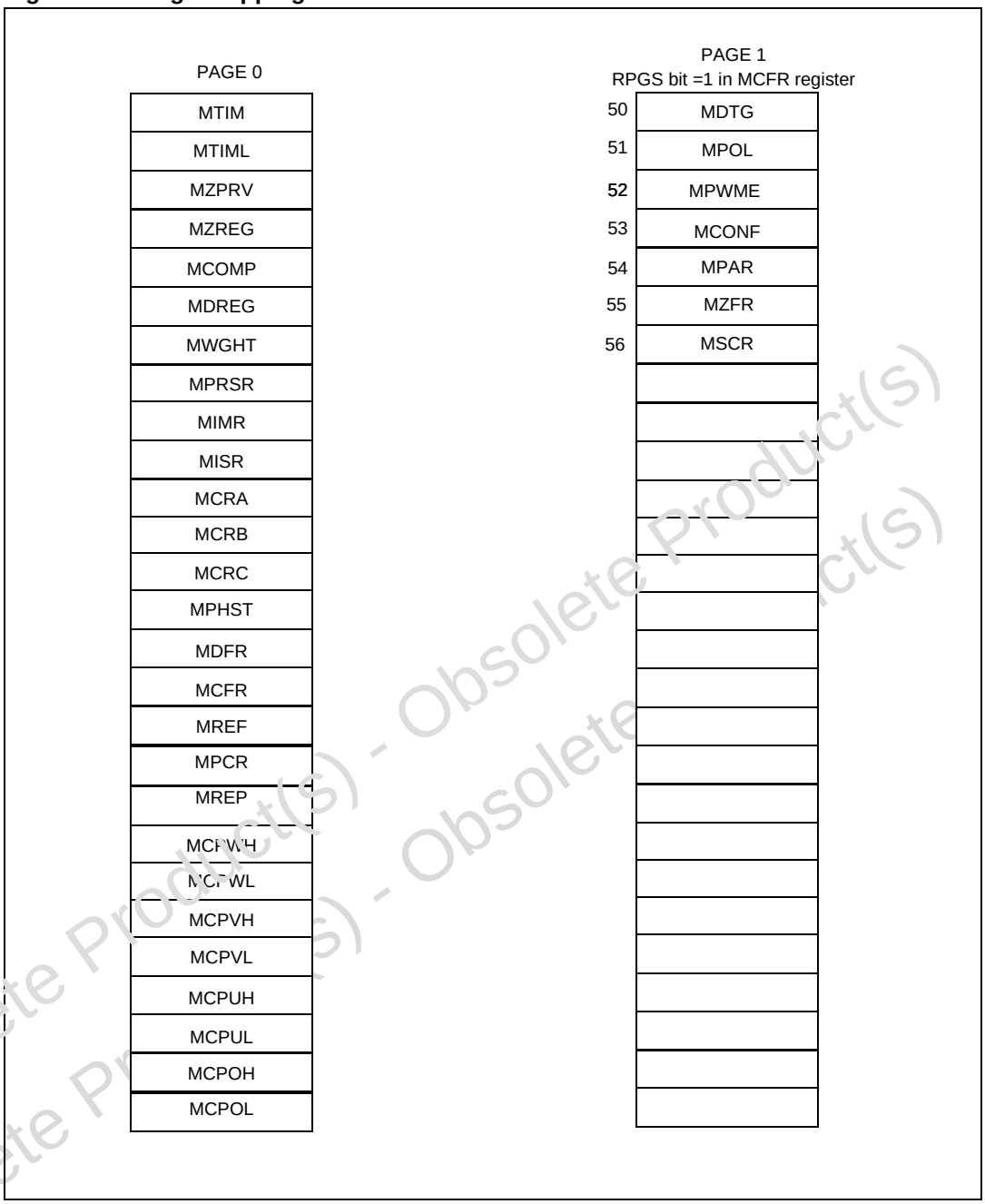
HFRQ2	HFRQ1	HFRQ0	Chopping frequency	
			F_{mtc} = 16 MHz; F_{mtc} = 8 MHz	F_{mtc} = 4 MHz
0	0	0	100 kHz	50 kHz
0	0	1	200 kHz	100 kHz
0	1	0	400 kHz	200 kHz
0	1	1	500 kHz	250 kHz
1	0	0	800 kHz	400 kHz
1	0	1	1 MHz	500 kHz
1	1	0	1.33 MHz	666.66 MHz
1	1	1	2 MHz	1 MHz

Note: When the PCN bit = 0:

- If complementary PWM signals are not applied (DTE bit = 0), the high and low drivers are fixed by the MPAR register. Figure 109, Figure 115 and Figure 116 indicate where the HFE[1:0] bits are taken into account depending on the PWM application.

- If complementary PWM signals are applied (DTE bit = 1), the channels are paired as explained in Deadtime generator on page 245. This means that the high and low channels are fixed and the HFE[1:0] bits indicate where to apply the chopper. Figure 117 shows typical complementary PWM signals with high frequency chopping enabled on both high and low drivers.

Figure 126. Page mapping for motor control



12 Electrical characteristics

12.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

12.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25°C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σσ).

12.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25°C, V_{DD} = 5V. They are given only as design guidelines and are not tested.

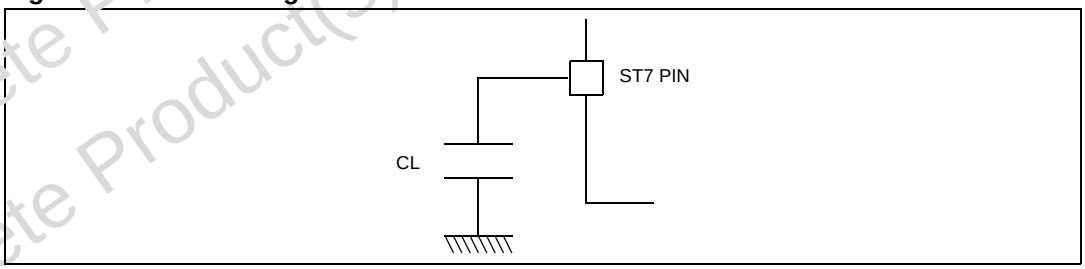
12.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

12.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 129*.

Figure 129. Pin loading conditions



12.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 130*.

12.3.2 Operating conditions with low voltage detector (LVD)

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A.

Table 190. Operating conditions with LVD

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IT+(LVD)}$	Reset release threshold (V_{DD} rise)		3.90	4.20	4.50	V
$V_{IT-(LVD)}$	Reset generation threshold (V_{DD} fall)		3.80	4.00	4.35	
$V_{hys(LVD)}$	LVD voltage threshold hysteresis	$V_{IT+(LVD)}$-$V_{IT-(LVD)}$		200		mV
Vt_{POR}	V_{DD} rise time rate(1)		20			µs/V
					100	ms/V
$t_{g(VDD)}$	Width of filtered glitches on V_{DD}(1) (which are not detected by the LVD)				40	ns

1. Data based on characterization results, not tested in production.

12.3.3 Auxiliary voltage detector (AVD) thresholds

Subject to general operating condition for V_{DD}, f_{OSC}, and T_A.

Table 191. AVD thresholds

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
$V_{IT+(AVD)}$	1=>0 AVDF flag toggle threshold (V_{DD} rise)		4.35	4.70	4.90	V
$V_{IT-(AVD)}$	0=>1 AVDF flag toggle threshold (V_{DD} fall)		4.20	4.50	4.70	
$V_{hyst(AVD)}$	AVD voltage threshold hysteresis(2)	$V_{IT+(AVD)}$-$V_{IT-(AVD)}$		200		mV
ΔV_{IT-}	Voltage drop between AVD flag set and LVD reset activated	$V_{IT-(AVD)}$-$V_{IT-(LVD)}$		450		mV

1. See *Section 15.7: Maximum values of AVD thresholds on page 366*
2. Data based on characterization results, not tested in production.

15.5 Missing detection of BLDC ‘Z event’

For a BLDC drive, the deadtime generator is enabled through the MDTG register (PCN = 0 and DTE = 1). If the duty cycle of the PWM signal generated to drive the motor is lower than the programmed deadtime, the Z event sampling is missing.

Workaround

The complementary PWM must be disabled by resetting the DTE bit in the MDTG register (see *Deadtime generator register (MDTG) on page 280*).

As the current in the motor is very low in this case, the MOSFET body diode can be used.

15.6 Reset value of unavailable pins

On rev. A silicon versions, some ports (ports A, C and E) have fewer than eight pins. The bits associated to the unavailable pins must always be kept at reset state.

15.7 Maximum values of AVD thresholds

On rev. A silicon versions, the maximum values of AVD thresholds are not tested in production.

15.8 External interrupt missed

To avoid any risk if generating a parasitic interrupt, the edge detector is automatically disabled for one clock cycle during an access to either DDR and OR. Any input signal edge during this period is not detected and an interrupt is not generated.

This case can typically occur if the application refreshes the port configuration registers at intervals during runtime.

Workaround

The workaround is based on software checking the level on the interrupt pin before and after writing to the PxOR or PxDDR registers. If there is a level change (depending on the sensitivity programmed for this pin) the interrupt routine is invoked using the call instruction with three extra push instructions before executing the interrupt routine (this is to make the call compatible with the IRET instruction at the end of the interrupt service routine).

But detection of the level change does not make sure that edge occurs during the critical 1 cycle duration and the interrupt has been missed. This may lead to occurrence of same interrupt twice (one hardware and another with software call).

To avoid this, a semaphore is set to '1' before checking the level change. The semaphore is changed to level '0' inside the interrupt routine. When a level change is detected, the semaphore status is checked and if it is '1' this means that the last interrupt has been missed. In this case, the interrupt routine is invoked with the call instruction.

There is another possible case, that is, if writing to PxOR or PxDDR is done with global interrupts disabled (interrupt mask bit set). In this case, the semaphore is changed to '1' when the level change is detected. Detecting a missed interrupt is done after the global interrupts are enabled (interrupt mask bit reset) and by checking the status of the