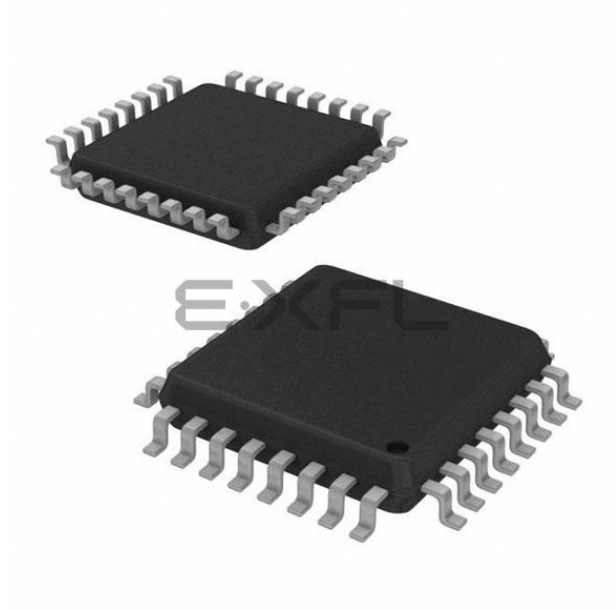

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	LINbusSCI
Peripherals	LVD, Motor Control PWM, POR, PWM, WDT
Number of I/O	17
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7fmc1k6tc

Table 3. Hardware register map (continued)

Address	Block	Register label	Register name	Reset status	Remarks
0074h	PWM ART	PWMDCR3	PWM AR timer duty cycle register 3	00h	R/W
0075h		PWMDCR2	PWM AR timer duty cycle register 2	00h	R/W
0076h		PWMDCR1	PWM AR timer duty cycle register 1	00h	R/W
0077h		PWMDCR0	PWM AR timer duty cycle register 0	00h	R/W
0078h		PWMCR	PWM AR timer control register	00h	R/W
0079h		ARTCSR	Auto-reload timer control/status register	00h	R/W
007Ah		ARTCAR	Auto-reload timer counter access register	00h	R/W
007Bh		ARTARR	Auto-reload timer auto-reload register	00h	R/W
007Ch		ARTICCSR	AR timer input capture control/status register	00h	R/W
007Dh		ARTICR1	AR timer input capture register 1	00h	Read only
007Eh		ARTICR2	AR timer input capture register 2	00h	Read only
007Fh	Op-amp	OACSR	Op-amp control/status register	00h	R/W

1. The contents of the I/O port DR registers are readable only in output configuration. In input configuration, the values of the I/O pins are returned instead of the DR register contents.
2. R/W = read/write
3. The bits associated with unavailable pins must always keep their reset value.
4. x = undefined.

4 Flash program memory

4.1 Introduction

The ST7 dual voltage high density Flash (HDFlash) is a non-volatile memory that can be electrically erased as a single block or by individual sectors and programmed on a byte-by-byte basis using an external V_{PP} supply.

The HDFlash devices can be programmed and erased off-board (plugged in a programming tool) or on-board using ICP (in-circuit programming) or IAP (in-application programming).

The array matrix organization allows each sector to be erased and reprogrammed without affecting other sectors.

4.2 Main features

- 3 Flash programming modes:
  - Insertion in a programming tool. In this mode, all sectors including option bytes can be programmed or erased.
  - ICP (in-circuit programming). In this mode, all sectors including option bytes can be programmed or erased without removing the device from the application board.
  - IAP (in-application programming) In this mode, all sectors except Sector 0, can be programmed or erased without removing the device from the application board and while the application is running.
- ICT (in-circuit testing) for downloading and executing user application test patterns in RAM
- Read-out protection
- Register access security system (RASS) to prevent accidental programming or erasing

4.3 Structure

The Flash memory is organized in sectors and can be used for both code and data storage.

Depending on the overall Flash memory size in the microcontroller device, there are up to three user sectors (see *Table 4*). Each of these sectors can be erased independently to avoid unnecessary erasing of the whole Flash memory when only a partial erasing is required.

The first two sectors have a fixed size of 4 Kbytes (see *Figure 5*). They are mapped in the upper part of the ST7 addressing space so the reset and interrupt vectors are located in Sector 0 (F000h-FFFFh).

Table 4. Sectors available in Flash devices

Flash size (bytes)	Available sectors
4K	Sector 0
8K	Sectors 0,1
> 8K	Sectors 0,1, 2

4.3.1 Read-out protection

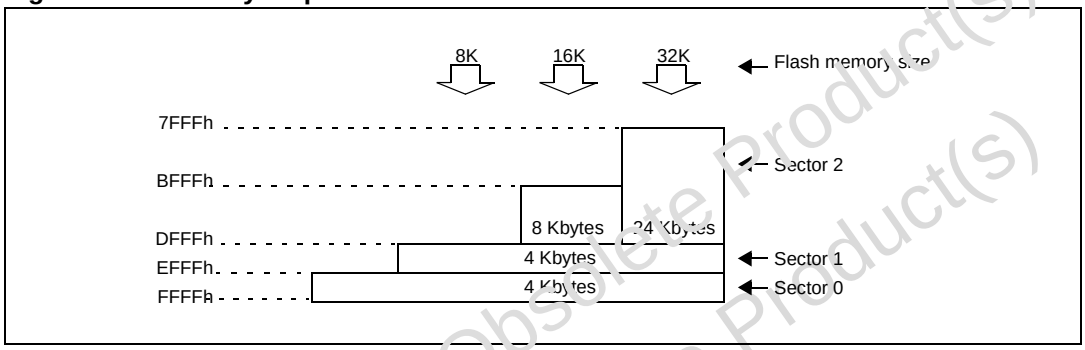
Read-out protection, when selected, provides a protection against Program Memory content extraction and against write access to Flash memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

In Flash devices, this protection is removed by reprogramming the option. In this case, the entire program memory is first automatically erased and the device can be reprogrammed.

Read-out protection selection depends on the device type:

- In Flash devices it is enabled and removed through the FMP_R bit in the option byte.
- In ROM devices it is enabled by mask option specified in the Option List.

Figure 5. Memory map and sector address

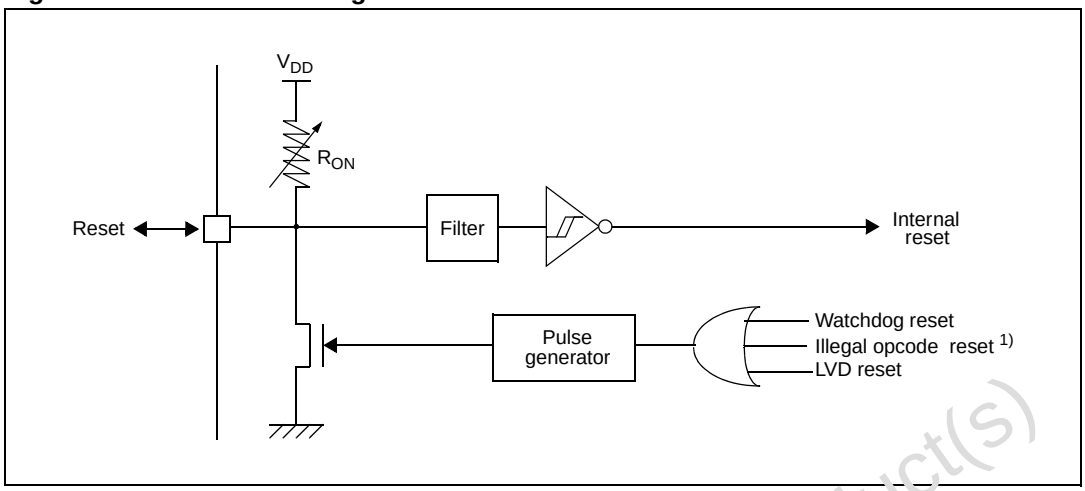


4.4 ICC interface

ICC (in-circuit communication) needs a minimum of 4 and up to 6 pins to be connected to the programming tool (see *Figure 6*). These pins are:

- $\overline{\text{RESET}}$: device reset
- V_{SS}: device power supply ground
- ICCCLK: ICC output serial clock pin
- ICCDATA: ICC input/output serial data pin
- ICCSEL/V_{PP}: programming voltage
- OSC1(or OSCIN): main clock input for external source (optional)
- V_{DD}: application board power supply (see *Figure 6*, Note 3)

Figure 11. Reset block diagram



1. See *Section 11.2.2: Illegal opcode reset on page 309* for more details on illegal opcode reset conditions.

The $\overline{\text{RESET}}$ pin is an asynchronous signal which plays a major role in EMS performance. In a noisy environment, it is recommended to follow the guidelines mentioned in the electrical characteristics section.

6.4.3 External power-on reset

If the LVD is disabled by option byte, to start up the microcontroller correctly, the user must ensure by means of an external reset circuit that the reset signal is held low until V_{DD} is over the minimum level specified for the selected f_{OSC} frequency.

A proper reset signal for a slow rising V_{DD} supply can generally be provided by an external RC network connected to the $\overline{\text{RESET}}$ pin.

6.4.4 Internal low voltage detector (LVD) reset

Two different reset sequences caused by the internal LVD circuitry can be distinguished:

- Power-on reset
- Voltage drop reset

The device $\overline{\text{RESET}}$ pin acts as an output that is pulled low when $V_{DD} < V_{IT+}$ (rising edge) or $V_{DD} < V_{IT-}$ (falling edge) as shown in *Figure 12*.

The LVD filters spikes on V_{DD} larger than $t_{g(VDD)}$ to avoid parasitic resets.

6.4.5 Internal watchdog reset

The RESET sequence generated by a internal watchdog counter overflow is shown in *Figure 12*.

Starting from the Watchdog counter underflow, the device $\overline{\text{RESET}}$ pin acts as an output that is pulled low during at least $t_{w(RSTL)out}$.

6.6.6 Interrupts

The MCC/RTC interrupt event generates an interrupt if the OIE bit of the MCCSR register is set and the interrupt mask in the CC register is not active (RIM instruction).

Table 12. MCC/RTC interrupt control/wake-up capability

Interrupt event	Event flag	Enable control bit	Exit from WAIT	Exit from HALT
Time base overflow event	OIF	OIE	Yes	No(1)

1. The MCC/RTC interrupt wakes up the MCU from Active Halt mode, not from Halt mode.

6.6.7 MCC control status register (MCCSR)

MCCSR Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
MCO	CP[1:0]		SMS	TB[1:0]		OIE	OIF
R/W	R/W		R/W	R/W		R/W	R/W

Table 13. MCCSR register description

Bit	Name	Function
7	MCO	Main clock out selection This bit enables the MCO alternate function on the PF0 I/O port. It is set and cleared by software. 0: MCO alternate function disabled (I/O pin free for general-purpose I/O) 1: MCO alternate function enabled (f_{OSC2} on I/O port) *Note: To reduce power consumption, the MCO function is not active in Active Halt mode.*
6:5	CP[1:0]	CPU clock prescaler These bits select the CPU clock prescaler which is applied in the different slow modes. Their action is conditioned by the setting of the SMS bit. These two bits are set and cleared by software: 00: f_{CPU} in slow mode = $f_{OSC2}/2$ 01: f_{CPU} in slow mode = $f_{OSC2}/4$ 10: f_{CPU} in slow mode = $f_{OSC2}/8$ 11: f_{CPU} in slow mode = $f_{OSC2}/16$
4	SMS	Slow mode select This bit is set and cleared by software. 0: Normal mode. $f_{CPU} = f_{OSC2}$ 1: Slow mode. f_{CPU} is given by CP1, CP0 See *Section 8.2: Slow mode* and *Section 6.6: Main clock controller with real time clock and beeper (MCC/RTC)* for more details.

8.4.2 Halt mode

The Halt mode is the lowest power consumption mode of the MCU. It is entered by executing the 'HALT' instruction when the OIE bit of the main clock controller status register (MCCSR) is cleared (see *Section 6.6 on page 54* for more details on the MCCSR register).

The MCU can exit Halt mode on reception of either a specific interrupt (see *Table 22: Interrupt mapping on page 70*) or a reset. When exiting Halt mode by means of a reset or an interrupt, the oscillator is immediately turned on and the 256 or 4096 CPU cycle delay is used to stabilize the oscillator. After the start up delay, the CPU resumes operation by servicing the interrupt or by fetching the reset vector which woke it up (see *Figure 27*).

When entering Halt mode, the I[1:0] bits in the CC register are forced to '10b'to enable interrupts. Therefore, if an interrupt is pending, the MCU wakes up immediately.

In Halt mode, the main oscillator is turned off causing all internal processing to be stopped, including the operation of the on-chip peripherals. All peripherals are not clocked except the ones which get their clock supply from another clock generator (such as an external or auxiliary oscillator).

The compatibility of Watchdog operation with Halt mode is configured by the "WDGHALT" option bit of the option byte. The HALT instruction when executed while the Watchdog system is enabled, can generate a Watchdog RESET (see *Section 14.1 on page 356* for more details).

Figure 26. HALT timing overview

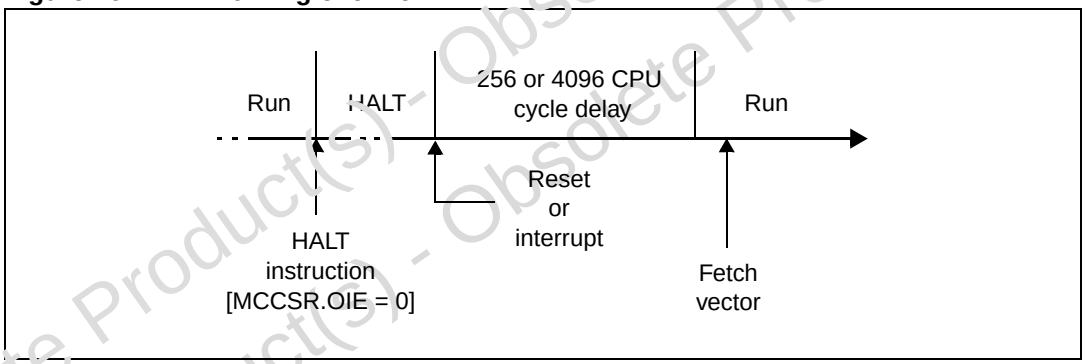


Table 41. PWMCR register description

Bit	Name	Function
7:4	OE[3:0]	PWM output enable These bits are set and cleared by software. They enable or disable the PWM output channels independently acting on the corresponding I/O pin. 0: PWM output disabled 1: PWM output enabled
3:0	OP[3:0]	PWM output polarity These bits are set and cleared by software. They independently select the polarity of the four PWM output signals (see *Table 42*).

Table 42. PWM output signal polarity selection

PWMx output level		OPx(1)
Counter ≤ OCRx	Counter > OCRx	
1	0	0
0	1	1

1. When an OPx bit is modified, the PWMx output signal polarity is immediately reversed.

PWM duty cycle registers (PWMDCRx)

PWMDCRx Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
DC[7:0]							
R/W							

Table 43. PWMDCRx register description

Bit	Name	Function
7:0	DC[7:0]	Duty cycle data These bits are set and cleared by software. A PWMDCRx register is associated with the OCRx register of each PWM channel to determine the second edge location of the PWM signal (the first edge location is common to all channels and given by the ARTARR register). These PWMDCR registers allow the duty cycle to be set independently for each PWM channel.

ART input capture control/status register (ARTICCSR)

ARTICCSR Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
Reserved		CS[2:1]		CIE[2:1]		CF[2:1]	
-		R/W		R/W		R/W	

A minimum of four falling edges of the CPU clock must occur between two consecutive active edges of the external clock; thus the external clock frequency must be less than a quarter of the CPU clock frequency.

Figure 42. Counter timing diagram, internal clock divided by 2

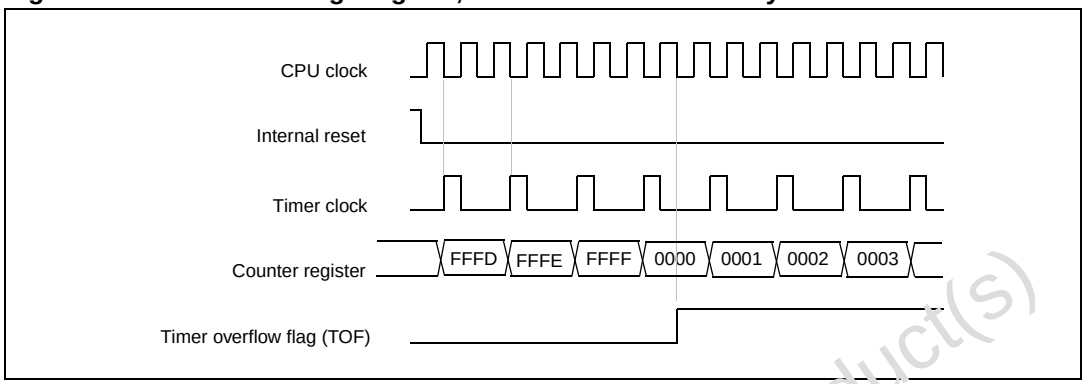


Figure 43. Counter timing diagram, internal clock divided by 4

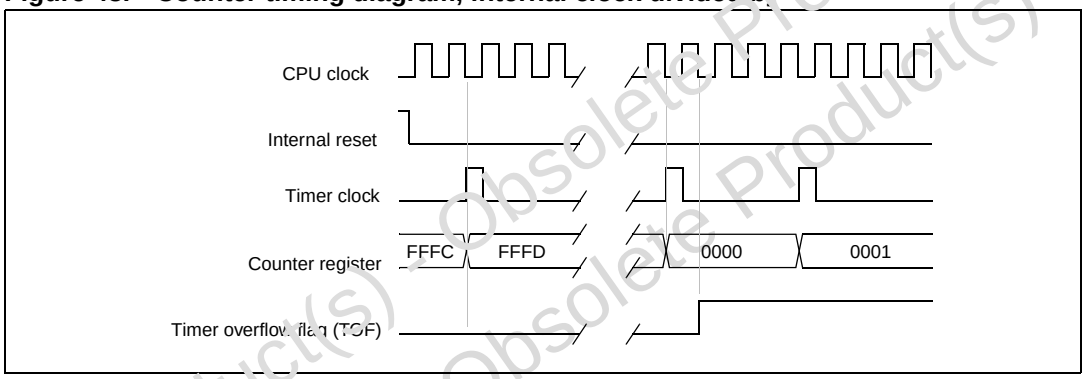
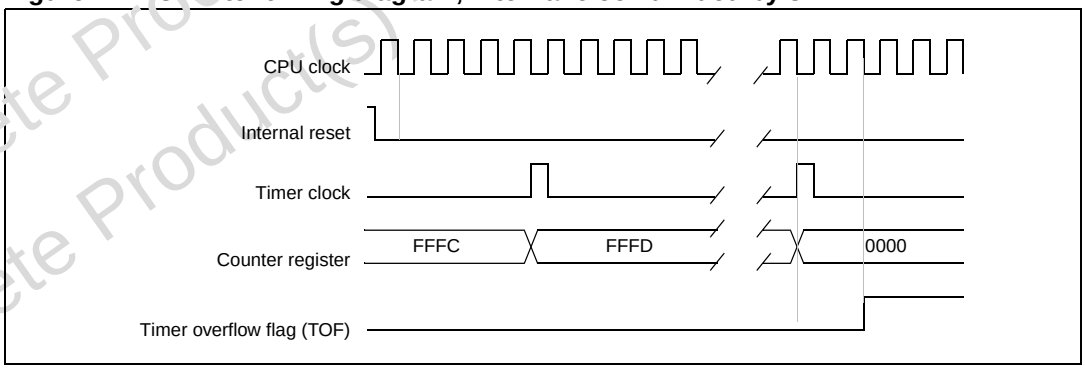
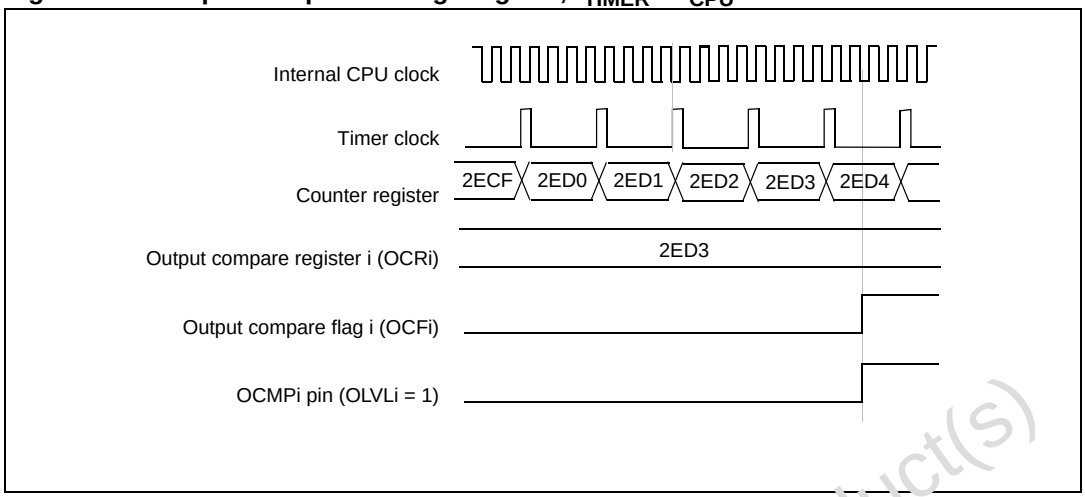


Figure 44. Counter timing diagram, internal clock divided by 8



Note: The device is in reset state when the internal reset signal is high, when it is low the device is running.

Figure 49. Output compare timing diagram, $f_{TIMER} = f_{CPU}/4$



One pulse mode

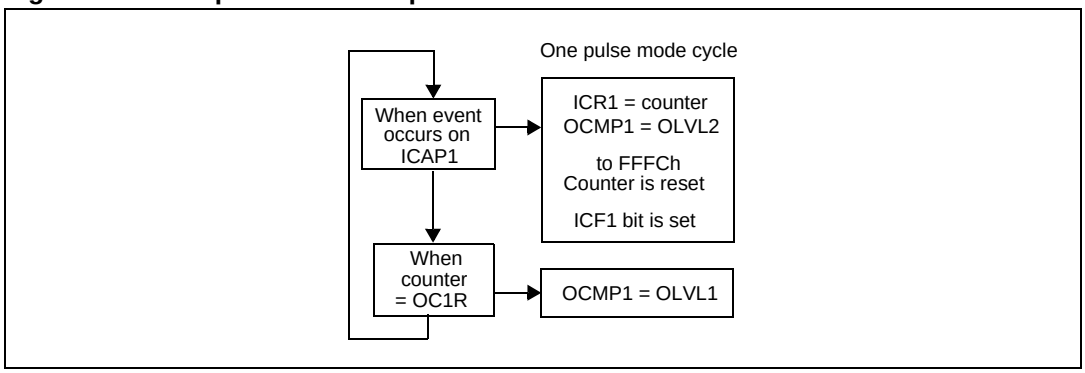
One pulse mode enables the generation of a pulse when an external event occurs. This mode is selected via the OPM bit in the CR2 register.

The one pulse mode uses the input capture1 function and the output compare1 function.

Procedure

1. Load the OC1R register with the value corresponding to the length of the pulse (see *Equation 3* below).
2. Select the following in the CR1 register:
   - Using the OLVL1 bit, select the level to be applied to the OCMP1 pin after the pulse.
   - Using the OLVL2 bit, select the level to be applied to the OCMP1 pin during the pulse.
   - Select the edge of the active transition on the ICAP1 pin with the IEDG1 bit (the ICAP1 pin must be configured as floating input).
3. Select the following in the CR2 register:
   - Set the OC1E bit, the OCMP1 pin is then dedicated to the output compare 1 function.
   - Set the OPM bit.
   - Select the timer clock CC[1:0] (see *Table 51*).

Figure 50. One pulse mode sequence



When a valid event occurs on the ICAP1 pin, the counter value is loaded in the ICR1 register. The counter is then initialized to FFFCh, the OLVL2 bit is output on the OCMP1 pin and the ICF1 bit is set.

Because the ICF1 bit is set when an active edge occurs, an interrupt can be generated if the ICIE bit is set.

Clearing the input capture interrupt request (that is, clearing the ICF*i* bit) is done in two steps:

1. Reading the SR register while the ICF*i* bit is set.
2. Accessing (reading or writing) the IC*i*LR register.

The OC1R register value required for a specific timing application can be calculated using the following formula:

Equation 3

$$OCiR\ value = \frac{t * f_{CPU}}{PRESC} - 5$$

Where:

t = pulse period (in seconds)

f_{CPU} = CPU clock frequency (in hertz)

$_{PRESC}$ = timer prescaler factor (2, 4 or 8 depending on the CC[1:0] bits, see *Table 51*)

If the timer clock is an external clock the formula is:

Equation 4

$$OCiR = t * f_{EXT} - 5$$

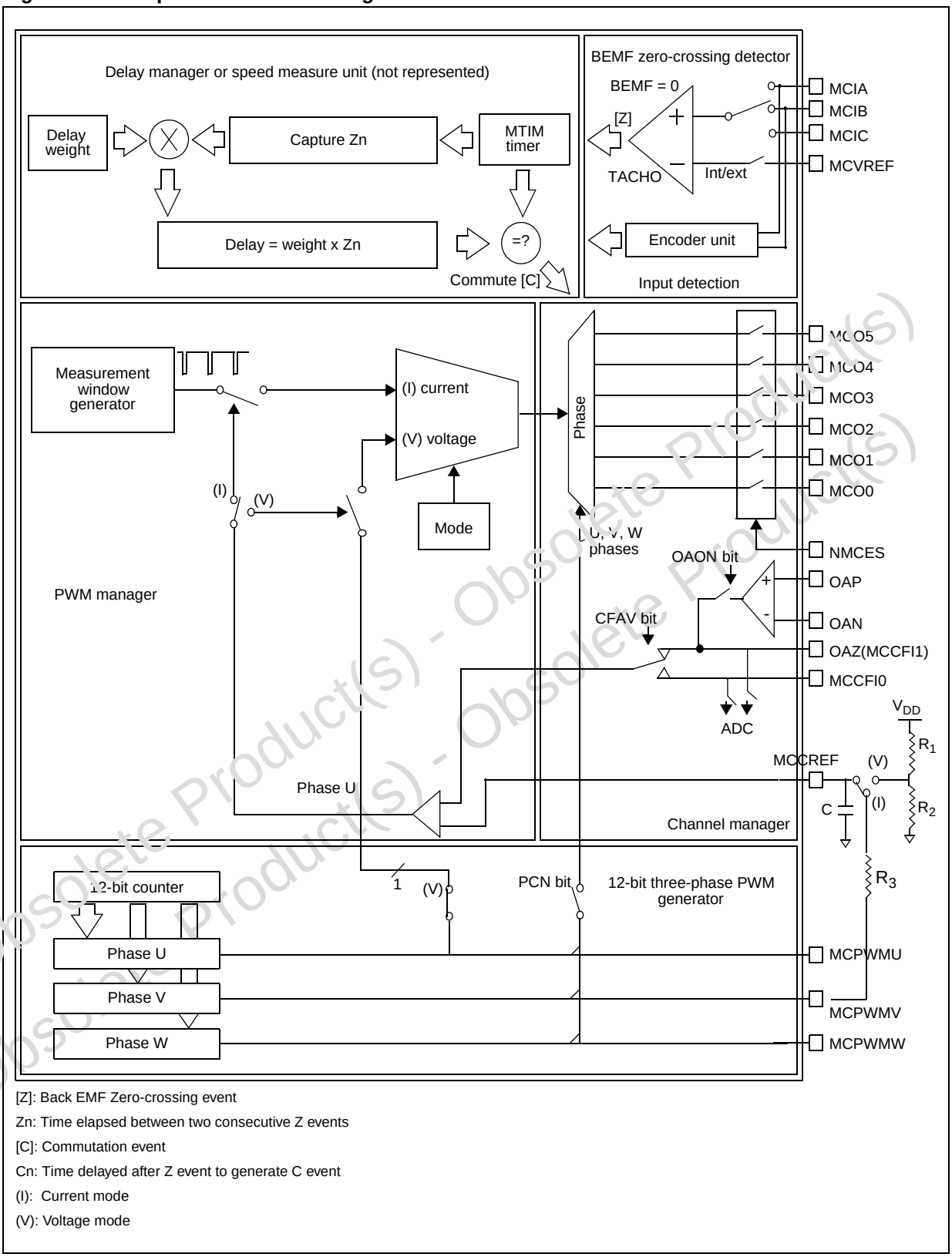
Where:

t = pulse period (in seconds)

f_{EXT} = external timer clock frequency (in hertz)

When the value of the counter is equal to the value of the contents of the OC1R register, the OLVL1 bit is output on the OCMP1 pin, (see *Figure 51*).

Figure 78. Simplified MTC block diagram



[Z]: Back EMF Zero-crossing event

Zn: Time elapsed between two consecutive Z events

[C]: Commutation event

Cn: Time delayed after Z event to generate C event

(I): Current mode

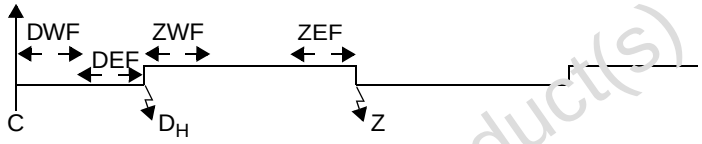
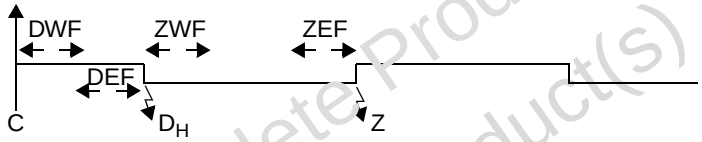
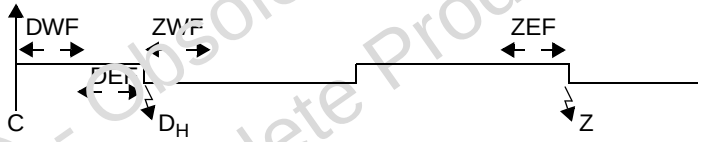
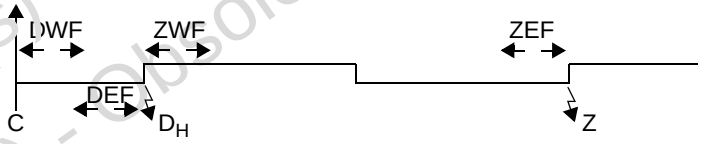
(V): Voltage mode

Table 87. Z event filter setting (continued)

ZEF3	ZEF2	ZEF1	ZEF0	Z event limit
1	1	1	0	15
1	1	1	1	16

Table 88 shows the event control selected by the ZVD and CPB bits. In most cases, the D and Z events have opposite edge polarity, so the ZVD bit is usually 0.

Table 88. ZVD and CPB edge selection bits(1)

ZVD bit	CPB bit	Event generation vs input data sampled
0	0	
0	1	
1	0	
1	1	
Note: The ZVD bit is located in the MPOL register, the CPB bit is in the MCRB register.		

1. Legend:
DW = D window filter
DEF = D event filter
ZWF = Z window filter
ZEF = Z event filter. Refer also to *Table 92 on page 207*.

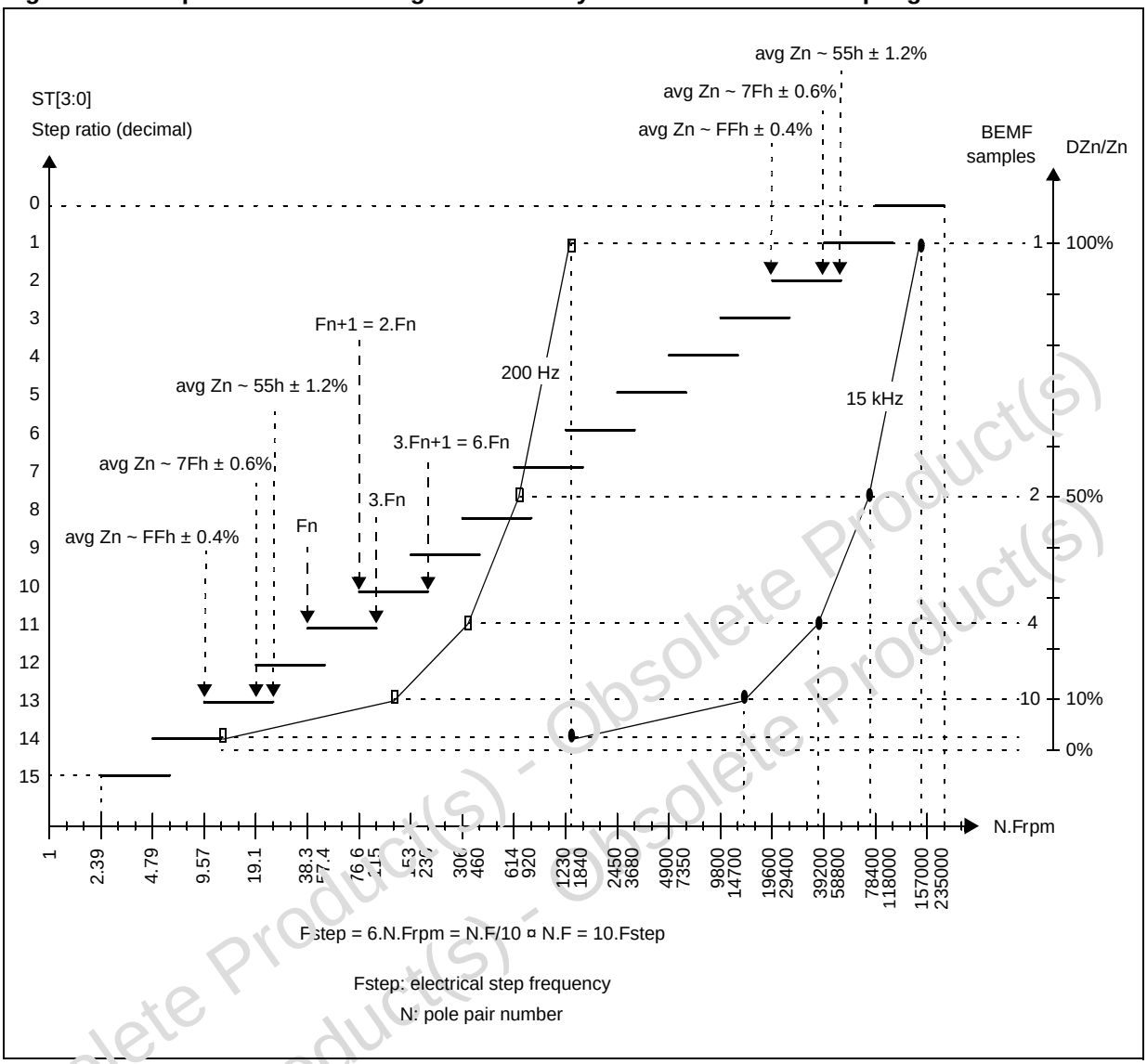
Demagnetization (D) event

At the end of the demagnetization phase, current no longer goes through the free-wheeling diodes. The voltage on the non-excited winding terminal goes from one of the power rail voltages to the common star connection voltage plus the BEMF voltage. In some cases (if the BEMF voltage is positive and the free-wheeling diodes are at ground for example) this end of demagnetization can be seen as a voltage edge on the selected MCIx input and it is called a hardware demagnetization event D_H. See *Table 88*.

The D event filter can be used to select the number of consecutive D events needed to generate the D_H event.

If enabled by the HDM bit in the MCRB register, the current value of the MTIM timer is captured in register MDREG when this event occurs in order to be able to simulate the demagnetization phase for the next steps.

Figure 99. Step ratio bits decoding and accuracy results and BEMF sampling rate



Hall sensors (or equivalent sensors providing position information) are widely used for motor control. There are two cases to be considered:

- BLDC motor or six-step synchronous motor drive; ‘sensor mode’ is recommended in this case, as most tasks are performed by hardware in the delay manager.
- BLAC, asynchronous or motors supplied with 3-phase sinewave-modulated PWM signals in general. In this case ‘speed sensor mode’ allows high accuracy speed measurement (the sensor mode of the delay manager being unsuitable for sinewave generation). Position information is handled by software to lock the statoric field to the rotoric one for driving synchronous motors.

Hall sensors are usually arranged in a 120° configuration. In that case they provide 3 ppr with both rising and falling edge triggering; the tachogenerator measurement method can therefore be applied. The main difference lies in the fact that one must use the position information they provide. This can be done using the three MCIx pins and the analog multiplexer to know which of the three sensors toggled; an interrupt is generated just after the expected transition (refer to *Figure 102*).

As described in *Figure 103*, the MTIM timer is re-configured depending on the selected sensor. This means that most of delay manager registers are used for a different purpose, with modified functionalities.

For greater precision, the MTIM up-counter is extended to 16 bits using MTIM and an additional MTIML register. On a capture event, the current counter value is captured and the counter [MTIM:MTIML] is cleared. The counting direction is not affected by the EDIR bit when using an encoder sensor.

A 16-bit capture register is used to store the captured value of the extended MTIM counter: the speed result is either a period in clock cycles or a number of encoder pulses. This 16-bit register is mapped in the MZREG and MZPRV register addresses. To ensure that the read value is not corrupted between the high and low byte accesses, a read access to the MSB of this register (MZREG) locks the LSB (that is, MZPRV content is locked) until it is read and any other capture event in between these two accesses is discarded.

A compare unit allows a maximum value to be entered for the tacho periods. If the 16-bit counter [MTIM:MTIML] exceeds this value, a speed error interrupt is generated. This may be used to warn the user that the tachogenerator signal is lost (wires disconnected, motor stalled,...). As 8-bit accuracy is sufficient for this purpose, only the MSByte of the counter (that is, MTIM) is compared to 8-bit compare register, mapped in the MDREG register location. The LSByte is nevertheless compared with a fixed FFh value. Available values for comparison are therefore FFFFh, FEFFh, FDFFh, ..., 01FFh, 00FFh.

Note: This functionality is not useful when using an encoder. With an encoder, user must monitor the captured values by software during the periodic capture interrupts: for instance, when driving an AC motor, if the values are too low compared to the stator frequency, a software interrupt may be triggered.

Table 125. MISR register description (continued)

Bit	Name	Function
1	DI	End of demagnetization interrupt flag 0: No end of demagnetization interrupt pending 1: End of demagnetization interrupt pending
0	CI	Commutation/capture interrupt flag 0: No commutation/capture interrupt pending 1: Commutation/capture interrupt pending

Note: 1 Loading value FFh in the MISR register resets the PWM generator counter and transfers the compare preload registers in the active registers by generating a U event (PUI bit set to 1). Refer to Timer resynchronization on page 258.

2 When several MTC interrupts are enabled at the same time the BRES instruction must not be used to avoid unwanted clearing of status flags: if a second interrupt occurs while BRES is executed (which performs a read-modify-write sequence) to clear the flag of a first interrupt, the flag of the second interrupt may also be cleared and the corresponding interrupt routine is not serviced. It is thus recommended to use a load instruction to clear the flag, with a value equal to the logical complement of the bit. For instance, to clear the PUI flag:

ld MISR, # 0x7F.

*3 **In autoswitched mode** (SWA = 1 in the MRCA register): As all bits in the MISR register are status flags, they are set by internal hardware signals and must be cleared by software. Any attempt to write them to 1 has no effect (they are read as 0) without interrupt generation.*

***In switched mode** (SWA = 0 in the MRCA register): To avoid losing any interrupts when modifying the RMI and RPI bits the following instruction sequence is recommended:*

ld MISR, # 0x9F; reset both RMI and RPI bits.

ld MISR, # 0xBF; set RMI bit.

ld MISR, # 0xDF; set RPI bit.

Control register A (MCRA)

MCRA Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
MOE	CKE	SR	DAC	V0C1	SWA	PZ	DCB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 126. MCRA register description

Bit	Name	Function
7	MOE	Output enable bit 0: Outputs disabled; MC0[5:0] outputs are put in reset state(1)(2) 1: Outputs enabled; MC0[5:0] outputs enabled

Table 126. MCRA register description (continued)

Bit	Name	Function
6	CKE	Clock enable bit 0: Motor control peripheral clocks disabled 1: Motor control peripheral clocks enabled *Note: 'Clocks disabled' means that all peripheral internal clocks (delay manager, internal sampling clock, PWM generator) are disabled. Therefore, the peripheral can no longer detect events and the preload registers do not operate. When clocks are disabled, write accesses are allowed, so for example, MTIM counter register can be reset by software.* See *Table 127*.
5	SR	Sensor ON/OFF 0: Sensorless mode 1: Position sensor mode See *Table 128*, *Table 133* and *Table 134*.
4	DAC	Direct access to phase state register 0: No direct access (reset value). In this mode the preload value of the MPHST and MCRB registers is taken into account at the C event 1: Direct access enabled. In this mode, write a value in the MPHST register to access the outputs directly See *Table 129*. *Note: In direct access mode (DAC bit is set in MCRA register), a C event is generated as soon as there is a write access to the OO[5:0] bits in MPHST register. In this case, the PWM low/high selection is done by the OS0 bit in the MCRB register.*
3	V0C1	Voltage/current mode 0: Voltage mode 1: Current mode
2	SWA	Switched/autoswitched mode 0: Switched mode 1: Autoswitched mode *Notes:* *1. After reset, in autoswitched mode (SWA = 1), the motor control peripheral is waiting for a C commutation event.* *2. After reset, a C event is immediately generated when CKE and SWA are simultaneously set due to a nil value of MCOMP.*
1	PZ	Protection from parasitic zero-crossing event detection *0: Protection disabled* *1: Protection enabled* *Note: If the PZ bit is set, the Z event filter (ZEF[3:0] in the MZFR register is ignored.*
0	DCB	Data capture bit 0: Use MZPRV (Z_N-1) for multiplication 1: Use MZREG (Z_N) for multiplication See *Table 130*.

1. The reset state is either high impedance, high or low state depending on the corresponding option bit.
2. When the MOE bit in the MCRA register is reset (MCOx outputs in reset state), and the SR bit in the MCRA register is reset (sensorless mode) and the SPLG bit in the MCRC register is reset (sampling at PWM frequency) then, depending on the state of the ZSV bit in the MSCR register, Z event sampling can run or be stopped (and D event is sampled).

Table 162. Tacho edges and input mode selection

TES 1	TES 0	Edge sensitivity	Operating mode
0	0	-	Position sensor or sensorless
0	1	Rising edge	Speed sensor
1	0	Falling edge	
1	1	Rising and falling edges	

Motor Z event filter register (MZFR)

MZFR Reset value: 0000 1111 (0Fh)

7	6	5	4	3	2	1	0
ZEF[3:0]				ZWF[3:0]			
R/W				R/W			

Table 163. MZFR register description

Bit	Name	Function
7:4	ZEF[3:0]	Z event filter bits These bits select the number of valid consecutive Z events (when the Z event is detected) needed to generate the active event. Sampling is done at the selected f_{SCF} frequency (see *Table 164*) or at PWM frequency.
3:0	ZWF[3:0]	Z window filter bits These bits select the length of the blanking window activated at each D event. The filter blanks the Z event detection until the end of the time window (see *Table 165*).

Table 164. Z event filter setting

ZEF3	ZEF2	ZEF1	ZEF0	Z event samples
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 205. EMS test results

Symbol	Parameter	Conditions		Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	Flash/ROM devices	V_{DD} = 5V, T_A = +25°C, f_{OSC} = 8 MHz, LVD OFF, Conforms to IEC 1000-4-2	4A
			V_{DD} = 5V, T_A = +25°C, f_{OSC} = 8 MHz, LVD ON, Conforms to IEC 1000-4-2	2B
V_{FFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{DD} pins to induce a functional disturbance	Flash devices	V_{DD} = 5V, T_A = +25°C, f_{OSC} = 8 MHz, Conforms to IEC 1000-4-4	4A
		ROM devices	V_{DD} = 5V, T_A = +25°C, f_{OSC} = 8 MHz, Conforms to IEC 1000-4-4	3B

12.12 Motor control characteristics

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

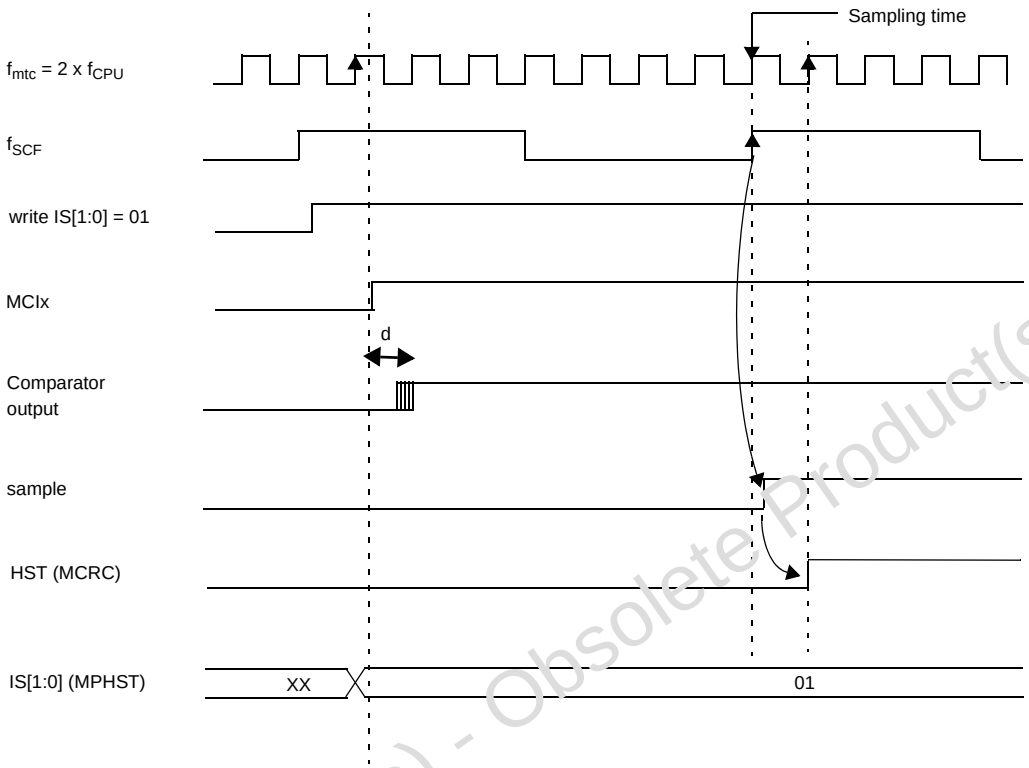
12.12.1 Internal reference voltage

Table 216. Internal reference voltage

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
V_{REF}	Voltage threshold (VR [2:0] = 000)	VR [2:0] = 000		V_{DD}*0.04		V
		Example: V_{DD} - V_{SSA} = 5V		0.2		
	Voltage threshold (VR [2:0] = 001)	VR [2:0] = 001		V_{DD}*0.12		
		Example: V_{DD} - V_{SSA} = 5V		0.6		
	Voltage threshold (VR [2:0] = 010)	VR [2:0] = 010		V_{DD}*0.2		
		Example: V_{DD} - V_{SSA} = 5V		1.0		
	Voltage threshold (VR [2:0] = 011)	VR [2:0] = 011		V_{DD}*0.3		
		Example: V_{DD} - V_{SSA} = 5V		1.5		
	Voltage threshold (VR [2:0] = 100)	VR [2:0] = 100		V_{DD}*0.4		
		Example: V_{DD} - V_{SSA} = 5V		2.0		
	Voltage threshold (VR [2:0] = 101)	VR [2:0] = 101		V_{DD}*0.5		
		Example: V_{DD} - V_{SSA} = 5V		2.5		
	Voltage threshold (VR [2:0] = 110)	VR [2:0] = 110		V_{DD}*0.7		
		Example: V_{DD} - V_{SSA} = 5V		3.5		
$\Delta V_{REF}/V_{REF}$	Tolerance on V_{REF}			2.5	10	%

1. Unless otherwise specified, typical data are based on T_A = 25°C and V_{DD} - V_{SS} = 5V. They are given only as design guidelines and are not tested.

Figure 155. Example 5: Waveforms for sensor HST update timing diagram for a newly selected phase input



Sampling of sensor input is done at f_{SCF}, so after writing IS[1:0] in the MPHST register for input selection, you have to wait:

1) $1/f_{mtc}$ to resynchronize the data and set the MCIx bit
2) 100ns corresponding to the comparator and multiplexer propagation delay (d)
3) $1/f_{SCF}$ to sample the comparator output
4) $1/f_{mtc}$ to resynchronize the data and set the HST bit

Example with $f_{PERIPH} = f_{mtc}$ = 4 MHz:

SCF[1:0]	00	01	10	11
f_{SCF}	1 MHz	500 kHz	250 kHz	125 kHz
Secure waiting time to read HST	2µs	3µs	5µs	9µs