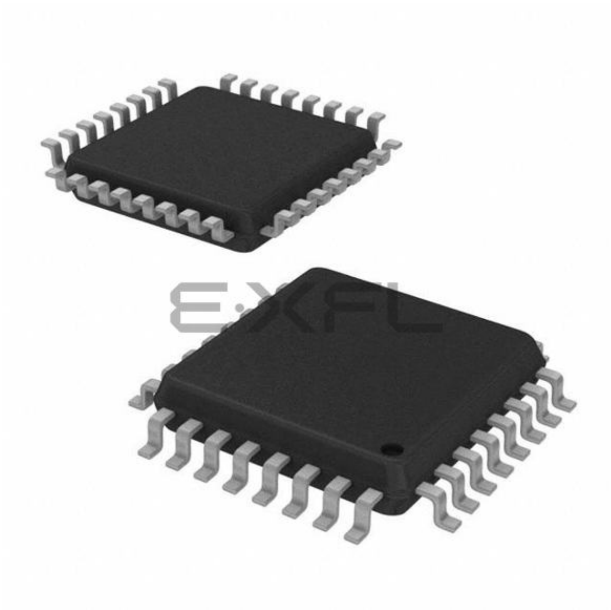


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	LINbusSCI
Peripherals	LVD, Motor Control PWM, POR, PWM, WDT
Number of I/O	17
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7fmc1k6tce

Contents

Table 2. Device pin description[1] (continued)

Pin number		Pin name	Type	Level		Port						Main function (after reset)	Alternate function[2]	
						Input				Output				
LQFP44	LQFP32			Input	Output	float	wpu	int[3]	ana	OD	PP			
9	7	PA3/PWM0/AIN0	I/O	C_T		X	ei1		X	X	X	Port A3	PWM output 0	ADC analog input 0
(5)	(5)	PA4 (HS)/ARTCLK	I/O	C_T	HS	X	X			X	X	Port A4	PWM-ART external clock	
10	8	PA5/ARTIC1/AIN1	I/O	C_T		X		ei1	X	X	X	Port A5	PWM-ART input capture 1	ADC analog input 1
(5)	(5)	PA6/ARTIC2	I/O	C_T		X	ei1			X	X	Port A6	PWM-ART input capture 2	
		PA7/AIN2	I/O	C_T		X		ei1	X	X	X	Port A7	ADC analog input 2	
11	9	PB0/MCVREF	I/O	C_T		X	X		X	X	X	Port B0	MTC voltage reference	
12	10	PB1/MCIA	I/O	C_T		X	X		X	X	X	Port B1	MTC input A	
13	11	PB2/MCIB	I/O	C_T		X	X		X	X	X	Port B2	MTC input B	
14	12	PB3/MCIC	I/O	C_T		X	X		X	X	X	Port B3	MTC input C	
15	(5)	PB4/MISO	I/O	C_T		X	X			X	X	Port B4	SPI master in/slave out data	
16		PB5/MOSI/AIN3	I/O	C_T		X	X			X	X	Port B5	SPI master out/slave in data	ADC analog input 3
17		PB6/SCK	I/O	C_T	HS	X	ei2			X	X	Port B6	SPI serial clock	
18		PB7/SS/AIN4	I/O	C_T	HS	X		ei2		X	X	Port B7	SPI slave select (active low)	ADC analog input 4
(5)		PG4	I/O	T_T		X	X			X	X	Port G4		
		PG5	I/O	T_T		X	X			X	X	Port G5		
		PG6	I/O	T_T		X	X			X	X	Port G6		
		PG7	I/O	T_T		X	X			X	X	Port G7		
		PC0	I/O	C_T	HS	X		ei2		X	X	Port C0		
(5)	(5)	PC1/MCCFI0[8]/AIN5	I/O	C_T		X	ei2		X	X	X	Port C1	MTC current feedback input 0[8]	ADC analog input 5
19	13	PC2/OAP	I/O	C_T		X		ei2	X	X	X	Port C2	Op-amp positive input	
20	14	PC3/OAN	I/O	C_T		X	X	ei2	X	X	X	Port C3	Op-amp negative input	

4.6 IAP (in-application programming)

This mode uses a Bootloader program previously stored in Sector 0 by the user (in ICP mode or by plugging the device in a programming tool).

This mode is fully controlled by user software. This allows it to be adapted to the user application, (user-defined strategy for entering programming mode, choice of communications protocol used to fetch the data to be stored, etc.). For example, it is possible to download code from the SPI, SCI or other type of serial interface and program it in the Flash. IAP mode can be used to program any of the Flash sectors except Sector 0, which is write/erase protected to allow recovery in case errors occur during the programming operation.

4.7 Related documentation

For details on Flash programming and ICC protocol, refer to the *ST7 Flash Programming Reference Manual* and to the *ST7 ICC Protocol Reference Manual*.

4.8 Flash control status register (FCSR)

FCSR Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
0							
R/W							

This register is reserved for use by programming tool software. It controls the Flash programming and erasing operations.

6.3 Oscillator

The main clock of the ST7 can be generated by a crystal or ceramic resonator oscillator or an external source.

The associated hardware configurations are shown in *Table 6*. Refer to the electrical characteristics section for more details.

6.3.1 External clock source

In this external clock mode, a clock signal (square, sinus or triangle) with ~50% duty cycle has to drive the OSC1 pin while the OSC2 pin is not connected.

Crystal/ceramic oscillators

This family of oscillators has the advantage of producing a very accurate rate on the main clock of the ST7. In this mode, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time.

This oscillator is not stopped during the reset phase to avoid losing time in its start-up phase. See *Section 12: Electrical characteristics* for more details.

Note: When crystal oscillator is used as a clock source, a risk of failure may exist if no series resistors are implemented.

Table 6. ST7 clock sources

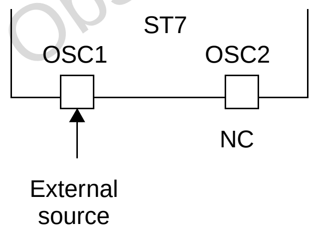
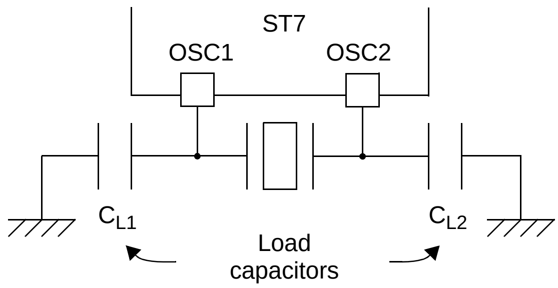
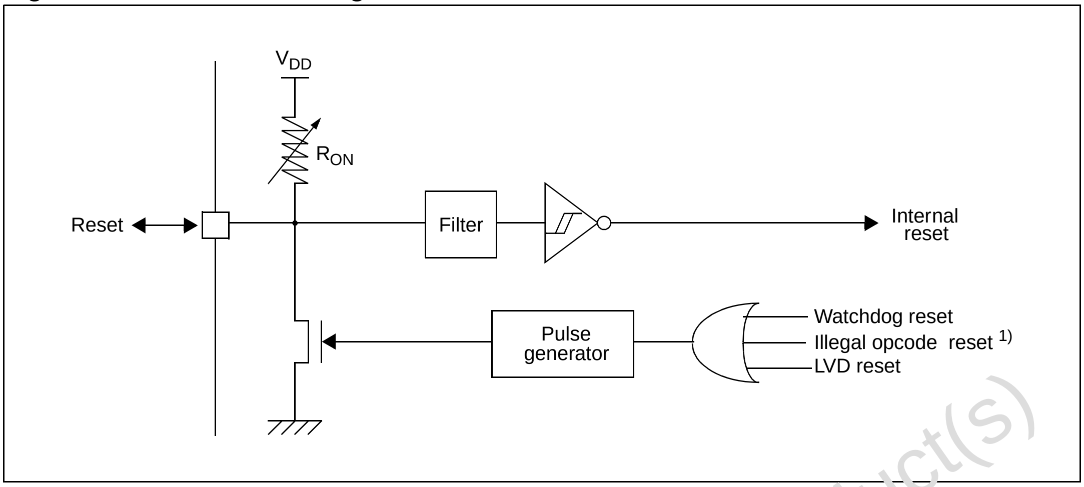
	Hardware configuration
External clock	
Crystal/ceramic resonators	

Figure 11. Reset block diagram



1. See *Section 11.2.2: Illegal opcode reset on page 309* for more details on illegal opcode reset conditions.

The $\overline{\text{RESET}}$ pin is an asynchronous signal which plays a major role in EMS performance. In a noisy environment, it is recommended to follow the guidelines mentioned in the electrical characteristics section.

6.4.3 External power-on reset

If the LVD is disabled by option byte, to start up the microcontroller correctly, the user must ensure by means of an external reset circuit that the reset signal is held low until V_{DD} is over the minimum level specified for the selected f_{OSC} frequency.

A proper reset signal for a slow rising V_{DD} supply can generally be provided by an external RC network connected to the $\overline{\text{RESET}}$ pin.

6.4.4 Internal low voltage detector (LVD) reset

Two different reset sequences caused by the internal LVD circuitry can be distinguished:

- Power-on reset
- Voltage drop reset

The device $\overline{\text{RESET}}$ pin acts as an output that is pulled low when $V_{DD} < V_{IT+}$ (rising edge) or $V_{DD} < V_{IT-}$ (falling edge) as shown in *Figure 12*.

The LVD filters spikes on V_{DD} larger than $t_{g(VDD)}$ to avoid parasitic resets.

6.4.5 Internal watchdog reset

The RESET sequence generated by a internal watchdog counter overflow is shown in *Figure 12*.

Starting from the Watchdog counter underflow, the device $\overline{\text{RESET}}$ pin acts as an output that is pulled low during at least $t_{w(RSTL)out}$.

9.5 Interrupts

The external interrupt event generates an interrupt if the corresponding configuration is selected with DDR and OR registers and the interrupt mask in the CC register is not active (RIM instruction).

Table 28. I/O port interrupt control/wake-up capability

Interrupt event	Event flag	Enable control bit	Exit from WAIT	Exit from HALT
External interrupt on selected external event	-	DDRx, ORx	Yes	

9.5.1 I/O port implementation

The I/O port register configurations are summarized below.

Standard ports

Table 29. Standard ports: PA4, PA2:0, PB5:0, PC7:4, PD7:6, PE5:0, PF5:0, PG7:0, PH7:0

Mode	DDR	OR
Floating input	0	0
Pull-up input	0	1
Open drain output	1	0
Push-pull output	1	1

Interrupt ports

Table 30. Interrupt ports with pull-up: PA6, PA3, PB6, PC3, PC1, PD5, PD4, PD2

Mode	DDR	OR
Floating input	0	0
Pull-up interrupt input	0	1
Open drain output	1	0
Push-pull output	1	1

Table 31. Interrupt ports without pull-up: PA7, PA5, PB7, PC2, PC0, PD6, PD3, PD

Mode	DDR	OR
Floating input	0	0
Floating interrupt input	0	1
Open drain output	1	0
Push-pull output	1	1

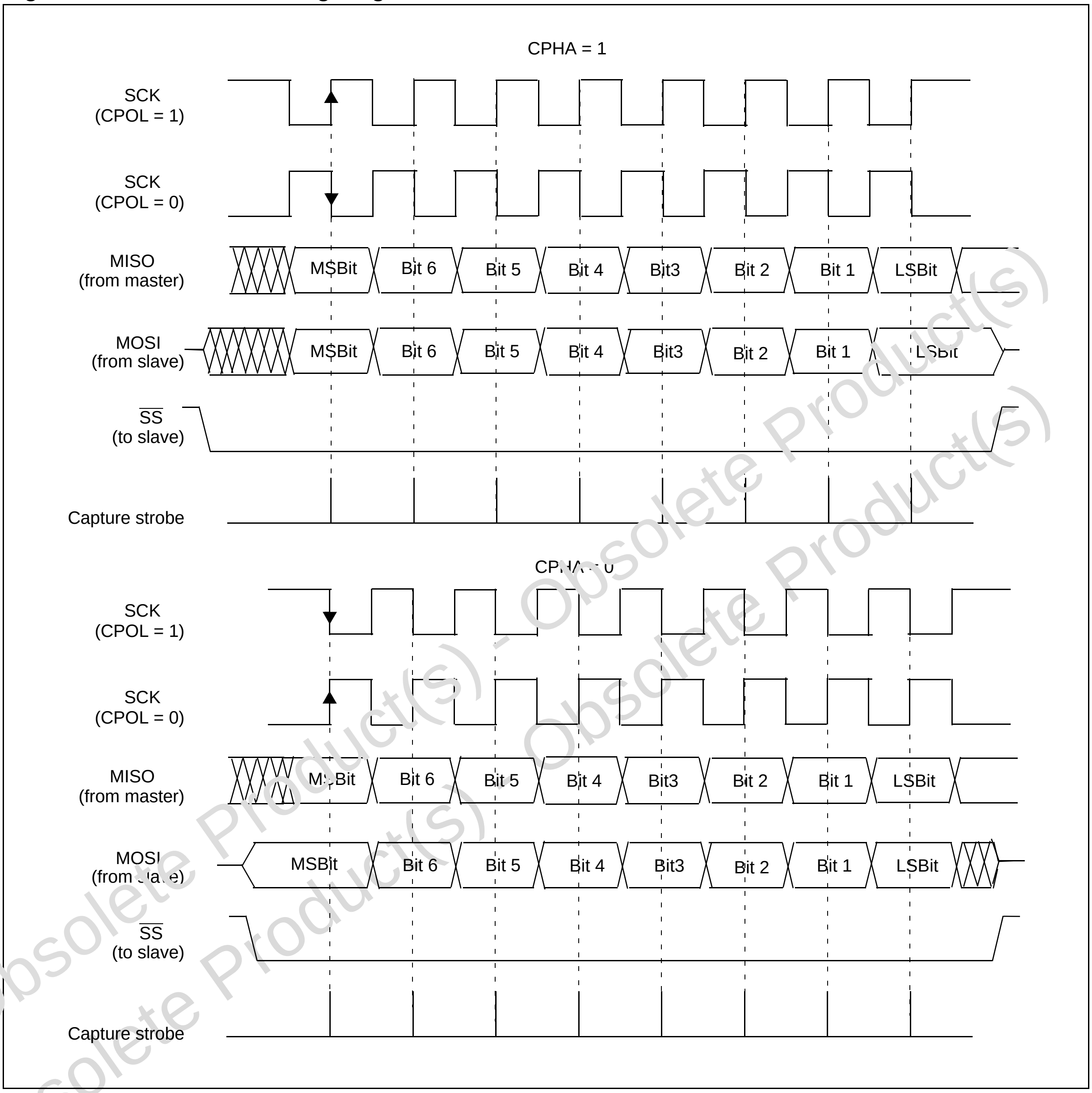
9.6 I/O port register map and reset values

Table 33. I/O port register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
Reset value of all I/O port registers		0	0	0	0	0	0	0	0
0000h	PADR	MSB							LSB
0001h	PADDR								
0002h	PAOR								
0003h	PBDR	MSB							LSB
0004h	PBDDR								
0005h	PBOR								
0006h	PCDR	MSB							LSB
0007h	PCDDR								
0008h	PCOR								
0009h	PDDR	MSB							LSB
000Ah	PDDDR								
000Bh	PDOR								
000Ch	PEDR	MSB							LSB
000Dh	PEDDR								
000Eh	PEOR								
000Fh	PFDR	MSB							LSB
0010h	PFDDR								
0011h	PFOR								
0012h	PGDR	MSB							LSB
0013h	PGDDR								
0014h	PGOR								
0015h	PHDR	MSB							LSB
0016h	PHDDR								
0017h	PHOR								

If CPOL is changed at the communication byte boundaries, the SPI must be disabled by resetting the SPE bit.

Figure 58. Data clock timing diagram



1. This figure should not be used as a replacement for parametric information. Refer to *Section 12: Electrical characteristics*.

Table 62. SCISR register description (continued)

Bit	Name	Function
3	OR	Overrun error The OR bit is set by hardware when the word currently being received in the shift register is ready to be transferred into the RDR register whereas RDRF is still set. An interrupt is generated if RIE = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register). 0: No Overrun error 1: Overrun error detected *Note: When this bit is set, RDR register contents are not lost but the shift register is overwritten.*
2	NF	Character noise flag This bit is set by hardware when noise is detected on a received character. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register). 0: No noise 1: Noise is detected *Note: This bit does not generate interrupt as it appears at the same time as the RDRF bit which itself generates an interrupt.*
1	FE	Framing error This bit is set by hardware when a desynchronization, excessive noise or a break character is detected. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register). 0: No framing error 1: Framing error or break character detected *Note: This bit does not generate an interrupt as it appears at the same time as the RDRF bit which itself generates an interrupt. If the word currently being transferred causes both a frame error and an overrun error, it is transferred and only the OR bit is set.*
0	PE	Parity error This bit is set by hardware when a byte parity error occurs (if the PCE bit is set) in receiver mode. It is cleared by a software sequence (a read to the status register followed by an access to the SCIDR data register). An interrupt is generated if PIE = 1 in the SCICR1 register. 0: No parity error 1: Parity error detected

SCI control register 1 (SCICR1)

SCICR1 Reset value: x000 0000 (x0h)

7	6	5	4	3	2	1	0
R8	T8	SCID	M	WAKE	PCE(1)	PS	PIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

1. This bit has a different function in LIN mode; please refer to *Section 10.5.10: LIN mode registers*

Examples of LHL coding:

Example 1: LHL = 33h = 001100 11b

LHL(7:3) = 1100b = 12d

LHL(1:0) = 11b = 3d

This leads to:

Mantissa (57 - T_{HEADER}) = 12d

Fraction (57 - T_{HEADER}) = 3/4 = 0.75

Therefore:

(57 - T_{HEADER}) = 12.75d and T_{HEADER} = 44.25d

Example 2:

57 - T_{HEADER} = 36.21d

LHL(1:0) = rounded(4*0.21d) = 1d

LHL(7:2) = Mantissa (36.21d) = 36d = 24h

Therefore LHL(7:0) = 10010001 = 91h

Example 3:

57 - T_{HEADER} = 36.90d

LHL(1:0) = rounded(4*0.90d) = 4d

The carry must be propagated to the matissa:

LHL(7:2) = Mantissa (36.90d) + 1 = 37d

Therefore LHL(7:0) = 10110000 = A0h

SCI register map and reset values

Table 79. SCI register map and reset values

Addr. (Hex.)	Register name	7	6	5	4	3	2	1	0
0018h	SCI1SR Reset value	TDRE 1	TC 1	RDRF 0	IDLE 0	OR/LHE 0	NF 0	FE 0	PE 0
0019h	SCI1DR Reset value	DR7 -	DR6 -	DR5 -	DR4 -	DR3 -	DR2 -	DR1 -	DR0 -
001Ah	SCI1BRR LPR (LIN slave mode) Reset value	SCP1 LPR7 0	SCP0 LPR6 0	SCT2 LPR5 0	SCT1 LPR4 0	SCT0 LPR3 0	SCR2 LPR2 0	SCR1 LPR1 0	SCR0 LPR0 0
001Bh	SCI1CR1 Reset value	R8 x	T8 0	SCID 0	M 0	WAKE 0	PCE 0	PS 0	PIE 0
001Ch	SCI1CR2 Reset value	TIE 0	TCIE 0	RIE 0	ILIE 0	TE 0	RE 0	RWU 0	SBK 0
001Dh	SCI1CR3 Reset Value	LDUM 0	LINE 0	LSLV 0	LASE 0	LHDM 0	LHIE 0	LHDF 0	LSF 0
001Eh	SCI1ERPR LHLR (LIN slave mode) Reset value	ERPR LHL7 0	ERPR LHL6 0	ERPR LHL5 0	ERPR LHL4 0	ERPR3 LHL3 0	ERPR LHL2 0	ERPR LHL1 0	ERPR LHL0 0
001Fh	SCI1TPR LPRF (LIN slave mode) Reset value	ETPR7 0 0	ETPR6 0 0	ETPR5 0 0	ETPR4 0 0	ETPR3 LPRF3 0	ETPR2 LPRF2 0	ETPR1 LPRF1 0	ETPR0 LPRF0 0

Table 85. D event filter setting (continued)

DEF3	DEF2	DEF1	DEF0	D event limit	SR = 1
1	1	1	0	15	No D event filter
1	1	1	1	16	

Z event detection

In sensorless mode, the Z window filter becomes active after each D event. It blanks out the Z event during the time window defined by the ZWF[3:0] bits in the MZFR register (see *Table 86*). The reset value is 200µs. This window filter becomes active after both hardware and software D events.

The Z event filter becomes active after the Z window filter. It counts the number of consecutive Z events up to a limit defined by the ZEF[3:0] bits in the MZFR register. The reset value is 1. The Z bit is set when the counter limit is reached.

Sampling is done at a selectable frequency (f_{SCF}), see *Table 166*.

The Z event filter is active only for a hardware Z event (Z_H). For a simulated (Z_S) event, it is forced to 1. Z event filter is also active in sensor mode.

Figure 81. Z window and event filter flowchart

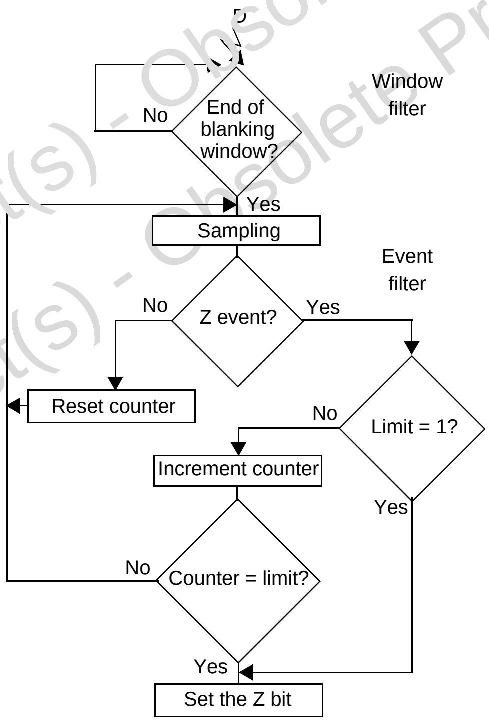
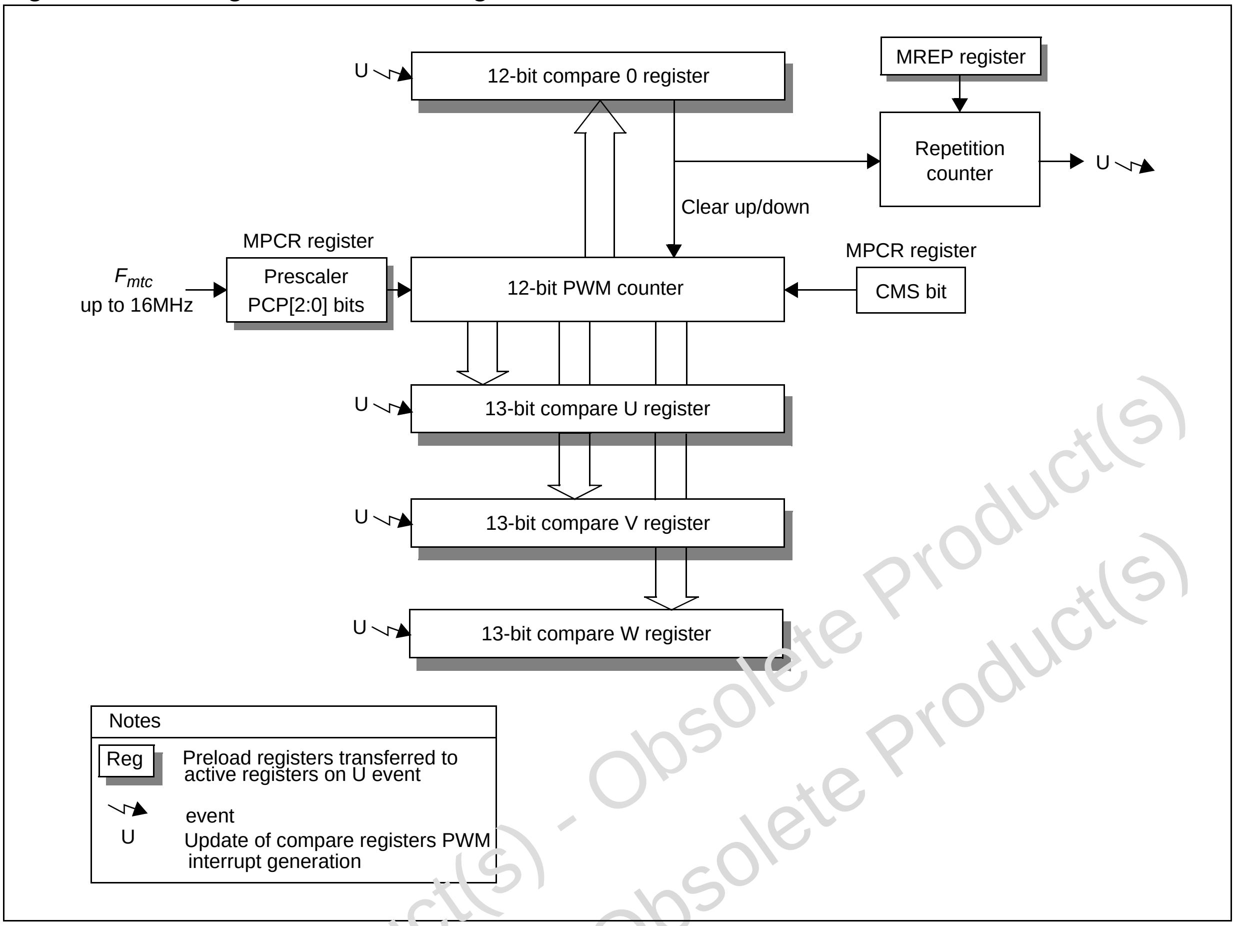


Figure 118. PWM generator block diagram



Functional description

The three PWM signals are generated using a free-running 12-bit PWM counter and three 13-bit compare registers for phase U, V and W: MCMPU, MCMPV and MCMPW registers respectively.

A fourth 12-bit register is needed to set-up the PWM carrier frequency: MCMP0 register.

Each of these compare registers is buffered with a preload register. Transfer from preload to active registers is done synchronously with PWM counter underflow or overflow depending on configuration. This allows compare values to be written without risks of spurious PWM transitions.

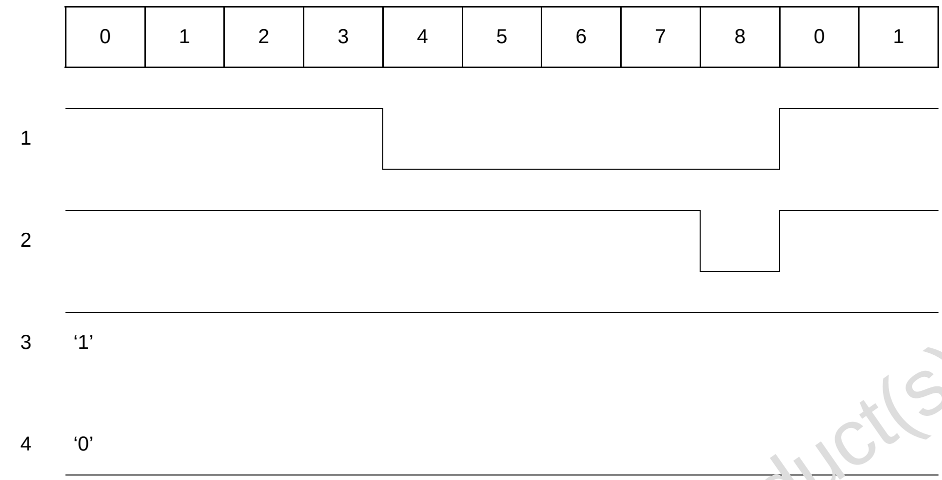
The block diagram of the PWM generator is shown in *Figure 118*.

Prescaler

The 12-bit PWM counter clock is supplied through a 3-bit prescaler to allow the generation of lower PWM carrier frequencies. It divides F_{mtc} by 1, 2, 3, ..., 8 to get $F_{mtc\text{-}pwm}$.

This prescaler is accessed through three bits PCP[2:0] in MPCR register; this register is buffered: the new value is taken into account after a PWM update event.

Figure 121. Edge-aligned PWM waveforms (compare 0 register = 8)



12-bit mode (PMS bit = 0 in the MPCR register)

This mode is useful for MCMP0 values ranging from 9 bits to 12 bits. *Figure 122* presents the way compare 0 and compare U, V, W should be loaded. It requires loading two bytes in the MCMPxH and MCMPxL registers (that is, MCMP0, MCMPU, MCMPV and MCMPW 16-bit registers) following the sequence described below:

- write to the MCMPxL register (LSB) first
- then write to the MCMPxH register (MSB).

The 16-bit value is then ready to be transferred in the active register as soon as an update event occurs. This sequence is necessary to avoid potential conflicts with update interrupts causing the hardware transfer from preload to active registers: if an update event occurs in the middle of the above sequence, the update is effective only when the MSB has been written.

8-bit PWM mode (PMS bit = 1 in MPCR register)

This mode is useful whenever the MCMP0 value is less than or equal to 8-bits. It allows significant CPU resource savings when computing three-phase duty cycles during PWM interrupt routines. In this mode, the compare 0 and compare U, V, W registers have the same size (8 bits). The extension of the MCMPx registers is done in using the OVFx bits in the MPCR register (refer to *Figure 122*). These bits force the related duty-cycles to 100% and are reset by hardware on occurence of a PWM update event.

Note: ***Read access to registers with preload****: During read accesses, values read are the content of the preload registers, not the active registers.*

Note: ***Compare register active bit locations****: The 13 active bits of the MCMPx registers are left-aligned. This allows temporary calculations to be done with 16-bit precision, round-up is done automatically to the 13-bit format when loading the values of the MCMPx registers.*

Note: ***MCMP0x registers****: The configuration MCMP0H = MCMP0L = 0 is not allowed.*

A_N weight register (MWGHT)

MWGHT Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
AN[7:0]							
R/W							

Table 122. MWGHT register description

Bit	Name	Function
7:0	AN[7:0]	A weight value These bits contain the A_N weight value for the multiplier. In autoswitched mode the MCOMP register is automatically loaded when a Z event occurs (see *Equation 10*).

Equation 10

$$\frac{Zn \times MWGHT}{256(d)} \text{ or } \frac{Zn-1 \times MWGHT}{256(d)} \quad (*)$$

where (*) depends on the DCB bit in the MCRA register.

Prescaler and sampling register (MPRSR)

MPRSR Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
SA[3:0]				ST[3:0]			
R/W				R/W			

Table 123. MPRSR register description

Bit	Name	Function
7:4	SA[3:0]	Sampling ratio These bits contain the sampling ratio value for current mode. Refer to *Table 105: Sampling frequency selection on page 238*.
3:0	ST[3:0]	Step ratio These bits contain the step ratio value. It acts as a prescaler for the MTIM timer and is auto incremented/decremented with each R+ or R- event. Refer to *Table 98: Step frequency/period range (4 MHz) on page 226* and *Table 99: modes of accessing mtim timer-related registers on page 226*.

Table 138. MCFR register description (continued)

Bit	Name	Function
2:0	CFW[2:0]	Current window filter bits These bits select the length of the blanking window activated each time PWM is turned on(2): 000: blanking window = off 001: blanking window = 0.5µs 010: blanking window = 1µs 011: blanking window = 1.5µs 100: blanking window = 2µs 101: blanking window = 2.5µs 110: blanking window = 3µs 111: blanking window = 3.5µs The filter blanks the output of the current comparator.

1. Sampling is done at $f_{PERIPH}/4$.
2. Times are indicated for 4 MHz f_{PERIPH}.

Motor D event filter register (MDFR)

MDFR Reset value: 0000 1111 (0Fh)

7	6	5	4	3	2	1	0
DEF[3:0]				DWF[3:0]			
R/W				R/W			

Table 139. MDFR register description

Bit	Name	Function
7:4	DEF[3:0]	D event filter bits These bits select the number of valid consecutive D events (when the D event is detected) needed to generate the active event. See *Table 140*.
3:0	DWF[3:0]	D window filter bits These bits select the length of the blanking window activated at each C event. The filter blanks the D event detection. See *Table 141*.

Table 140. D event filter setting(1)

DEF3	DEF2	DEF1	DEF0	D event samples	SR = 1
0	0	0	0	1	No D event filter
0	0	0	1	2	
0	0	1	0	3	
0	0	1	1	4	
0	1	0	0	5	
0	1	0	1	6	
0	1	1	0	7	
0	1	1	1	8	
1	0	0	0	9	

**Warning: Access to preload registers: Special care has to be taken with preload registers, especially when using the ST7 BSET and BRES instructions on MTC registers.
For instance, while writing to the MPHST register, the value in the preload register is written. However, while reading at the same address, the current value in the register and not the value of the preload register is obtained.
Excepted for three-phase PWM generator's registers, all preload registers are loaded in the active registers at the same time. In normal mode this is done automatically when a C event occurs, however in direct access mode (DAC bit = 1) the preload registers are loaded as soon as a value is written in the MPHST register.**

Caution: **Access to write-once bits:** Special care has to be taken with write-once bits in MPOL and MDTG registers; these bits have to be first accessed during the set-up. Any access to the other bits (not write-once) through a BRES or a BSET instruction locks the content of write-once bits (no possibility for the core to distinguish individual bit access: Read/write internal signal acts on a whole register only). This protection is then only unlocked after a processor hardware reset.

Deadtime generator register (MDTG)

MDTG Reset value: 1111 1111 (FFh)

7	6	5	4	3	2	1	0
PCN	DTE	DTG[5:0]					
R/W	(1)	Write once only					

1. Write once-only bit if PCN bit is set, read/write if PCN bit is reset.

10.7.5 Op-amp programming

The flowchart for op-amp operation is shown in *Figure 127*.

Figure 127. Normal op-amp operation

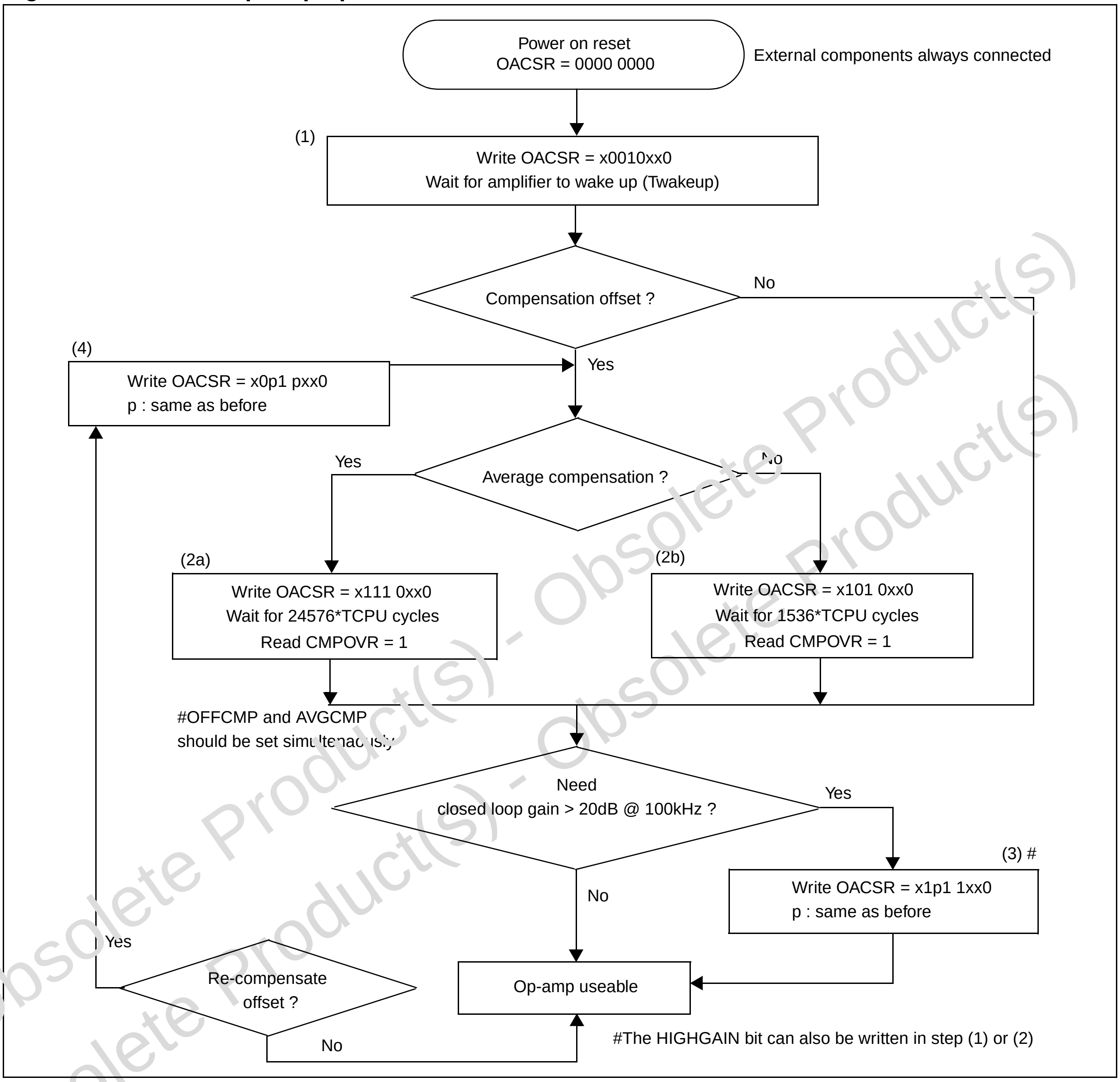
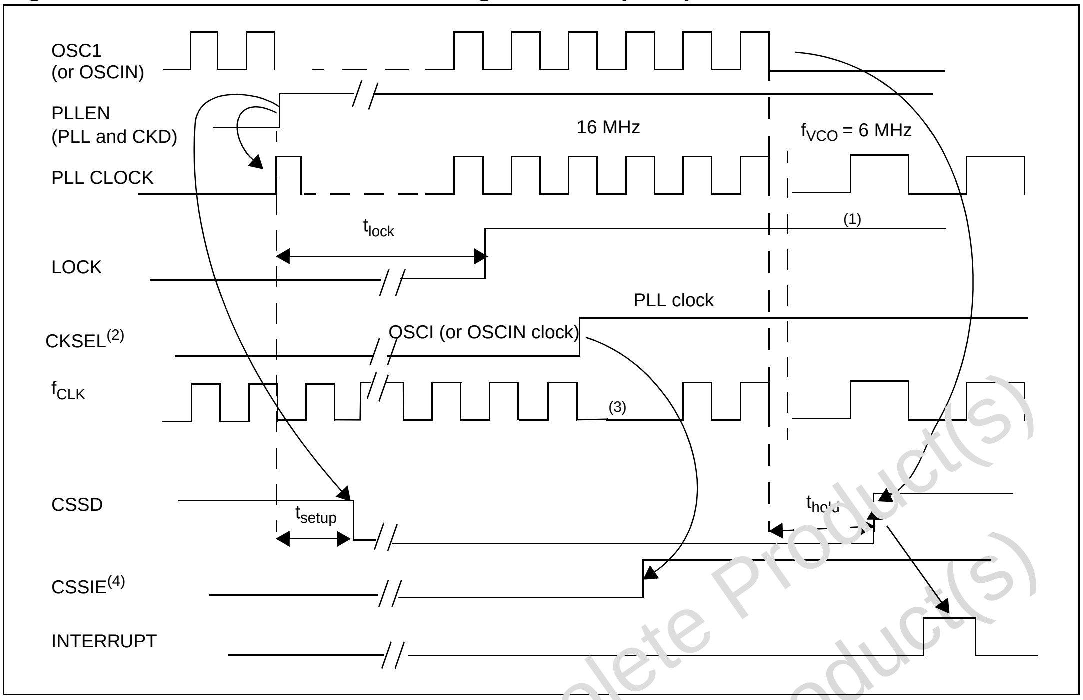


Figure 138. PLL and clock detector signal start up sequence



1. Lock does not go low without resetting the PLLEN bit.
2. Before setting the CKSEL bit by software in order to switch to the PLL clock, a period of t_{lock} must have elapsed.
3. 2 clock cycles are missing after CKSEL = 1.
4. CKSEL bit must be set before enabling the CSS interrupt (CSSIE = 1).

12.6 Memory characteristics

12.6.1 RAM and hardware registers

Table 203. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode(1)	Halt mode (or reset)	1.6			V

1. Minimum V_{DD} supply voltage without losing data stored in RAM (in Halt mode or under RESET) or in hardware registers (only in Halt mode). Not tested in production.

13 Package characteristics

13.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

13.2 LQFP packages

The following pages contain the package drawings and mechanical data as well as the thermal characteristics and soldering information for the 44- and 32-pin LQFP packages.