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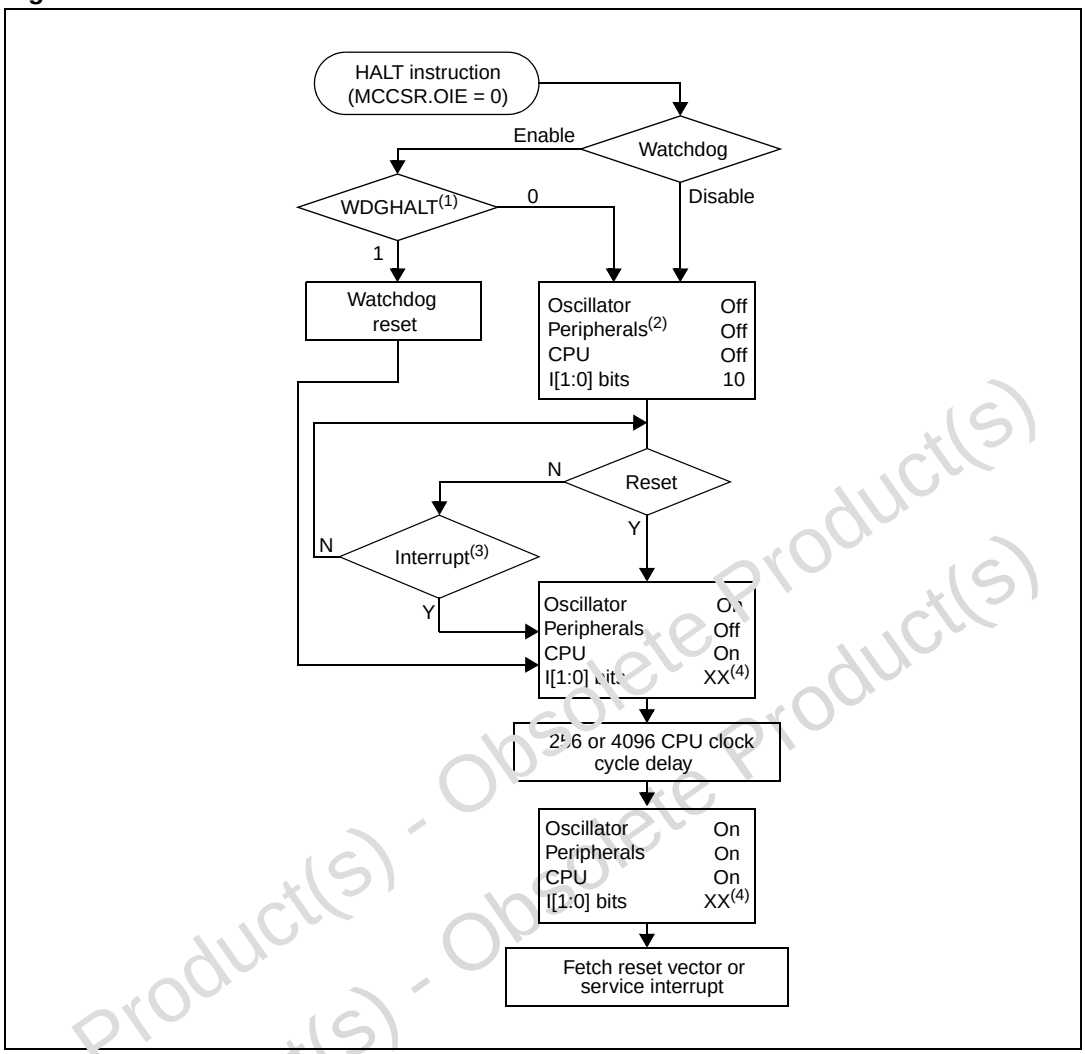
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	LINbusSCI, SPI
Peripherals	LVD, Motor Control PWM, POR, PWM, WDT
Number of I/O	26
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7fmc2s4tce

Table 2. Device pin description[1] (continued)

Pin number		Pin name	Type	Level		Port						Main function (after reset)	Alternate function[2]	
						Input				Output				
LQFP44	LQFP32			Input	Output	float	wpu	int[3]	ana	OD	PP			
29	21	PD0/OCMP2_A/ MCPWMW[10]/AIN11	I/O	C_T		X			X	X	X	Port D0	Timer A output compare 2	
													MTC PWM output W[10]	
													ADC analog input 11	
30	22	PD1(HS)/OCMP1_A/ MCPWMV[10]/ MCDEM[11]	I/O	C_T	HS	X		ei0		X	X	Port D1	Timer A output compare 1	
													MTC PWM output V[10]	
													MTC demagnetization[11]	
31	23	PD2/ICAP2_A/ MCZEM[11]/AIN12	I/O	C_T		X		ei0		X	X	Port D2	Timer A input capture 2	
													MTC BEMF[11]	
													ADC analog input 12	
32	24	PD3/ICAP1_A/AIN13	I/O	C_T		X		ei0		X	X	Port D3	Timer A input capture 1	ADC analog input 13
33	25	PD4/EXTCLK_A/ICCCLK/ AIN14	I/O	C_T		X		ei0		X	X	Port D4	Timer A external clock source	
													ICC clock output	
													ADC analog input 14	
34	26	PD5/ICCDATA/AIN15	I/O	C_T		X		ei0		X	X	Port D5	ICC data input	
													ADC analog input 15	
35	27	PD6/RDI	I/O	C_T	HS	X		ei0		X	X	Port D6	SCI receive data in	
36	28	PD7/TDO	I/O	C_T	HS	X	X			X	X	Port D7	SCI transmit data output	
(5)	(5)	V_{SS_2}[7]	S									Digital ground voltage		
		V_{DD_2}[7]	S									Digital main supply voltage		
		PH4	I/O	T_T		X	X			X	X	Port H4		
		PH5	I/O	T_T		X	X			X	X	Port H5		
		PH6	I/O	T_T		X	X			X	X	Port H6		

Figure 27. Halt mode flowchart



1. WDGHALT is an option bit. See option byte section for more details.
2. Peripherals clocked with an external clock source can still be active.
3. Only some specific interrupts can exit the MCU from Halt mode (such as external interrupt). Refer to *Table 22: Interrupt mapping on page 70* for more details.
4. Before servicing an interrupt, the CC register is pushed on the stack. The I[1:0] bits of the CC register are set to the current software priority level of the interrupt routine and recovered when the CC register is popped.

Table 44. ARTICCSR register description

Bit	Name	Function
7:6	-	Reserved, must be kept cleared.
5:4	CS[2:1]	Capture sensitivity These bits are set and cleared by software. They determine the trigger event polarity on the corresponding input capture channel. 0: Falling edge triggers capture on channel x 1: Rising edge triggers capture on channel x
3:2	CIE[2:1]	Capture interrupt enable These bits are set and cleared by software. They enable or disable the input capture channel interrupts independently. 0: Input capture channel x interrupt disabled 1: Input capture channel x interrupt enabled
1:0	CF[2:1]	Capture flag These bits are set by hardware and cleared by software reading the corresponding ARTICRx register. Each CFx bit indicates that an input capture x has occurred. 0: No input capture on channel x 1: An input capture has occurred on channel x

ART input capture registers (ARTICRx)

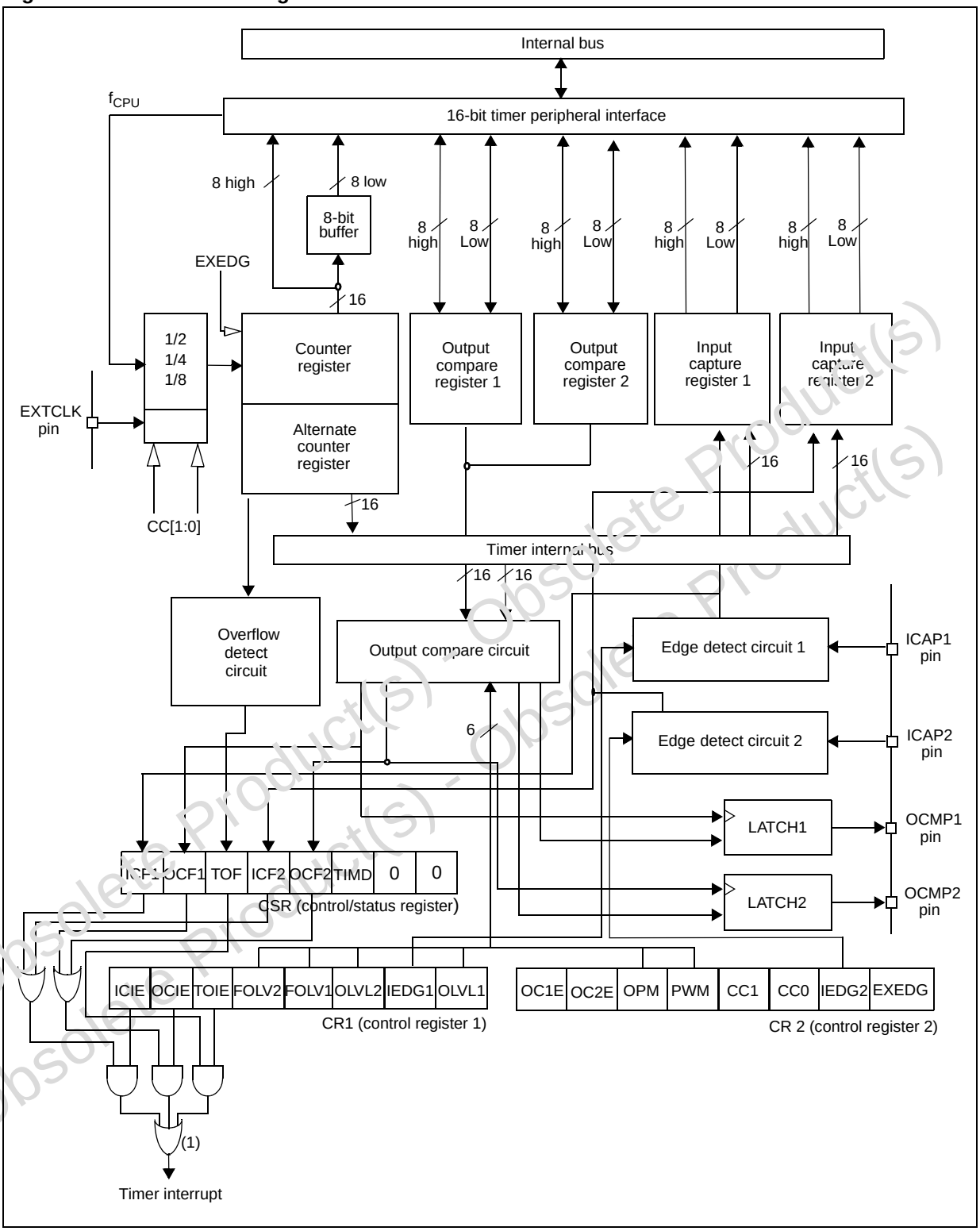
ARTICRx Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
IC[7:0]							
RO							

Table 45. ARTICRx register description

Bit	Name	Function
7:0	IC[7:0]	Input capture data These read-only bits are set and cleared by hardware. An ARTICRx register contains the 8-bit auto-reload counter value transferred by the input capture channel x event.

Figure 40. Timer block diagram



1. If IC, OC and TO interrupt requests have separate vectors then the last OR is not present (see *Table 22: Interrupt mapping*)

Table 50. CR1 register description

Bit	Name	Function
7	ICIE	Input capture interrupt enable 0: Interrupt is inhibited 1: A timer interrupt is generated whenever the ICF1 or ICF2 bit of the SR register is set
6	OCIE	Output compare interrupt enable 0: Interrupt is inhibited 1: A timer interrupt is generated whenever the OCF1 or OCF2 bit of the SR register is set
5	TOIE	Timer overflow interrupt enable 0: Interrupt is inhibited 1: A timer interrupt is enabled whenever the TOF bit of the SR register is set
4	FOLV2	Forced output compare 2 This bit is set and cleared by software. 0: No effect on the OCMP2 pin 1: Forces the OLVL2 bit to be copied to the OCMP2 pin, if the OC2E bit is set and even if there is no successful comparison
3	FOLV1	Forced output compare 1 This bit is set and cleared by software. 0: No effect on the OCMP1 pin 1: Forces OLVL1 to be copied to the OCMP1 pin, if the OC1E bit is set and even if there is no successful comparison
2	OLVL2	Output level 2 This bit is copied to the OCMP2 pin whenever a successful comparison occurs with the OC2R register and OCxE is set in the CR2 register. This value is copied to the OCMP1 pin in one pulse mode and pulse width modulation mode.
1	IEDG1	Input edge 1 This bit determines which type of level transition on the ICAP1 pin triggers the capture. 0: A falling edge triggers the capture 1: A rising edge triggers the capture
0	OLVL1	Output level 1 The OLVL1 bit is copied to the OCMP1 pin whenever a successful comparison occurs with the OC1R register and the OC1E bit is set in the CR2 register.

Table 52. CSR register description (continued)

Bit	Name	Function
3	OCF2	Output compare flag 2 0: No match (reset value) 1: The content of the free running counter has matched the content of the OC2R register. To clear this bit, first read the SR register, then read or write the low byte of the OC2R (OC2LR) register.
2	TIMD	Timer disable This bit is set and cleared by software. When set, it freezes the timer prescaler and counter and disabled the output functions (OCMP1 and OCMP2 pins) to reduce power consumption. Access to the timer registers is still available, allowing the timer configuration to be changed while it is disabled. 0: Timer enabled 1: Timer prescaler, counter and outputs disabled
1:0	-	Reserved, must be kept cleared

Input capture 1 high register (IC1HR)

This is an 8-bit read-only register that contains the high part of the counter value (transferred by the input capture 1 event).

IC1HR — Reset value: undefined

7	6	5	4	3	2	1	0
MSB							LSB
RO	RO	RO	RO	RO	RO	RO	RO

Input capture 1 low register (IC1LR)

This is an 8-bit read only register that contains the low part of the counter value (transferred by the input capture 1 event).

IC1LR — Reset value: undefined

7	6	5	4	3	2	1	0
MSB							LSB
RO	RO	RO	RO	RO	RO	RO	RO

Output compare 1 high register (OC1HR)

This is an 8-bit register that contains the high part of the value to be compared to the CHR register.

OC1HR — Reset value: 1000 0000 (80h)

7	6	5	4	3	2	1	0
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Output compare 1 low register (OC1LR)

This is an 8-bit register that contains the low part of the value to be compared to the CLR register.

OC1LR — Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Output compare 2 high register (OC2HR)

This is an 8-bit register that contains the high part of the value to be compared to the CHR register.

OC2HR — Reset value: 1000 0000 (80h)

7	6	5	4	3	2	1	0
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Output compare 2 low register (OC2LR)

This is an 8-bit register that contains the low part of the value to be compared to the CLR register.

OC2LR — Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Counter high register (CHR)

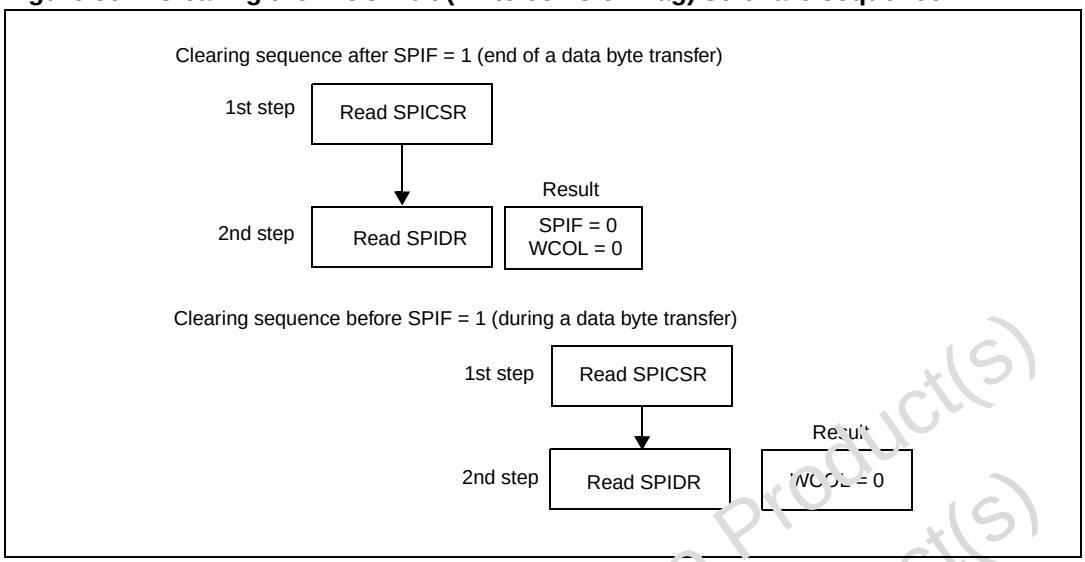
This is an 8-bit read-only register that contains the high part of the counter value.

CHR — Reset value: 1111 1111 (FFh)

7	6	5	4	3	2	1	0
MSB							LSB
RO	RO	RO	RO	RO	RO	RO	RO

Clearing the WCOL bit is done through a software sequence (see *Figure 59*).

Figure 59. Clearing the WCOL bit (write collision flag) software sequence



1. Writing to the SPIDR register instead of reading it does not reset the WCOL bit.

Single master and multimaster configurations

There are two types of SPI systems:

- Single master system
- Multimaster system

Single master system

A typical single master system may be configured using a device as the master and four devices as slaves (see *Figure 60*).

The master device selects the individual slave devices by using four pins of a parallel port to control the four $\overline{SS}$ pins of the slave devices.

The $\overline{SS}$ pins are pulled high during reset since the master device ports are forced to be inputs at that time, thus disabling the slave devices.

Note: To prevent a bus conflict on the MISO line, the master allows only one active slave device during a transmission.

For more security, the slave device may respond to the master with the received data byte. Then the master receives the previous byte back from the slave device if all MISO and MOSI pins are connected and the slave has not written to its SPIDR register.

Other transmission security methods can use ports for handshake lines or data bytes with command fields.

Multimaster system

A multimaster system may also be configured by the user. Transfer of master control could be implemented using a handshake method through the I/O ports or by an exchange of code messages through the serial peripheral interface system.

The multimaster system is principally handled by the MSTR bit in the SPICR register and the MODF bit in the SPICSR register.

Table 69. SCICR1 register description(1) (continued)

Bit	Name	Function
4	M	Word length This bit determines the word length. It is set or cleared by software. 0: 1 start bit, 8 data bits, 1 stop bit 1: 1 start bit, 9 data bits, 1 stop bit *Note: The M bit must not be modified during a data transfer (both transmission and reception).*
3	WAKE	Wake-up method This bit determines the SCI wake-up method. It is set or cleared by software. 0: Idle line 1: Address mark *Note: If the LINE bit is set, the WAKE bit is deactivated and replaced by the LHDM bit.*
2	PCE	Parity control enable This bit is set and cleared by software. It selects the hardware parity control for LIN identifier parity check. 0: Parity control disabled 1: Parity control enabled When a parity error occurs, the PE bit in the SCISR register is set.
1	-	Reserved, must be kept cleared
0	PIE	Parity interrupt enable This bit enables the interrupt capability of the hardware parity control when a parity error is detected (PE bit set). The parity error involved can be a byte parity error (if bit PCE is set and bit LPE is reset) or a LIN parity error (if bit PCE is set and bit LPE is set). 0: Parity error interrupt disabled 1: Parity error interrupt enabled

1. Bits 7:3 and bit 0 have the same function as in SCI mode; please refer to *SCI control register 1 (SCICR1) on page 153*.

SCI control register 2 (SCICR2)

SCICR2 Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

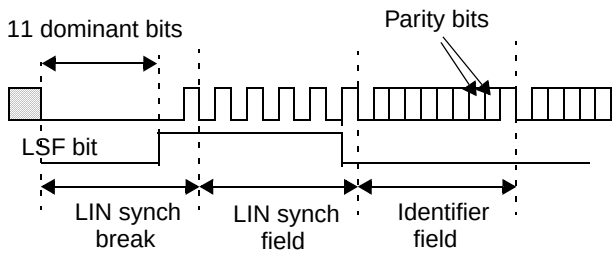
Table 70. SCICR2 register description(1)

Bit	Name	Function
7	TIE	Transmitter interrupt enable This bit is set and cleared by software. 0: Interrupt is inhibited 1: An SCI interrupt is generated whenever TDRE = 1 in the SCISR register
6	TCIE	Transmission complete interrupt enable This bit is set and cleared by software. 0: Interrupt is inhibited 1: An SCI interrupt is generated whenever TC = 1 in the SCISR register

Table 71. SCICR3 register description (continued)

Bit	Name	Function
3	LHDM	LIN header detection method This bit is set and cleared by software. It is only usable in LIN slave mode. It enables the header detection method. In addition if the RWU bit in the SCICR2 register is set, the LHDM bit selects the wake-up method (replacing the WAKE bit). 0: LIN synch break detection method 1: LIN identifier field detection method
2	LHIE	LIN header interrupt enable This bit is set and cleared by software. It is only usable in LIN slave mode. 0: LIN header interrupt is inhibited 1: An SCI interrupt is generated whenever LHDF = 1
1	LHDF	LIN header detection flag This bit is set by hardware when a LIN header is detected and cleared by a software sequence (an access to the SCISR register followed by a read of the SCICR3 register). It is only usable in LIN slave mode. 0: No LIN header detected 1: LIN header detected *Note: The header detection method depends on the LHDM bit:* *- If LHDM = 0, a header is detected as a LIN synch break* *- If LHDM = 1, a header is detected as a LIN Identifier, meaning that a LIN synch break field + a LIN synch field + a LIN identifier field have been consecutively received.*
0	LSF	LIN synch field state This bit indicates that the LIN synch field is being analyzed. It is only used in LIN slave mode. In auto synchronization mode (LASE bit = 1), when the SCI is in the LIN synch field state it waits or counts the falling edges on the RDI line. It is set by hardware as soon as a LIN synch break is detected and cleared by hardware when the LIN synch field analysis is finished (see *Figure 73*). This bit can also be cleared by software to exit LIN Synch state and return to idle mode. 0: The current character is not the LIN synch field 1: LIN synch field state (LIN synch field undergoing analysis)

Figure 73. LSF bit set and clear



Sensorless mode

This mode is used to detect BEMF zero crossing and end of demagnetization events.

The analog phase multiplexer connects the non-excited motor winding to an analog 100mV hysteresis comparator referred to a selectable reference voltage.

IS[1:0] bits in MPHST register allow the input to be selected which drives to the comparator (either MCIA, B or C). Be careful that the comparator is OFF until CKE and/or DAC bits are set in MCRA register.

The VR[2:0] bits in the MCRC register select the reference voltage from seven internal values depending on the noise level and the application voltage supply. The reference voltage can also be set externally through the MCVREF pin when the VR[2:0] bits are set.

Table 83. Threshold voltage setting

VR2	VR1	VR0	V_{REF} voltage threshold
1	**1**	**1**	**Threshold voltage set by external MCVREF pin typical value for V_{DD} = 5V**
1	1	0	3.5V
1	0	1	2.5V
1	0	0	2V
0	1	1	1.5V
0	1	0	1V
0	0	1	0.6V
0	0	0	0.2V

BEMF detections are performed during the measurement window, when the excited windings are free wheeling through the low side switches and diodes. At this stage the common star connection voltage is near to ground voltage (instead of $V_{DD}/2$ when the excited windings are powered) and the complete BEMF voltage is present on the non-excited winding terminal, referred to the ground terminal.

The zero crossing sampling frequency is then defined, in current mode, by the measurement window generator frequency (SA[3:0] bits in the MPRSR register) or, in voltage mode, by the PWM generator frequency and phase U duty cycle.

During a short period after a phase commutation (C event), the winding where the back-emf is read is no longer excited but needs a demagnetization phase during which the BEMF cannot be read. A demagnetization current goes through the free-wheeling diodes and the winding voltage is stuck at the high voltage or to the ground terminal. For this reason an ‘end of demagnetization event’ D must be detected on the winding before the detector can sense a BEMF zero crossing.

For the end-of-demagnetization detection, no special PWM configuration is needed; the comparator sensing is done at a selectable frequency (f_{SCF}) (see *Table 166*).

So the three events C (commutation), D (demagnetization) and Z (BEMF zero crossing) must always occur in this order in autoswitched mode when hard commutation is selected.

The comparator output is processed by a detector that automatically recognizes the D or Z event, depending on the CPB or ZVD edge and level configuration bits as described in *Table 88*.

To avoid wrong detection of D and Z events, a blanking window filter is implemented for spike filtering. In addition, by means of an event counter, software can filter several consecutive events up to a programmed limit before generating the D or Z event internally. This is shown in *Figure 80* and *Figure 81*.

D event detection

In sensorless mode, the D window filter becomes active after each C event. It blanks out the D event during the time window defined by the DWF[3:0] bits in the MDFR register (see *Table 84*). The reset value is 200µs.

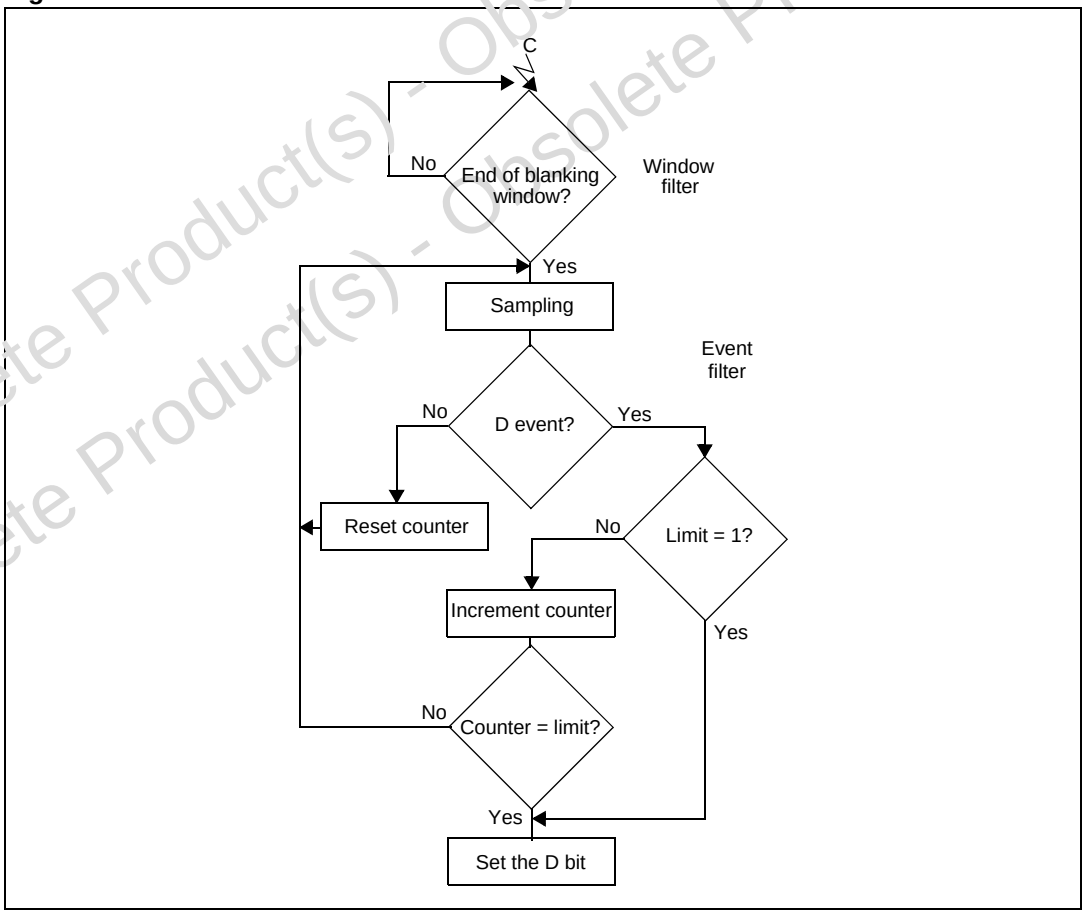
This window filter becomes active after both hardware and software C events.

The D event filter becomes active after the D window filter. It counts the number of consecutive D events up to a limit defined by the DEF[3:0] bits in the MDFR register. The reset value is 1. The D bit is set when the counter limit is reached.

Sampling is done at a selectable frequency (f_{SCF}), see *Table 163*.

The D event filter is active only for a hardware D event (D_H). For a simulated (D_S) event, it is forced to 1.

Figure 80. D window and event filter flowchart



When enabled by the SDM bit in the MCRB register, demagnetization can also be simulated by comparing the MTIM timer with the MDREG register. This kind of demagnetization is called simulated demagnetization D_S.

If the HDM and SDM bits are both set, the first event that occurs, triggers a demagnetization event. For this to work correctly, a D_S event must not precede a D_H event because the latter could be detected as a Z event.

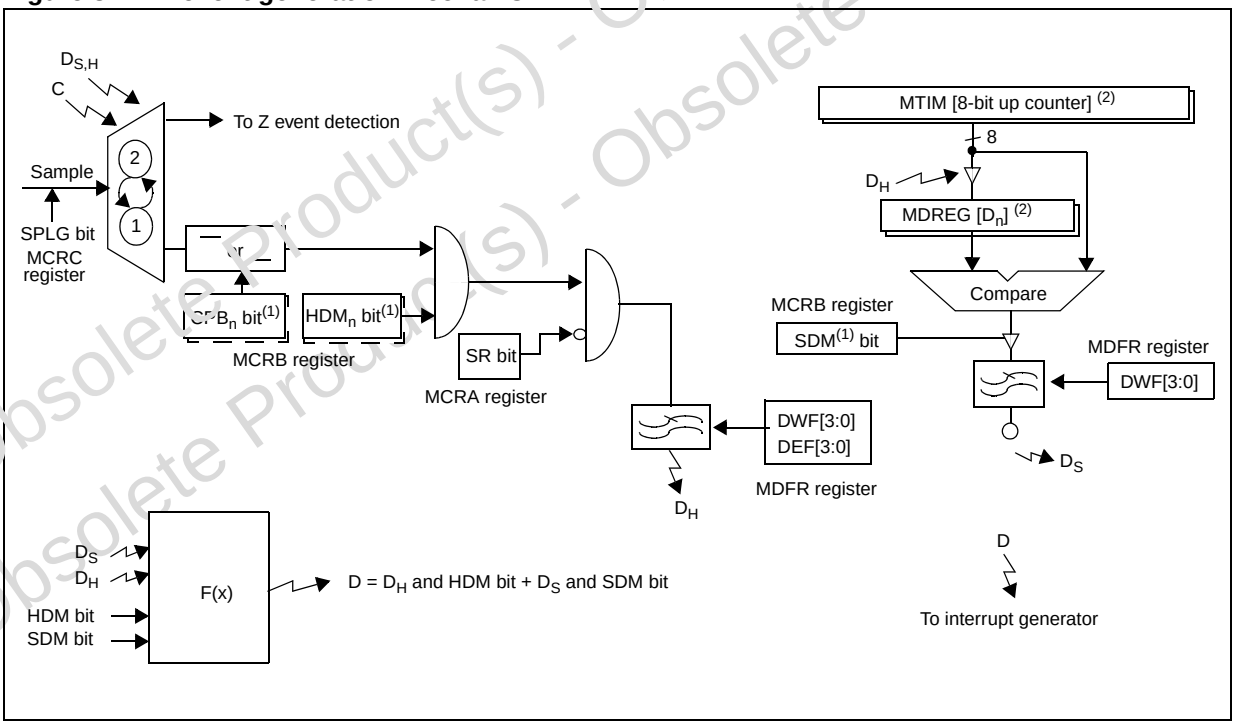
Simulated demagnetization can also be always used if the HDM bit is reset and the SDM bit is set. This mode works as a programmable masking time between the C_H and Z events. To drive the motor securely, the masking time must be always greater than the real demagnetization time in order to avoid a spurious Z event.

When an event occurs, (either D_H or D_S) the DI bit in the MISR register is set and an interrupt request is generated if the DIM bit of register MIMR is set.

Caution: **1:** Due to the alternate automatic capture and compare of the MTIM timer with MDREG register by D_H and D_S events, the MDREG register should be manipulated with special care.

Caution: **2:** Due to the event generation protection in the MZREG, MCOMP and MDREG registers for Soft Event generation (see *Built-in checks and controls for simulated events on page 221*), the value written in the MDREG register in soft demagnetization mode (SDM = 1) is checked by hardware after the C event. If this value is less than or equal to the MTIM counter value at this moment, the Software demagnetization event is generated immediately and the MTIM current value overwrites the value in the MDREG register to be able to re-use the right demagnetization time for another simulated event generation.

Figure 82. D event generation mechanism



1. Preload bit, new value taken into account at the next C event (in normal mode) or when a value is written in the MPHST register when in direct access mode. For more details refer to the description of the DAC bit in *Control register A (MCRA) on page 265*. The use of a preload register allows all the registers to be updated at the same time
2. Register updated on R event

shifted left (multiplied by two). The RMI bit in the MISR register is set and an interrupt is generated if RIM is set.

– If the prescaler contents reach the value 0, it can no longer be automatically decremented, the MTC continues working with the same prescaler value, that is, with a lower accuracy. No RMI interrupt can be generated.

– If the prescaler contents reach the value 15, it can no longer be automatically incremented. When the timer reaches the value FFh, the prescaler and all the relevant registers remain unchanged and no interrupt is generated, the timer restarts counting from 0 x 00h and if the TES[1:0] bits = 00, the OI bit in the MCRC register is set at each overflow (it has to be reset by software). The RPI bit is no longer set. The PWM is still generated and the D and Z detection circuitry still work, enabling the capture of the maximum timer value.

The automatically updated registers are: MTIM, MZREG, MZPRV, MCOMP and MDREG. Access to these registers is summarized in *Table 99*.

Debug option

In both switched mode and autoswitched mode, setting the bit DG in MPWME register enables the debug option. This option consists of outputting the C, D and Z signals in real time on pins MCZEM and MCDEM. This is very useful during the debug phase of the application. *Figure 95* shows the signals output on pins MCDEM and MCZEM with the debug option.

Note: 1 When the delay coefficient equals 0/256 (C event immediately after Z event), a glitch appears on MCZEM pin to be able to see the event even in this case.

This option is also available in speed measurement mode with different signal outputs (see Figure 95):

- MCDEM toggles when a capture event is generated.
- MCZEM toggles every time a U event is generated.

These signals are only available if the TES[1:0] bits = 10, 01 or 11.

2 In sensor mode, the MCDEM output pin toggles at each C event. The MCZEM pin outputs the Z event.

Table 105. Sampling frequency selection(1) (continued)

SA3	SA2	SA1	SA0	Sampling frequency
1	1	0	1	961 Hz
1	1	1	0	625 Hz
1	1	1	1	390 Hz

1. *Times are indicated for 4 MHz f_{PERIPH}.*

Warning: If the off time value set is superior than the period of the PWM signal (for example 40µs off time for a 50 kHz (25µs period) PWM frequency), then the signal output on MCOx pins selected is a 100% duty cycle signal (always at 1).

Table 106. Off time table(1)

OT3	OT2	OT1	OT0	OFF time sensorless mode (SR = 0) (DS[3:0] = 0)	Sensor mode (SR = 1) or sampling during ON time in sensorless mode (SPLG = 1 and/or DS[3:0] bits)
0	0	0	0	2.5 µs	No minimum off time
0	0	0	1	5 µs	
0	0	1	0	7.5 µs	
0	0	1	1	10 µs	
0	1	0	0	12.5 µs	
0	1	0	1	15 µs	
0	1	1	0	17.5 µs	
0	1	1	1	20 µs	
1	0	0	0	22.5 µs	
1	0	0	1	25 µs	
1	0	1	0	27.5 µs	
1	0	1	1	30 µs	
1	1	0	0	32.5 µs	
1	1	0	1	35 µs	
1	1	1	0	37.5 µs	
1	1	1	1	40 µs	

1. Times are indicated for 4 MHz f_{PERIPH}.

Table 110. Deadtime programming and example

DTG5	DTG4	T_{dtg}	Deadtime expression	Deadtime value	T_{dtg} @ 16 MHz f_{mtc}	Deadtime range @ 16 MHz f_{mtc}
0	X	$2xT_{mtc}$	(DTG[4..0]+1) x T_{dtg}	From 1 to 32 T_{dtg}	125ns	0.125µs to 4µs
1	0	$4xT_{mtc}$	(DTG[3..0]+17) x T_{dtg}	From 17 to 32 T_{dtg}	250ns	4.25µs to 8µs
1	1	$8xT_{mtc}$			500ns	8.5µs to 16µs

The deadtime delay is the same for each of the channels and is programmable with the DTG[5..0] bits in the MDTG register.

The resolution is variable and depends on the DTG5 and DTG4 bits. *Table 110* summarizes the set-up of the deadtime generator.

IT_{mtc} is the period of the deadtime generator input clock (F_{mtc} = 16 MHz in most cases, not affected by the XT16:XT8 prescaler bits in the MCONF register).

For safety reasons, and since the deadtime depends only on external component characteristics (level-shifter delay, power components switching duration, etc.), the register used to set-up deadtime duration can be written only once after the MCU reset. This prevents a corrupted program counter modifying this system critical set-up, which may cause excessive power dissipation or destructive shoot-through in the power stage half bridges.

When using the three independent U, V and W PWM signals (PCN bit set) (see *Figure 115*) to drive the MCOx outputs, deadtime is added as shown in *Figure 112*.

The deadtime generator is enabled/disabled using the DTE bit.

The effect of the DTE bit depends on the PCN bit value.

If the PCN bit is set:

- DTE is read only. To reset it, first reset the PCN bit, then reset DTE and set PCN to 1 again.
- If DTE = 0, the high and low side outputs are simply complemented (no deadtime insertion, DTG[5:0] bits are not significant); this is to allow the use of an external deadtime generator.

Note: The reset value of the MDTG register is FFh so when configuring the deadtime, it is mandatory to follow one the two following sequences:

1. *To use deadtimes while the PCN bit is set; from reset state write the MDTG value at once. The DTE bit is read back as 1 whatever the programming value (read only if PCN = 1)*
2. *To use deadtimes while the PCN bit is reset, write first the deadtime value in DTG[5:0], then reset the PCN bit, or do both actions at the same time.*

Interrupt mask register (MIMR)

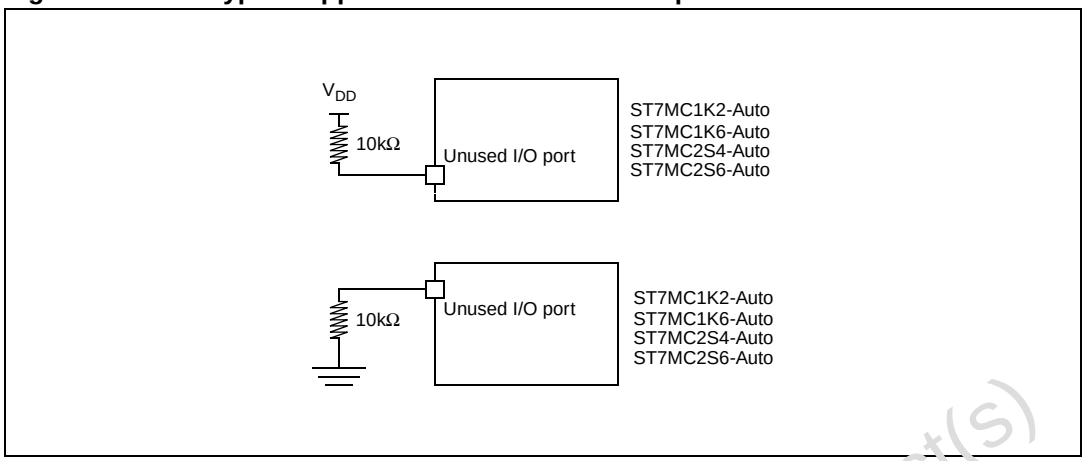
MIMR Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
PUM	SEM	RIM	CLIM	EIM	ZIM	DIM	CIM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 124. MIMR register description

Bit	Name	Function
7	PUM	PWM update mask bit 0: PWM update interrupt disabled 1: PWM update interrupt enabled
6	SEM	Speed error mask bit 0: Speed error interrupt disabled 1: Speed error interrupt enabled
5	RIM	Ratio update interrupt mask bit 0: Ratio update interrupts (R+ and R-) disabled 1: Ratio update interrupts (R+ and R-) enabled
4	CLIM	Current limitation interrupt mask bit 0: Current limitation interrupt disabled 1: Current limitation interrupt enabled This interrupt is available only in voltage mode (VOC1 bit = 0 in MCRA register) and occurs when the motor current feedback reaches the external current limitation value.
3	EIM	Emergency stop interrupt mask bit 0: Emergency stop interrupt disabled 1: Emergency stop interrupt enabled
2	ZIM	Back EMF zero-crossing interrupt mask bit 0: BEMF Zero-crossing Interrupt disabled 1: BEMF Zero-crossing Interrupt enabled
1	DIM	End of demagnetization interrupt mask bit 0: End of demagnetization interrupt disabled 1: End of demagnetization interrupt enabled if the HDM or SDM bit in the MCRB register is set
0	CIM	Commutation/capture interrupt mask bit 0: Commutation/capture interrupt disabled 1: Commutation/capture interrupt enabled

Figure 139. Two typical applications with unused I/O pin



1. I/O can be left unconnected if it is configured as output (0 or 1) by the software. This has the advantage of greater EMC robustness and lower cost.

Figure 140. Typical I_{PU} vs. V_{DD} with $V_{IN} = V_{SS}$

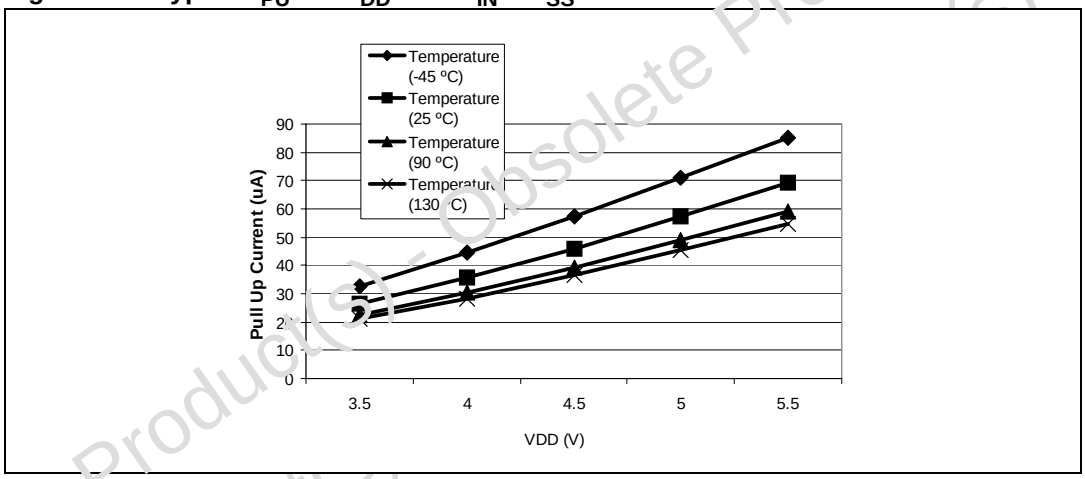
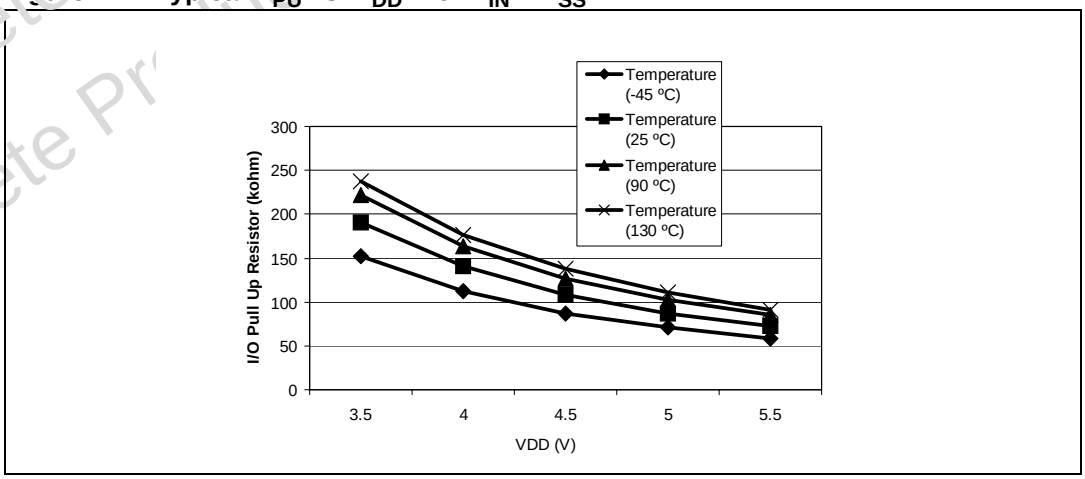


Figure 141. Typical R_{PU} vs. V_{DD} with $V_{IN} = V_{SS}$



14.2 Device ordering information and transfer of customer code

The FASTROM or ROM contents are to be sent on diskette, or by electronic means, with the hexadecimal file in .S19 format generated by the development tool. All unused bytes must be set to FFh.

The selected options are communicated to STMicroelectronics using the correctly completed option list appended.

Refer to application note AN1635 for information on the counter listing returned by ST after code has been transferred.

The STMicroelectronics sales organization provides detailed information on contractual points.

Table 229. Supported part numbers

Part number	Program memory (bytes)	RAM (bytes)	Temp. range	Package
ST7FMC1K2TC	8K Flash	384	-40°C +125°C	LQFP32
ST7FMC1K6TC	32K Flash	1024		
ST7FMC2S4TC	16K Flash	768		LQFP44
ST7FMC2S6TC	32K Flash	1024		
ST7MC1K2TC/xxx(1)	8K ROM	384		LQFP32
ST7MC2S4TC/xxx(1)	16K ROM	768		LQFP44
ST7PMC1K2TC/xxx(1)	8K FASTROM	384		LQFP32
ST7PMC1K6TC/xxx(1)	32K FASTROM	1024		
ST7PMC2S4TC/xxx(1)	16K FASTROM	768		LQFP44
ST7PMC2S6TC/xxx(1)	32K FASTROM	1024		

1. /xxx stands for the ROM or FASTROM code assigned by STMicrolectronics.