# Infineon Technologies - MB96F386RSBPMC-GSE2 Datasheet

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## What is "Embedded - Microcontrollers"?

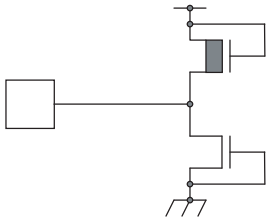
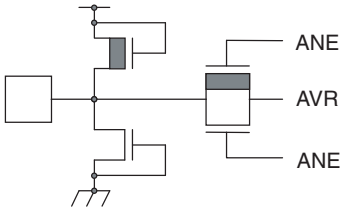
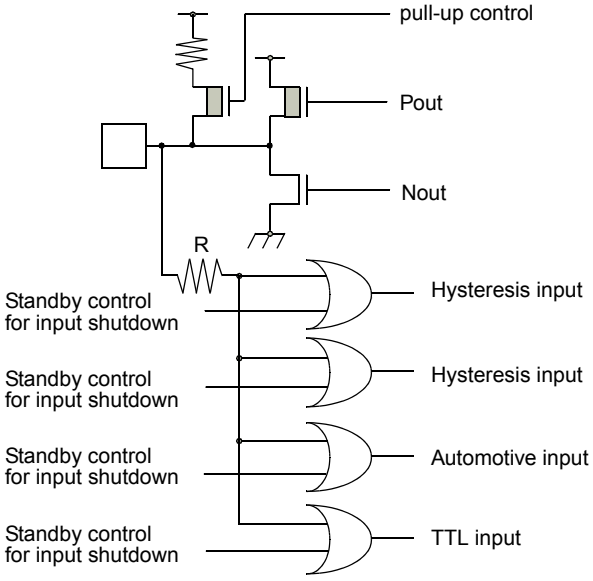
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | F²MC-16FX |
| Core Size | 16-Bit |
| Speed | 56MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART |
| Peripherals | DMA, LCD, LVD, LVR, POR, PWM, WDT |
| Number of I/O | 96 |
| Program Memory Size | 288KB (288K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 120-LQFP |
| Supplier Device Package | 120-LQFP (16x16) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb96f386rsbpmc-gse2 |

## 1. Product Lineup

| Features | | MB96V300B | MB96(F)38x |
|---|---|---|---|
| Product type | | Evaluation sample | Flash product: MB96F38x<br>Mask ROM product: MB9638x |
| Product options | | | |
| YS | | NA | Low voltage reset persistently on / Single clock |
| RS | | | Low voltage reset can be disabled / Single clock |
| YW | | | Low voltage reset persistently on / Dual clock |
| RW | | | Low voltage reset can be disabled / Dual clock |
| TS | | | indep. 32KB Flash / Low voltage reset persistently on / Single clock |
| HS | | | indep. 32KB Flash / Low voltage reset can be disabled / Single clock |
| TW | | | indep. 32KB Flash / Low voltage reset persistently on / Dual clock |
| HW | | | indep. 32KB Flash / Low voltage reset can be disabled / Dual clock |
| Flash/ROM | RAM | | |
| 128KB | 6KB | ROM/Flash memory emulation by external RAM, 92KB internal RAM | MB96384Y[*1], MB96384R[*1] |
| 160KB | 8KB | | MB96385Y[*1], MB96385R[*1], MB96F385Y[*1], MB96F385R[*1] |
| 288KB | 16KB | | MB96F386Y, MB96F386R |
| 416KB | 16KB | | MB96F387Y, MB96F387R |
| 576KB [Flash A: 544KB, Flash B: 32KB] | 28KB | | MB96F388T[*1], MB96F388H[*1] |
| 832KB [Flash A: 544KB, Flash B: 288KB] | 32KB | | MB96F389Y[*1], MB96F389R[*1], |
| Package | | BGA416 | FPT-120P-M21 |
| DMA | | 16 channels | 7 channels |
| USART | | 10 channels | 5 channels |
| I2C | | 2 channels | 1 channel |
| A/D Converter | | 40 channels | 16 channels |
| A/D Converter Reference Voltage switch | | yes | Only for MB96F386Y, MB96F386R, MB96F387Y, MB96F387R |
| 16-bit Reload Timer | | 6 channels + 1 channel (for PPG) | 4 channels + 1 channel (for PPG) |
| 16-bit Free-Running Timer | | 4 channels | 2 channels |
| 16-bit Output Compare | | 12 channels | 4 channels |

| Type | Circuit | Remarks |
|---|---|---|
| F |  | • Power supply input protection circuit |
| G |  | • A/D converter ref+ (AVRH/AVRH2) power supply input pin with protection circuit<br>• Flash devices do not have a protection circuit against VCC for pins AVRH/AVRH2<br>• Devices without AVRH reference switch do not have an analog switch for the AVRL pin |
| H |  | • CMOS level output (programmable $I_{OL}$ = 5mA, $I_{OH}$ = -5mA and $I_{OL}$ = 2mA, $I_{OH}$ = -2mA)<br>• 2 different CMOS hysteresis inputs with input shutdown function<br>• Automotive input with input shutdown function<br>• TTL input with input shutdown function<br>• Programmable pull-up resistor: 50kΩ approx. |

**I/O map MB96(F)38x (Sheet 22 of 30)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| $00061F_H$ | LCD - Output Enable Register 3 (Seg 31-24) | LCDER3 | - | R/W |
| $000620_H$ | LCD - Output Enable Register 4 (Seg 39-32) | LCDER4 | - | R/W |
| $000621_H$ | LCD - Output Enable Register 5 (Seg 47-40) | LCDER5 | - | R/W |
| $000622_H$ | LCD - Output Enable Register 6 (Seg 55-48) | LCDER6 | - | R/W |
| $000623_H$ | LCD - Output Enable Register 7 (Seg 63-56) | LCDER7 | - | R/W |
| $000624_H$ | LCD - Output Enable Register 8 (Seg 71-64) | LCDER8 | - | R/W |
| $000625_H$ | Reserved | - | - | - |
| $000626_H$ | LCD - Output Enable Register V (Vx) | LCDVER | - | R/W |
| $000627_H$ | LCD - Extended Control Register | LECR | - | R/W |
| $000628_H$ | LCD - Common pin switching register | LCDCMR | - | R/W |
| $000629_H$ | LCD - Control Register | LCR | - | R/W |
| $00062A_H$ | LCD - Data register for Segment 1-0 | VRAM0 | - | R/W |
| $00062B_H$ | LCD - Data register for Segment 3-2 | VRAM1 | - | R/W |
| $00062C_H$ | LCD - Data register for Segment 5-4 | VRAM2 | - | R/W |
| $00062D_H$ | LCD - Data register for Segment 7-6 | VRAM3 | - | R/W |
| $00062E_H$ | LCD - Data register for Segment 9-8 | VRAM4 | - | R/W |
| $00062F_H$ | LCD - Data register for Segment 11-10 | VRAM5 | - | R/W |
| $000630_H$ | LCD - Data register for Segment 13-12 | VRAM6 | - | R/W |
| $000631_H$ | LCD - Data register for Segment 15-14 | VRAM7 | - | R/W |
| $000632_H$ | LCD - Data register for Segment 17-16 | VRAM8 | - | R/W |
| $000633_H$ | LCD - Data register for Segment 19-18 | VRAM9 | - | R/W |
| $000634_H$ | LCD - Data register for Segment 21-20 | VRAM10 | - | R/W |
| $000635_H$ | LCD - Data register for Segment 23-22 | VRAM11 | - | R/W |
| $000636_H$ | LCD - Data register for Segment 25-24 | VRAM12 | - | R/W |
| $000637_H$ | LCD - Data register for Segment 27-26 | VRAM13 | - | R/W |
| $000638_H$ | LCD - Data register for Segment 29-28 | VRAM14 | - | R/W |
| $000639_H$ | LCD - Data register for Segment 31-30 | VRAM15 | - | R/W |
| $00063A_H$ | LCD - Data register for Segment 33-32 | VRAM16 | - | R/W |
| $00063B_H$ | LCD - Data register for Segment 35-34 | VRAM17 | - | R/W |
| $00063C_H$ | LCD - Data register for Segment 37-36 | VRAM18 | - | R/W |

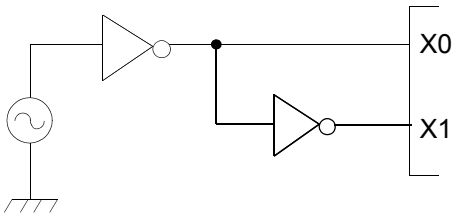
**I/O map MB96(F)38x (Sheet 23 of 30)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| $00063D_H$ | LCD - Data register for Segment 39-38 | VRAM19 | - | R/W |
| $00063E_H$ | LCD - Data register for Segment 41-40 | VRAM20 | - | R/W |
| $00063F_H$ | LCD - Data register for Segment 43-42 | VRAM21 | - | R/W |
| $000640_H$ | LCD - Data register for Segment 45-44 | VRAM22 | - | R/W |
| $000641_H$ | LCD - Data register for Segment 47-46 | VRAM23 | - | R/W |
| $000642_H$ | LCD - Data register for Segment 49-48 | VRAM24 | - | R/W |
| $000643_H$ | LCD - Data register for Segment 51-50 | VRAM25 | - | R/W |
| $000644_H$ | LCD - Data register for Segment 53-52 | VRAM26 | - | R/W |
| $000645_H$ | LCD - Data register for Segment 55-54 | VRAM27 | - | R/W |
| $000646_H$ | LCD - Data register for Segment 57-56 | VRAM28 | - | R/W |
| $000647_H$ | LCD - Data register for Segment 59-58 | VRAM29 | - | R/W |
| $000648_H$ | LCD - Data register for Segment 61-60 | VRAM30 | - | R/W |
| $000649_H$ | LCD - Data register for Segment 63-62 | VRAM31 | - | R/W |
| $00064A_H$ | LCD - Data register for Segment 65-64 | VRAM32 | - | R/W |
| $00064B_H$-$00065F_H$ | Reserved | - | - | - |
| $000660_H$ | Peripheral Resource Relocation Register 10 | PRRR10 | - | R/W |
| $000661_H$ | Peripheral Resource Relocation Register 11 | PRRR11 | - | R/W |
| $000662_H$ | Peripheral Resource Relocation Register 12 | PRRR12 | - | R/W |
| $000663_H$ | Peripheral Resource Relocation Register 13 | PRRR13 | - | W |
| $000664_H$-$0006DF_H$ | Reserved | - | - | - |
| $0006E0_H$ | External Bus - Area configuration register 0 Low | EACL0 | EAC0 | R/W |
| $0006E1_H$ | External Bus - Area configuration register 0 High | EACH0 | - | R/W |
| $0006E2_H$ | External Bus - Area configuration register 1 Low | EACL1 | EAC1 | R/W |
| $0006E3_H$ | External Bus - Area configuration register 1 High | EACH1 | - | R/W |
| $0006E4_H$ | External Bus - Area configuration register 2 Low | EACL2 | EAC2 | R/W |
| $0006E5_H$ | External Bus - Area configuration register 2 High | EACH2 | - | R/W |
| $0006E6_H$ | External Bus - Area configuration register 3 Low | EACL3 | EAC3 | R/W |
| $0006E7_H$ | External Bus - Area configuration register 3 High | EACH3 | - | R/W |
| $0006E8_H$ | External Bus - Area configuration register 4 Low | EACL4 | EAC4 | R/W |

**I/O map MB96(F)38x (Sheet 26 of 30)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| $000746_H$ | CAN0 - IF2 Mask 2 Register Low | IF2MSK2L0 | IF2MSK20 | R/W |
| $000747_H$ | CAN0 - IF2 Mask 2 Register High | IF2MSK2H0 | - | R/W |
| $000748_H$ | CAN0 - IF2 Arbitration 1 Register Low | IF2ARB1L0 | IF2ARB10 | R/W |
| $000749_H$ | CAN0 - IF2 Arbitration 1 Register High | IF2ARB1H0 | - | R/W |
| $00074A_H$ | CAN0 - IF2 Arbitration 2 Register Low | IF2ARB2L0 | IF2ARB20 | R/W |
| $00074B_H$ | CAN0 - IF2 Arbitration 2 Register High | IF2ARB2H0 | - | R/W |
| $00074C_H$ | CAN0 - IF2 Message Control Register Low | IF2MCTRL0 | IF2MCTR0 | R/W |
| $00074D_H$ | CAN0 - IF2 Message Control Register High | IF2MCTRH0 | - | R/W |
| $00074E_H$ | CAN0 - IF2 Data A1 Low | IF2DTA1L0 | IF2DTA10 | R/W |
| $00074F_H$ | CAN0 - IF2 Data A1 High | IF2DTA1H0 | - | R/W |
| $000750_H$ | CAN0 - IF2 Data A2 Low | IF2DTA2L0 | IF2DTA20 | R/W |
| $000751_H$ | CAN0 - IF2 Data A2 High | IF2DTA2H0 | - | R/W |
| $000752_H$ | CAN0 - IF2 Data B1 Low | IF2DTB1L0 | IF2DTB10 | R/W |
| $000753_H$ | CAN0 - IF2 Data B1 High | IF2DTB1H0 | - | R/W |
| $000754_H$ | CAN0 - IF2 Data B2 Low | IF2DTB2L0 | IF2DTB20 | R/W |
| $000755_H$ | CAN0 - IF2 Data B2 High | IF2DTB2H0 | - | R/W |
| $000756_H$-$00077F_H$ | Reserved | - | - | - |
| $000780_H$ | CAN0 - Transmission Request 1 Register Low | TREQR1L0 | TREQR10 | R |
| $000781_H$ | CAN0 - Transmission Request 1 Register High | TREQR1H0 | - | R |
| $000782_H$ | CAN0 - Transmission Request 2 Register Low | TREQR2L0 | TREQR20 | R |
| $000783_H$ | CAN0 - Transmission Request 2 Register High | TREQR2H0 | - | R |
| $000784_H$-$00078F_H$ | Reserved | - | - | - |
| $000790_H$ | CAN0 - New Data 1 Register Low | NEWDT1L0 | NEWDT10 | R |
| $000791_H$ | CAN0 - New Data 1 Register High | NEWDT1H0 | - | R |
| $000792_H$ | CAN0 - New Data 2 Register Low | NEWDT2L0 | NEWDT20 | R |
| $000793_H$ | CAN0 - New Data 2 Register High | NEWDT2H0 | - | R |
| $000794_H$-$00079F_H$ | Reserved | - | - | - |
| $0007A0_H$ | CAN0 - Interrupt Pending 1 Register Low | INTPND1L0 | INTPND10 | R |
| $0007A1_H$ | CAN0 - Interrupt Pending 1 Register High | INTPND1H0 | - | R |

2. Opposite phase external clock
   - When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.




### 14.4 Unused sub clock signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

### 14.5 Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

### 14.6 Power supply pins ($V_{CC}$/$V_{SS}$)

It is required that all $V_{CC}$-level as well as all $V_{SS}$-level power supply pins are at the same potential. If there is more than one $V_{CC}$ or $V_{SS}$ level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

$V_{CC}$ and $V_{SS}$ must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 µF between $V_{CC}$ and $V_{SS}$ as close as possible to $V_{CC}$ and $V_{SS}$ pins.

### 14.7 Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

### 14.8 Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply ($AV_{CC}$, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply ($V_{CC}$) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or $AV_{CC}$ (turning the analog and digital power supplies simultaneously on or off is acceptable).

### 14.9 Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as $AV_{CC} = V_{CC}$, $AV_{SS}$ = AVRH = AVRL = $V_{SS}$.

### 14.10 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2 V to 2.7 V.

### 14.11 Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard Vcc power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

## 15.3 DC characteristics

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input H voltage | $V_{IH}$ | Port inputs Pnn_m | CMOS Hysteresis 0.8/0.2 input selected | 0.8 $V_{CC}$ | - | (D)$V_{CC}$ + 0.3 | V | |
| | | | CMOS Hysteresis 0.7/0.3 input selected | 0.7 $V_{CC}$ | - | (D)$V_{CC}$ + 0.3 | V | (D)$V_{CC}$ ≥ 4.5V |
| | | | | 0.74 $V_{CC}$ | - | (D)$V_{CC}$ + 0.3 | V | (D)$V_{CC}$ < 4.5V |
| | | | AUTOMOTIVE Hysteresis input selected | 0.8 $V_{CC}$ | - | (D)$V_{CC}$ + 0.3 | V | |
| | | | TTL input selected | 2.0 | - | (D)$V_{CC}$ + 0.3 | V | |
| | $V_{IHX0F}$ | X0 | External clock in “Fast Clock Input mode” | 0.8 $V_{CC}$ | - | $V_{CC}$ + 0.3 | V | Not available in MB96F386xxA/F387xxA |
| | $V_{IHX0S}$ | X0,X1, X0A,X1A | External clock in “oscillation mode” | 2.5 | - | $V_{CC}$ + 0.3 | V | |
| | $V_{IHR}$ | RSTX | - | 0.8 $V_{CC}$ | - | $V_{CC}$ + 0.3 | V | CMOS Hysteresis input |
| | $V_{IHM}$ | MD2-MD0 | - | $V_{CC}$ - 0.3 | - | $V_{CC}$ + 0.3 | V | |
| Input L voltage | $V_{IL}$ | Port inputs Pnn_m | CMOS Hysteresis 0.8/0.2 input selected | $V_{SS}$ - 0.3 | - | 0.2 (D)$V_{CC}$ | V | |
| | | | CMOS Hysteresis 0.7/0.3 input selected | $V_{SS}$ - 0.3 | - | 0.3 (D)$V_{CC}$ | V | |
| | | | AUTOMOTIVE Hysteresis input selected | $V_{SS}$ - 0.3 | - | 0.5 (D)$V_{CC}$ | V | (D)$V_{CC}$ ≥ 4.5V |
| | | | | $V_{SS}$ - 0.3 | - | 0.46 (D)$V_{CC}$ | | (D)$V_{CC}$ < 4.5V |
| | | | TTL input selected | $V_{SS}$ - 0.3 | - | 0.8 | V | |
| | $V_{ILX0F}$ | X0 | External clock in “Fast Clock Input mode” | $V_{SS}$ - 0.3 | - | 0.2 $V_{CC}$ | V | Not available in MB96F386xxA/F387xxA |
| | $V_{ILX0S}$ | X0,X1, X0A,X1A | External clock in “oscillation mode” | $V_{SS}$ - 0.3 | - | 0.4 | V | |
| | $V_{ILR}$ | RSTX | - | $V_{SS}$ - 0.3 | - | 0.2 $V_{CC}$ | V | CMOS Hysteresis input |
| | $V_{ILM}$ | MD2-MD0 | - | $V_{SS}$ - 0.3 | - | $V_{SS}$ + 0.3 | V | |

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

| Parameter | Symbol | Condition (at $T_A$) | | Value | | | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Max | Unit | |
| Power supply current in Sleep modes* | $I_{CCSMAIN}$ | Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped) | +25°C | 1.5 | 1.8 | mA | MB96F386/F387 |
| | | | +125°C | 2 | 4.5 | | |
| | | | +25°C | 1.6 | 2 | mA | MB96F388/F389 |
| | | | +125°C | 2.1 | 4.2 | | |
| | | | +25°C | 1.5 | 1.8 | mA | MB96384/385/F385 |
| | | | +125°C | 2 | 3.3 | | |
| | $I_{CCSRCH}$ | RC Sleep mode with CLKS1/2 = CLKP1/2 = 2MHz (CLKMC, CLKPLL and CLKSC stopped) | +25°C | 0.9 | 1.4 | mA | MB96F386/F387 |
| | | | +125°C | 1.5 | 4 | | |
| | | | +25°C | 0.9 | 1.4 | mA | MB96F388/F389 |
| | | | +125°C | 1.5 | 3.5 | | |
| | | | +25°C | 0.9 | 1.4 | mA | MB96384/385/F385 |
| | | | +125°C | 1.5 | 2.8 | | |

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

| Parameter | Symbol | Condition (at $T_A$) | | Value | | | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Max | Unit | |
| Power supply current in Sleep modes* | $I_{CCSRCL}$ | RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode) | +25°C | 0.3 | 0.5 | mA | MB96F386/F387 |
| | | | +125°C | 0.8 | 3.4 | | |
| | | | +25°C | 0.3 | 0.5 | mA | MB96F388/F389 |
| | | | +125°C | 0.8 | 2.8 | | |
| | | | +25°C | 0.3 | 0.5 | mA | MB96384/385/F385 |
| | | | +125°C | 0.8 | 2 | | |
| | | RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode) | +25°C | 0.06 | 0.15 | mA | MB96F386/F387 |
| | | | +125°C | 0.56 | 3 | | |
| | | | +25°C | 0.06 | 0.15 | mA | MB96F388/F389 |
| | | | +125°C | 0.56 | 2.4 | | |
| | | | +25°C | 0.06 | 0.15 | mA | MB96384/385/F385 |
| | | | +125°C | 0.56 | 1.6 | | |
| | $I_{CCSUB}$ | Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz (CLKMC, CLKPLL and CLKRC stopped) | +25°C | 0.04 | 0.12 | mA | MB96F386/F387 |
| | | | +125°C | 0.54 | 2.9 | | |
| | | | +25°C | 0.04 | 0.12 | mA | MB96F388/F389 |
| | | | +125°C | 0.54 | 2.3 | | |
| | | | +25°C | 0.04 | 0.12 | mA | MB96384/385/F385 |
| | | | +125°C | 0.54 | 1.55 | | |
| Power supply current in Timer modes* | $I_{CCTPLL}$ | PLL Timer mode with CLKMC = 4MHz, CLKPLL = 48MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V) | +25°C | 1.6 | 2 | mA | MB96F386/F387 |
| | | | +125°C | 2.1 | 4.8 | | |
| | | | +25°C | 1.6 | 2 | mA | MB96F388/F389 |
| | | | +125°C | 2.1 | 4.2 | | |
| | | | +25°C | 1.6 | 2 | mA | MB96384/385/F385 |
| | | | +125°C | 2.1 | 3.5 | | |

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

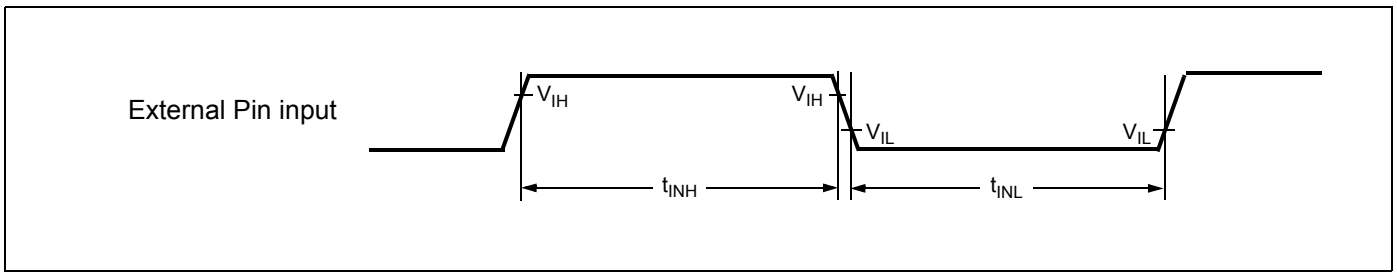
| Parameter | Symbol | Condition (at $T_A$) | | Value | | | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Max | Unit | |
| Power supply current in Timer modes* | $I_{CCTRCL}$ | RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode) | +25°C | 0.3 | 0.45 | mA | MB96F386/F387 |
| | | | +125°C | 0.8 | 3.2 | | |
| | | | +25°C | 0.3 | 0.45 | mA | MB96F386/F387 |
| | | | +125°C | 0.8 | 2.6 | | |
| | | | +25°C | 0.3 | 0.45 | mA | MB96384/385/F385 |
| | | | +125°C | 0.8 | 1.95 | | |
| | | RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode) | +25°C | 0.05 | 0.1 | mA | MB96F386/F387 |
| | | | +125°C | 0.55 | 2.8 | | |
| | | | +25°C | 0.05 | 0.1 | mA | MB96F388/F389 |
| | | | +125°C | 0.55 | 2.2 | | |
| | | | +25°C | 0.05 | 0.1 | mA | MB96384/385/F385 |
| | | | +125°C | 0.55 | 1.55 | | |
| | $I_{CCTSUB}$ | Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped) | +25°C | 0.03 | 0.1 | mA | MB96F386/F387 |
| | | | +125°C | 0.53 | 2.8 | | |
| | | | +25°C | 0.03 | 0.1 | mA | MB96F388/F389 |
| | | | +125°C | 0.53 | 2.2 | | |
| | | | +25°C | 0.03 | 0.1 | mA | MB96384/385/F385 |
| | | | +125°C | 0.53 | 1.55 | | |

### External Input timing

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

| Parameter | Symbol | Pin | Condition | Value | | Unit | Used Pin input function |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{INH}$ $t_{INL}$ | INTn(_R) | — | 200 | — | ns | External Interrupt |
| | | NMI(_R) | | | | | NMI |
| | | Pnn_m | | $2*t_{CLKP1}$ + 200 ($t_{CLKP1}$=1/$f_{CLKP1}$) | — | ns | General Purpose IO |
| | | TINn(_R) | | | | | Reload Timer |
| | | TTGn(_R) | | | | | PPG Trigger input |
| | | ADTG(_R) | | | | | AD Converter Trigger |
| | | FRCKn(_R) | | | | | Free Running Timer external clock |
| | | INn(_R) | | | | | Input Capture |

Note : Relocated Resource Inputs have same characteristics



## Bus Timing (Read)

($T_A$ = –40°C to +125°C, $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $IO_{drive}$ = 5mA, $C_L$ = 50pF)

| Parameter | Symbol | Pin | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| ALE pulse width (multiplexed) | $t_{LHLL}$ | ALE | EACL:STS=0 and EACL:ACE=0 | $t_{CYC}/2 - 5$ | — | ns | |
| | | | EACL:STS=1 | $t_{CYC} - 5$ | — | | |
| | | | EACL:STS=0 and EACL:ACE=1 | $3t_{CYC}/2 - 5$ | — | | |
| Valid address ⇒ ALE ↓ time (multiplexed) | $t_{AVLL}$ | ALE, A[23:16], | EACL:STS=0 and EACL:ACE=0 | $t_{CYC} - 15$ | — | ns | EBM:NMS = 0 |
| | | | EACL:STS=1 and EACL:ACE=0 | $3t_{CYC}/2 - 15$ | — | | |
| | | | EACL:STS=0 and EACL:ACE=1 | $2t_{CYC} - 15$ | — | | |
| | | | EACL:STS=1 and EACL:ACE=1 | $5t_{CYC}/2 - 15$ | — | | |
| | $t_{ADVLL}$ | ALE,AD[15:0] | EACL:STS=0 and EACL:ACE=0 | $t_{CYC}/2 - 15$ | — | ns | |
| | | | EACL:STS=1 and EACL:ACE=0 | $t_{CYC} - 15$ | — | | |
| | | | EACL:STS=0 and EACL:ACE=1 | $3t_{CYC}/2 - 15$ | — | | |
| | | | EACL:STS=1 and EACL:ACE=1 | $2t_{CYC} - 15$ | — | | |
| ALE ↓ ⇒ Address valid time (multiplexed) | $t_{LLAX}$ | ALE, AD[15:0] | EACL:STS=0 | $t_{CYC}/2 - 15$ | — | ns | |
| | | | EACL:STS=1 | -15 | — | | |
| Valid address ⇒ RDX ↓ time (non-multiplexed) | $t_{AVRL}$ | RDX, A[23:0] | EBM:NMS= 1 | $t_{CYC}/2 - 15$ | — | ns | |
| Valid address ⇒ RDX ↓ time (multiplexed) | $t_{AVRL}$ | RDX, A[23:16] | EACL:ACE=0 EBM:NMS=0 | $3t_{CYC}/2 - 15$ | — | ns | |
| | | | EACL:ACE=1 EBM:NMS=0 | $5t_{CYC}/2 - 15$ | — | | |
| | $t_{ADVRL}$ | RDX, AD[15:0] | EACL:ACE=0 EBM:NMS=0 | $t_{CYC} - 15$ | — | ns | |
| | | | EACL:ACE=1 EBM:NMS=0 | $2t_{CYC} - 15$ | — | | |
| Valid address ⇒ Valid data input (non-multiplexed) | $t_{AVDV}$ | A[23:0], AD[15:0] | EBM:NMS= 1 | — | $2t_{CYC} - 55$ | ns | w/o cycle extension |

($T_A$ = −40°C to +125°C, $V_{CC}$ = 3.0 to 4.5V, $V_{SS}$ = 0.0 V, $IO_{drive}$ = 5mA, $C_L$ = 50pF)

| Parameter | Sym-bol | Pin | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Valid address ⇒ Valid data input (multiplexed) | $t_{AVDV}$ | A[23:16], AD[15:0] | EACL:ACE=0 EBM:NMS=0 | — | $3t_{CYC}$ − 60 | ns | w/o cycle extension |
| | | | EACL:ACE=1 EBM:NMS=0 | — | $4t_{CYC}$ − 60 | | |
| | $t_{AD-VDV}$ | AD[15:0] | EACL:ACE=0 EBM:NMS=0 | — | $5t_{CYC}/2$ − 60 | ns | w/o cycle extension |
| | | | EACL:ACE=1 EBM:NMS=0 | — | $7t_{CYC}/2$ − 60 | | |
| RDX pulse width | $t_{RLRH}$ | RDX | — | $3t_{CYC}/2$ − 8 | — | ns | w/o cycle extension |
| RDX ↓ ⇒ Valid data input | $t_{RLDV}$ | RDX, AD[15:0] | — | — | $3t_{CYC}/2$ − 55 | ns | w/o cycle extension |
| RDX ↑ ⇒ Data hold time | $t_{RHDX}$ | RDX, AD[15:0] | — | 0 | — | ns | |
| Address valid ⇒ Data hold time | $t_{AXDX}$ | A[23:0] | — | 0 | — | ns | |
| RDX ↑ ⇒ ALE ↑ time | $t_{RHLH}$ | RDX, ALE | EACL:STS=1 and EACL:ACE=1 | $3t_{CYC}/2$ − 15 | — | ns | |
| | | | other ECL:STS, EACL:ACE setting | $t_{CYC}/2$ − 15 | — | | |
| Valid address ⇒ ECLK ↑ time | $t_{AVCH}$ | A[23:0], ECLK | — | $t_{CYC}$ − 20 | — | ns | |
| | $t_{AD-VCH}$ | AD[15:0], ECLK | | $t_{CYC}/2$ − 20 | — | | |
| RDX ↓ ⇒ ECLK ↑ time | $t_{RLCH}$ | RDX, ECLK | — | $t_{CYC}/2$ − 15 | — | ns | |
| ALE ↓ ⇒ RDX ↓ time | $t_{LLRL}$ | ALE, RDX | EACL:STS=0 | $t_{CYC}/2$ − 15 | — | ns | |
| | | | EACL:STS=1 | − 15 | — | | |
| ECLK↑ ⇒ Valid data input | $t_{CHDV}$ | AD[15:0], ECLK | — | — | $t_{CYC}$ − 55 | ns | |

### Ready Input Timing

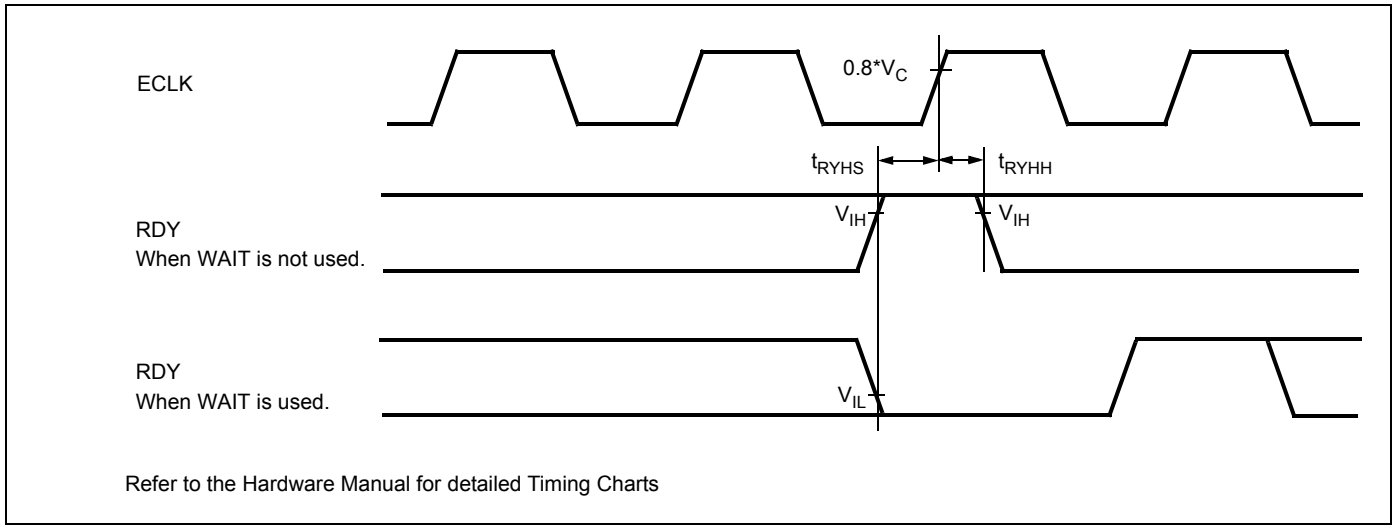
($T_A$ = –40°C to +125°C, $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $IO_{drive}$ = 5mA, $C_L$ = 50pF)

| Parameter | Symbol | Pin | Test Condition | Rated Value | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| RDY setup time | $t_{RYHS}$ | RDY | — | 35 | — | ns | |
| RDY hold time | $t_{RYHH}$ | RDY | | 0 | — | ns | |

($T_A$ = –40°C to +125°C, $V_{CC}$ = 3.0 to 4.5V, $V_{SS}$ = 0.0 V, $IO_{drive}$ = 5mA, $C_L$ = 50pF)

| Parameter | Symbol | Pin | Test Condition | Rated Value | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| RDY setup time | $t_{RYHS}$ | RDY | — | 45 | — | ns | |
| RDY hold time | $t_{RYHH}$ | RDY | | 0 | — | ns | |

Note : If the RDY setup time is insufficient, use the auto-ready function.




Refer to the Hardware Manual for detailed Timing Charts

## 15.5 Analog Digital Converter

($T_A$ = -40 °C to +125 °C, 3.0 V ≤ AVRH - AVRL, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V)

| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | - | - | - | - | 10 | bit | |
| Total error | - | - | -3 | - | +3 | LSB | |
| Nonlinearity error | - | - | -2.5 | - | +2.5 | LSB | |
| Differential nonlinearity error | - | - | -1.9 | - | +1.9 | LSB | |
| Zero reading voltage | $V_{OT}$ | ANn | AVRL-1.5 LSB | AVRL+0.5 LSB | AVRL+2.5 LSB | V | |
| Full scale reading voltage | $V_{FST}$ | ANn | AVRH-3.5 LSB | AVRH-1.5 LSB | AVRH+0.5 LSB | V | |
| Compare time | - | - | 1.0 | - | 16,500 | µs | 4.5V ≤ $AV_{CC}$ ≤ 5.5V |
| | | | 2.0 | - | - | µs | 3.0V ≤ $AV_{CC}$ < 4.5V |
| Sampling time | - | - | 0.5 | - | - | µs | 4.5V ≤ $AV_{CC}$ ≤ 5.5V |
| | | | 1.2 | - | - | µs | 3.0V ≤ $AV_{CC}$ < 4.5V |
| Analog port input current | $I_{AIN}$ | ANn | -3 | - | +3 | µA | $AV_{SS}$, AVRL < $V_I$ < $AV_{CC}$, AVRH |
| Analog input leakage current (during conversion) | $I_{AIN}$ | ANn | -1 | - | +1 | µA | $T_A$ = 25 ·C, $AV_{SS}$, AVRL < $V_I$ < $AV_{CC}$, AVRH |
| | | | -3 | - | +3 | µA | $T_A$ = 125 ·C, $AV_{SS}$, AVRL < $V_I$ < $AV_{CC}$, AVRH |
| Analog input voltage range | $V_{AIN}$ | ANn | AVRL | - | AVRH | V | |
| Reference voltage range | AVRH | AVRH/AVRH2 | 0.75 AVcc | - | AVcc | V | |
| | AVRL | AVRL | $AV_{SS}$ | - | 0.25 $AV_{CC}$ | V | |
| Power supply current | $I_A$ | AVcc | - | 2.5 | 5 | mA | A/D Converter active |
| | $I_{AH}$ | AVcc | - | - | 5 | µA | A/D Converter not operated |
| Reference voltage current | $I_R$ | AVRH/AVRL | - | 0.7 | 1 | mA | A/D Converter active |
| | $I_{RH}$ | AVRH/AVRL | - | - | 5 | µA | A/D Converter not operated |
| Offset between input channels | - | ANn | - | - | 4 | LSB | |

Note: The accuracy gets worse as |AVRH - AVRL| becomes smaller.

## 15.7 Low Voltage Detector characteristics

($T_A$ = -40 °C to +125 °C, $V_{cc}$ = $AV_{cc}$ = 3.0V - 5.5V, $V_{ss}$ = $AV_{ss}$ = 0V)

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Stabilization time | $T_{LVDSTAB}$ | - | 75 | µs | After power-up or change of detection level |
| Level 0 | $V_{DL0}$ | 2.7 | 2.9 | V | CILCR:LVL[3:0]="0000" |
| Level 1 | $V_{DL1}$ | 2.9 | 3.1 | V | CILCR:LVL[3:0]="0001" |
| Level 2 | $V_{DL2}$ | 3.1 | 3.3 | V | CILCR:LVL[3:0]="0010" |
| Level 3 | $V_{DL3}$ | 3.5 | 3.75 | V | CILCR:LVL[3:0]="0011" |
| Level 4 | $V_{DL4}$ | 3.6 | 3.85 | V | CILCR:LVL[3:0]="0100" |
| Level 5 | $V_{DL5}$ | 3.7 | 3.95 | V | CILCR:LVL[3:0]="0101" |
| Level 6 | $V_{DL6}$ | 3.8 | 4.05 | V | CILCR:LVL[3:0]="0110" |
| Level 7 | $V_{DL7}$ | 3.9 | 4.15 | V | CILCR:LVL[3:0]="0111" |
| Level 8 | $V_{DL8}$ | 4.0 | 4.25 | V | CILCR:LVL[3:0]="1000" |
| Level 9 | $V_{DL9}$ | 4.1 | 4.35 | V | CILCR:LVL[3:0]="1001" |
| Level 10 | $V_{DL10}$ | not used | | | |
| Level 11 | $V_{DL11}$ | not used | | | |
| Level 12 | $V_{DL12}$ | not used | | | |
| Level 13 | $V_{DL13}$ | not used | | | |
| Level 14 | $V_{DL14}$ | not used | | | |
| Level 15 | $V_{DL15}$ | not used | | | |

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

Levels 10 to 15 are not used in this device.

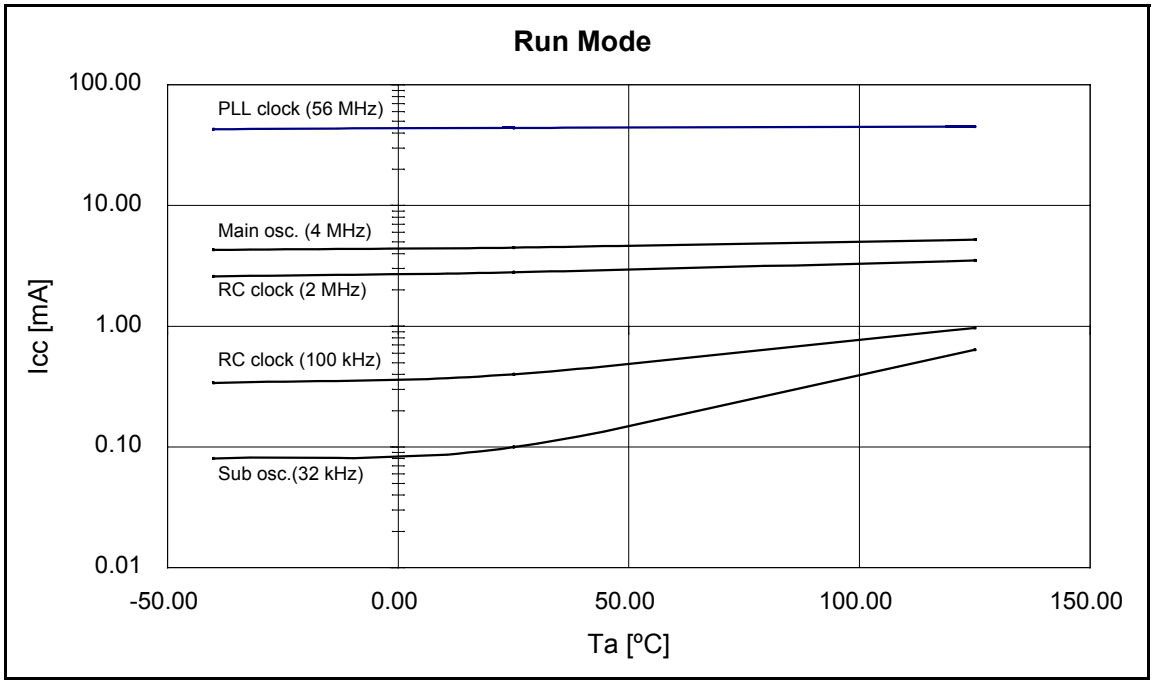
For correct detection, the slope of the voltage level must satisfy $\left|\frac{dV}{dt}\right| \leq 0.004 \frac{V}{\mu s}$.

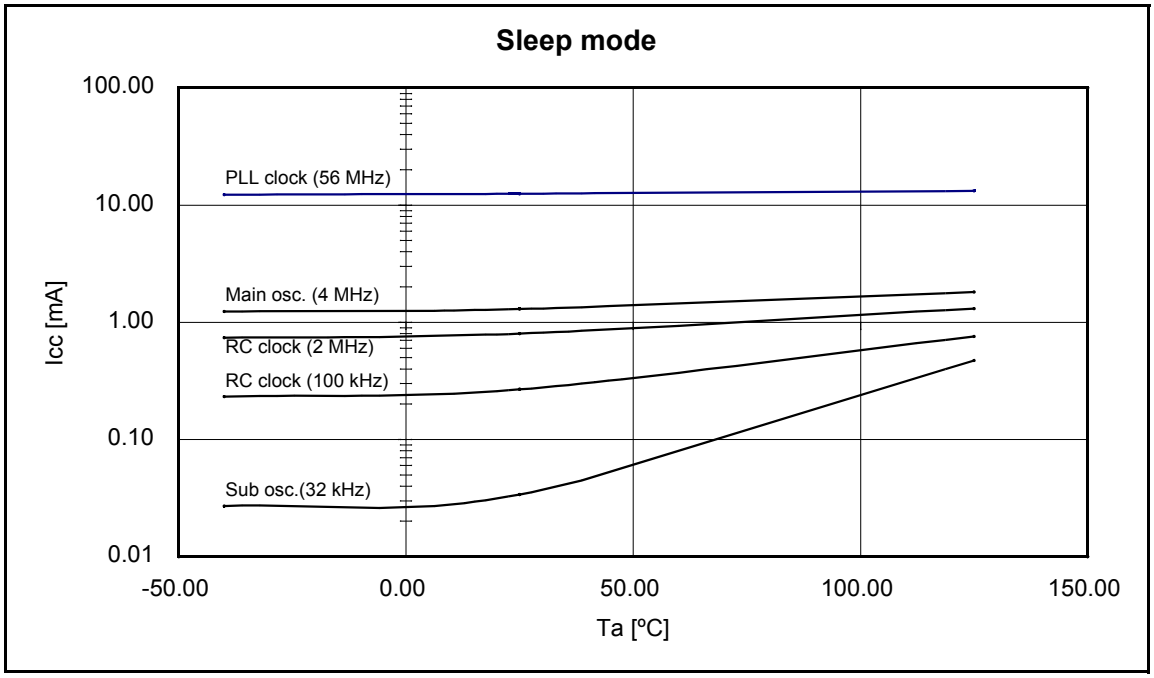
Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of Vcc = 2.7V. The electrical characteristics however are only valid in the specified range (usually down to 3.0V).

## 16. Example Characteristics

The diagrams below show the characteristics of one measured sample with typical process parameters.



## 18. Ordering Information

| Part number | Flash/ROM | Subclock | Persistent Low Voltage Reset | Package |
|---|---|---|---|---|
| MB96384YSB PMC-GSE2 *1 | ROM (128KB) | No | Yes | 120 pin Plastic LQFP (FPT-120P-M21) |
| MB96384RSB PMC-GSE2 *1 | | | No | |
| MB96384YWB PMC-GSE2 *1 | | Yes | Yes | |
| MB96384RWB PMC-GSE2 *1 | | | No | |
| MB96385YSB PMC-GSE2 *1 | ROM (160KB) | No | Yes | 120 pin Plastic LQFP (FPT-120P-M21) |
| MB96385RSB PMC-GSE2 *1 | | | No | |
| MB96385YWB PMC-GSE2 *1 | | Yes | Yes | |
| MB96385RWB PMC-GSE2 *1 | | | No | |
| MB96F385YSA PMC-GSE2 *1 | Flash A (160KB) | No | Yes | 120 pin Plastic LQFP (FPT-120P-M21) |
| MB96F385RSA PMC-GSE2 *1 | | | No | |
| MB96F385YWA PMC-GSE2 *1 | | Yes | Yes | |
| MB96F385RWA PMC-GSE2 *1 | | | No | |
| MB96F386YSB PMC-GSE2 | Flash A (288KB) | No | Yes | 120 pin Plastic LQFP (FPT-120P-M21) |
| MB96F386RSB PMC-GSE2 | | | No | |
| MB96F386YWB PMC-GSE2 | | Yes | Yes | |
| MB96F386RWB PMC-GSE2 | | | No | |
| MB96F387YSB PMC-GSE2 | Flash A (416KB) | No | Yes | 120 pin Plastic LQFP (FPT-120P-M21) |
| MB96F387RSB PMC-GSE2 | | | No | |
| MB96F387YWB PMC-GSE2 | | Yes | Yes | |
| MB96F387RWB PMC-GSE2 | | | No | |
| MB96F388TSA PMC-GSE2 *1 | Flash A (544KB) Flash B (32KB) | No | Yes | 120 pin Plastic LQFP (FPT-120P-M21) |
| MB96F388HSA PMC-GSE2 *1 | | | No | |
| MB96F388TWA PMC-GSE2 *1 | | Yes | Yes | |
| MB96F388HWA PMC-GSE2 *1 | | | No | |
| MB96F389YSA PMC-GSE2 *1 | Flash A (544KB) Flash B (288kB) | No | Yes | 120 pin Plastic LQFP (FPT-120P-M21) |
| MB96F389RSA PMC-GSE2 *1 | | | No | |
| MB96F389YWA PMC-GSE2 *1 | | Yes | Yes | |
| MB96F389RWA PMC-GSE2 *1 | | | No | |
| MB96V300BRB-ES (for evaluation) | Emulated by ext. RAM | Yes | No | 416 pin Plastic BGA (BGA-416P-M02) |

*1: These devices are under development and specification is preliminary. These products under development may change its specification without notice.

**This datasheet is also valid for the following outdated devices:**

MB96F386YSA, MB96F386RSA, MB96F386YWA, MB96F386RWA,
MB96F387YSA, MB96F387RSA, MB96F387YWA, MB96F387RWA

## 19. Revision History

**Spansion Publication Number: DS07-13803-2E**

| Revision | Date | Modification |
|---|---|---|
| Prelim 1 | 2007-05-2 | Creation |
| Prelim 2 | 2007-05-24 | Electrical characteristics and memory description updates |
| Prelim 3 | 2007-08-09 | Typo errors corrections, Flash memory programming interface update |
| Prelim 4 | 2007-08-31 | Update of DC characteristics. new MB96F388 and MB96F389 added. LVD chapter added as well as an example characteristics chapter |
| Prelim 5 | 2007-09-06 | Updates of the DC characteristics, interrupt vector table update, update of the LVD characteristics |
| Prelim 6 | 2007-11-14 | Memory map for external bus modified. Modifications of the drawing of the pin circuits. Electrical characteristics updates. Rephrasing and typos corrections. Add Slew rate high current outputs chapter.<br>Modification of the block diagram.<br>Memory map modified for Flash. RAM memory map added.<br>Pin circuit type corrected. Type L IO is now included. |
| Prelim 7 | 2007-12-12 | Memory IO map modified<br>New Flash/ROM configuration presentation<br>Ordering information: MB96300B used as reference.<br>Block diagram modified to included relocated pins.<br>Main Flash becomes Flash memory A and Satellite flash becomes Flash memory B |
| Prelim 8 | 2008-02-04 | • Devices under development added: MB96384/385/F385/F388/F389<br>• Block diagram corrected (existing resource pins)<br>• Pin assignment: TTG8 -> TTG7<br>• Pin function table corrected<br>• I/O circuit type diagrams corrected<br>• Memory map cleaned up<br>• "Flash sector configuration" replaced by corrected "User ROM Memory map for Flash devices", “ROM configuration” replaced by “User ROM Memory map for Mask ROM devices”<br>• IO map table regenerated:<br>- Port register: Naming style corrected<br>- Memory control registers renamed (Main/Sat -> A/B)<br>- addresses after 000BFFh removed<br>• Absolute maximum ratings: Pd and Ta specified more precisely<br>• Run and Sleep mode currents: more conditions added (1WS settings)<br>• Run mode current spec in 48/24MHz mode corrected<br>• Maximum CLKP2 frequency for MB96F386/F387 corrected<br>• High current port input capacitance added<br>• External bus timings: missing conditions added and readability improved<br>• Alarm comparator spec updated (transition voltages defined)<br>• MB96V300A removed<br>• Ordering information updated<br>• Typos and formatting corrected |

| Revision | Date | Modification |
|---|---|---|
| 9 | 2009-01-09 | • Format adjusted to official Fujitsu Microelectronics datasheet standard (mainly style changes and official notes and disclaimer added)<br>• Numbering of Electrical Characteristics subchapters automated<br>• Note about devices under development modified<br>• I/O map: Note added about reserved addresses<br>• Serial programming interface: Note about handshaking pins improved<br>• ICCPLL for CLKS1/2=80MHz, CLKB=40MHz (F388/F389) increased by 5mA<br>• ICCSPLL for CLKS1/2=80MHz, CLKB=40MHz (F388/F389) increased by 0.8mA (typ) and 1.3mA (max)<br>• Updated ordering information: MB96384/385**A -> MB96384/385**B<br>• Package code of MB96V300 corrected in ordering information<br>• Internal LCD divider resistance value corrected: Typ 35kOhm -> 40kOhm, Max 50kOhm -> 65kOhm<br>• Run and Sleep mode currents of ROM devices (MB96384/385) reduced<br>• Added voltage condition to pull-up resistance and LCD divide resistance spec<br>• Lineup: Term “Data Flash” replaced by “independent 32KB Flash”<br>• Ordering information: column “Independent 32KB Data Flash” replaced by new column “Flash/ROM”, column “Remarks” removed<br>• Official package dimension drawing with additional notes added<br>• Empty pages removed<br>• MB96384/385 and MB96F385/F388/F389 separated in DC spec and currents of these devices adjusted according to first evaluation results<br>• Alarm comparator: Power supply current max values increased, comparison time reduced, mode transition time and power-up stabilization time newly added<br>• Handling devices: Notes added about Serial communication and about using ceramic resonators.<br>• Feature list and AC Characteristics: 16MHz maximum frequency is valid for crystal oscillators. For resonators, maximum frequency depends on Q-factor<br>• AC characteristics: PLL phase skew spec added, CLKVCO min=64MHz<br>• VOL3 spec improved: spec valid for 3mA load for full Vcc range<br>• C-Pin cap spec updated: 4.7uF-10uF capacitor with tolerance permitted<br>• “Preliminary” watermark removed |

**NOTE: Please see “Document History” about later revised information.**