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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	CANbus, LINbusSCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f561k9tae

Address	Block	Register Label	Register Name	Reset Status	Remarks
0048h 0049h 004Ah 004Bh 004Ch 004Dh 004Eh 004Fh	LINSCI1 (LIN Master/ Slave)	SCI1ISR SCI1DR SCI1BRR SCI1CR1 SCI1CR2 SCI1CR3 SCI1ERPR SCI1ETPR	SCI1 Status Register SCI1 Data Register SCI1 Baud Rate Register SCI1 Control Register 1 SCI1 Control Register 2 SCI1 Control Register 3 SCI1 Extended Receive Prescaler Register SCI1 Extended Transmit Prescaler Register	C0h xxh 00h xxh 00h 00h 00h 00h	Read Only R/W R/W R/W R/W R/W R/W R/W
0050h	Reserved Area (1 byte)				
0051h 0052h 0053h 0054h 0055h 0056h 0057h 0058h 0059h 005Ah 005Bh 005Ch 005Dh 005Eh 005Fh	16-BIT TIMER	T16CR2 T16CR1 T16CSR T16IC1HR T16IC1LR T16OC1HR T16OC1LR T16CHR T16CLR T16ACHR T16ACLR T16IC2HR T16IC2LR T16OC2HR T16OC2LR	Timer Control Register 2 Timer Control Register 1 Timer Control/Status Register Timer Input Capture 1 High Register Timer Input Capture 1 Low Register Timer Output Compare 1 High Register Timer Output Compare 1 Low Register Timer Counter High Register Timer Counter Low Register Timer Alternate Counter High Register Timer Alternate Counter Low Register Timer Input Capture 2 High Register Timer Input Capture 2 Low Register Timer Output Compare 2 High Register Timer Output Compare 2 Low Register	00h 00h 00h xxh xxh 80h 00h FFh FCh FFh FCh xxh xxh 80h 00h	R/W R/W R/W Read Only Read Only R/W R/W Read Only Read Only Read Only Read Only Read Only R/W R/W
0060h 0061h 0062h 0063h 0064h 0065h 0066h 0067h	LINSCI2 (LIN Master)	SCI2SR SCI2DR SCI2BRR SCI2CR1 SCI2CR2 SCI2CR3 SCI2ERPR SCI2ETPR	SCI2 Status Register SCI2 Data Register SCI2 Baud Rate Register SCI2 Control Register 1 SCI2 Control Register 2 SCI2 Control Register 3 SCI2 Extended Receive Prescaler Register SCI2 Extended Transmit Prescaler Register	C0h xxh 00h xxh 00h 00h 00h 00h	Read Only R/W R/W R/W R/W R/W R/W R/W

FLASH PROGRAM MEMORY (Cont'd)

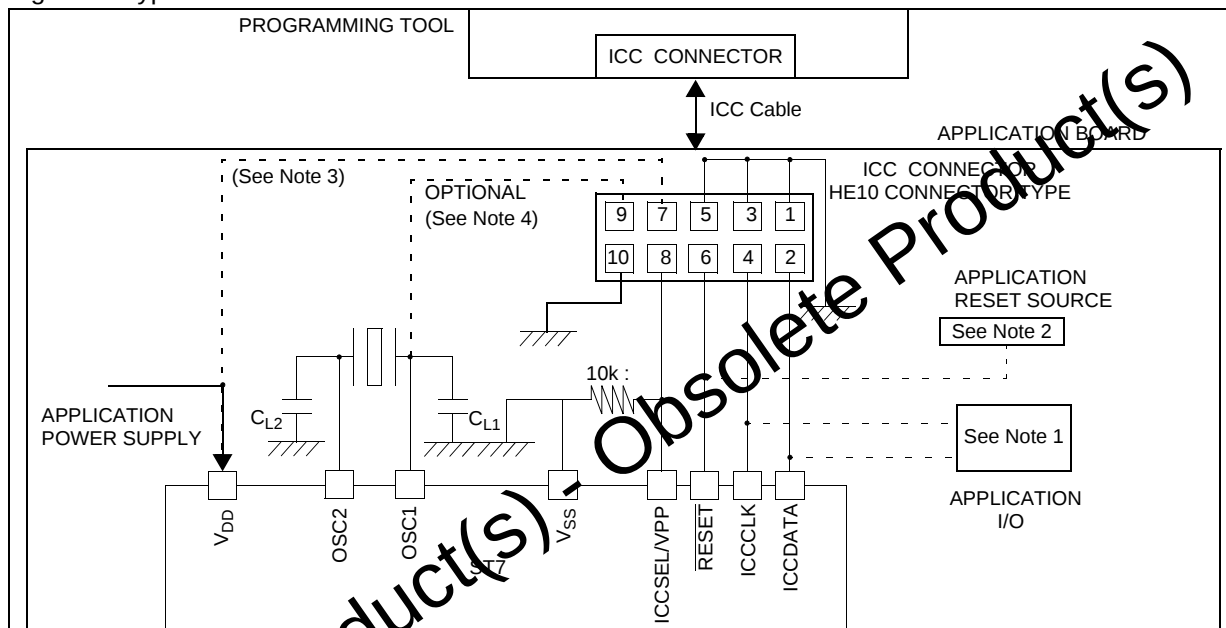
4.4 ICC INTERFACE

ICC (In-Circuit Communication) needs a minimum of four and up to six pins to be connected to the programming tool (see Figure 7). These pins are:

- $\overline{\text{RESET}}$: device reset
- V_{SS} : device power supply ground

- ICCCLK: ICC output serial clock pin
- ICCDATA: ICC input/output serial data pin
- ICCSEL/ V_{PP} : programming voltage
- OSC1(or OSCIN): main clock input for external source (optional)
- V_{DD} : application board power supply (see Figure 7, Note 3)

Figure 7. Typical ICC Interface



Notes:

1. If the ICCCLK or ICCDATA pins are only used as outputs in the application, no signal isolation is necessary. As soon as the Programming Tool is plugged to the board, even if an ICC session is not in progress, the ICCCLK and ICCDATA pins are not available for the application. If they are used as inputs by the application, isolation such as a serial resistor has to be implemented in case another device forces the signal. Refer to the Programming Tool documentation for recommended resistor values.

2. During the ICC session, the programming tool must control the $\overline{\text{RESET}}$ pin. This can lead to conflicts between the programming tool and the application reset circuit if it drives more than 5mA at high level (push pull output or pull-up resistor < 1K). A schottky diode can be used to isolate the application $\overline{\text{RESET}}$ circuit in this case. When using a classical RC network with $R > 1K$ or a reset man-

agement IC with open drain output and pull-up resistor > 1K, no additional components are needed. In all cases the user must ensure that no external reset is generated by the application during the ICC session.

3. The use of Pin 7 of the ICC connector depends on the Programming Tool architecture. This pin must be connected when using most ST Programming Tools (it is used to monitor the application power supply). Please refer to the Programming Tool manual.

4. Pin 9 has to be connected to the OSC1 or OSCIN pin of the ST7 when the clock is not available in the application or if the selected clock option is not programmed in the option byte. ST7 devices with multi-oscillator capability need to have OSC2 grounded in this case.

INTERRUPTS (Cont'd)

Table 8. Dedicated Interrupt Instruction Set

Instruction	New Description	Function/Example	I1	H	I0	N	Z	C
HALT	Entering Halt mode		1		0			
IRET	Interrupt routine return	Pop CC, A, X, PC	I1	H	I0	N	Z	C
JRM	Jump if I1:0 = 11 (level 3)	I1:0 = 11 ?						
JRNM	Jump if I1:0 <> 11	I1:0 <> 11 ?						
POP CC	Pop CC from the Stack	Mem => CC	I1	H	I0	N	Z	C
RIM	Enable interrupt (level 0 set)	Load I0 in I1:0 of CC	1		0			
SIM	Disable interrupt (level 3 set)	Load I1 in I1:0 of CC	1		1			
TRAP	Software trap	Software NMI	1		1			
WFI	Wait for interrupt		1		1			

Note : During the execution of an interrupt routine, the HALT, POPCC, RIM, SIM and WFI instructions change the current software priority up to the next IRET instruction or one of the previously mentioned instructions.

PWM AUTO-RELOAD TIMER (Cont'd)

10.3.2 Functional Description

Counter

The free running 8-bit counter is fed by the output of the prescaler, and is incremented on every rising edge of the clock signal.

It is possible to read or write the contents of the counter on the fly by reading or writing the Counter Access register (ARTCAR).

When a counter overflow occurs, the counter is automatically reloaded with the contents of the ARTARR register (the prescaler is not affected).

Counter clock and prescaler

The counter clock frequency is given by:

$$f_{\text{COUNTER}} = f_{\text{INPUT}} / 2^{\text{CC}[2:0]}$$

The timer counter's input clock (f_{INPUT}) feeds the 7-bit programmable prescaler, which selects one of the eight available taps of the prescaler, as defined by CC[2:0] bits in the Control/Status Register (ARTCSR). Thus the division factor of the prescaler can be set to 2^n (where $n = 0, 1, \dots, 7$).

This f_{INPUT} frequency source is selected through the EXCL bit of the ARTCSR register and can be either the f_{CPU} or an external input frequency f_{EXT} . The clock input to the counter is enabled by the TCE (Timer Counter Enable) bit in the ARTCSR register. When TCE is reset, the counter is stopped and the prescaler and counter contents are frozen. When TCE is set, the counter runs at the rate of the selected clock source.

Counter and Prescaler Initialization

After RESET, the counter and the prescaler are cleared and $f_{\text{INPUT}} = f_{\text{CPU}}$.

The counter can be initialized by:

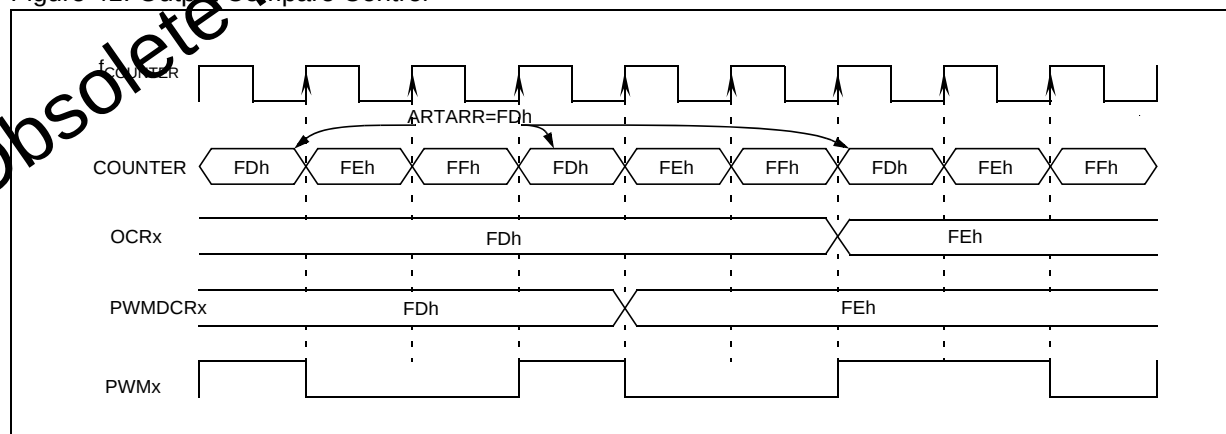
- Writing to the ARTARR register and then setting the FCRL (Force Counter Re-Load) and the TCE (Timer Counter Enable) bits in the ARTCSR register.
- Writing to the ARTCAR counter access register. In both cases the 7-bit prescaler is also cleared, whereupon counting will start from a known value. Direct access to the prescaler is not possible.

Output compare control

The timer compare function is based on four different comparisons with the counter (one for each PWMx output). Each comparison is made between the counter value and an output compare register (OCRx) value. This OCRx register can not be accessed directly, it is loaded from the duty cycle register (PWMDCRx) at each overflow of the counter.

This double buffering method avoids glitch generation when changing the duty cycle on the fly.

Figure 41. Output Compare Control



16-BIT TIMER (Cont'd)

Figure 52. Input Capture Block Diagram

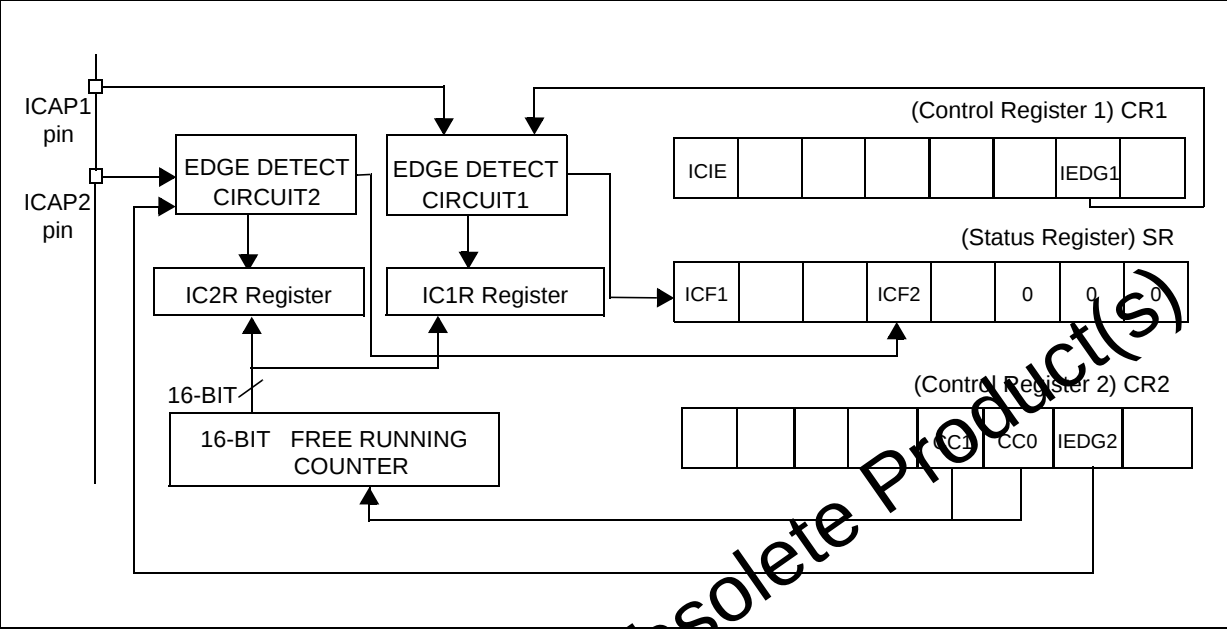
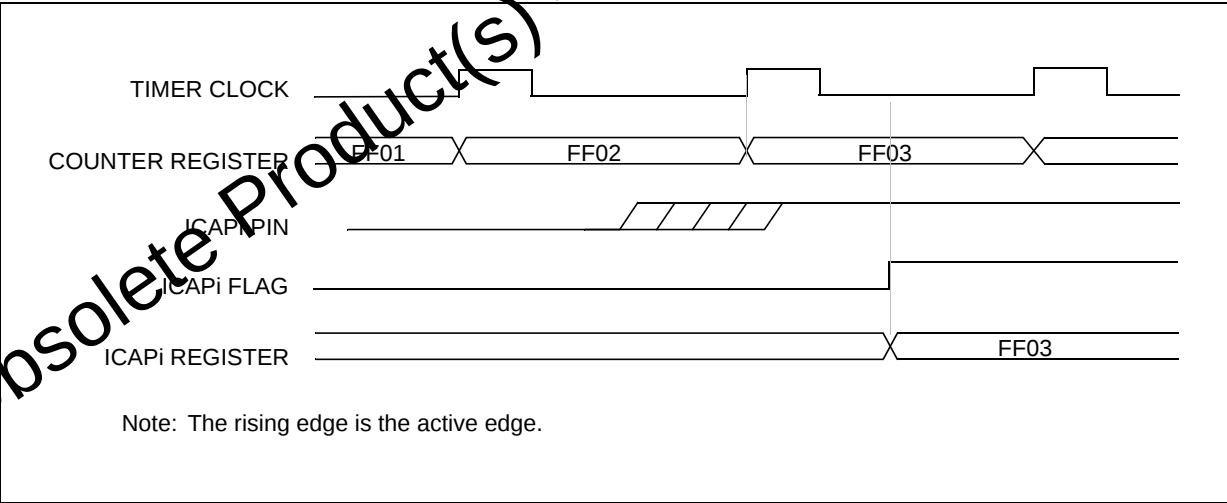


Figure 53. Input Capture Timing Diagram



8-BIT TIMER (Cont'd)

10.5.3.4 One Pulse Mode

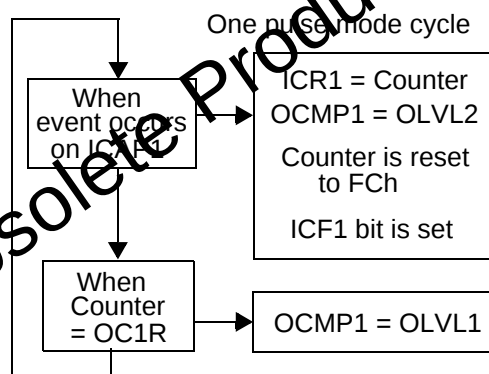
One Pulse mode enables the generation of a pulse when an external event occurs. This mode is selected via the OPM bit in the CR2 register.

The one pulse mode uses the Input Capture1 function and the Output Compare1 function.

Procedure:

To use one pulse mode:

1. Load the OC1R register with the value corresponding to the length of the pulse (see the formula in the opposite column).
2. Select the following in the CR1 register:
 - Using the OLVL1 bit, select the level to be applied to the OCMP1 pin after the pulse.
 - Using the OLVL2 bit, select the level to be applied to the OCMP1 pin during the pulse.
 - Select the edge of the active transition on the ICAP1 pin with the IEDG1 bit (the ICAP1 pin must be configured as floating input).
3. Select the following in the CR2 register:
 - Set the OC1E bit, the OCMP1 pin is then dedicated to the Output Compare 1 function.
 - Set the OPM bit.
 - Select the timer clock CC[1:0] (see Table 19 Clock Control Bits).



Then, on a valid event on the ICAP1 pin, the counter is initialized to FCh and OLVL2 bit is loaded on the OCMP1 pin, the ICF1 bit is set and the value FFFDh is loaded in the IC1R register.

Because the ICF1 bit is set when an active edge occurs, an interrupt can be generated if the ICIE bit is set.

Clearing the Input Capture interrupt request (that is, clearing the ICFi bit) is done in two steps:

1. Reading the SR register while the ICFi bit is set.
2. An access (read or write) to the ICiLR register.

The OC1R register value required for a specific timing application can be calculated using the following formula:

$$\text{OCiR Value} = \frac{t * f_{\text{CPU}}}{\text{PRESC}} - 5$$

Where:

t = Pulse period (in seconds)

f_{CPU} = PLL output x2 clock frequency in hertz (or f_{OSC}/2 if PLL is not enabled)

PRESC = Timer prescaler factor (2, 4, 8 or 8000 depending on the CC[1:0] bits, see Table 19 Clock Control Bits)

When the value of the counter is equal to the value of the contents of the OC1R register, the OLVL1 bit is output on the OCMP1 pin, (See Figure 68).

Notes:

1. The OCF1 bit cannot be set by hardware in one pulse mode but the OCF2 bit can generate an Output Compare interrupt.
2. When the Pulse Width Modulation (PWM) and One Pulse Mode (OPM) bits are both set, the PWM mode is the only active one.
3. If OLVL1=OLVL2 a continuous signal will be seen on the OCMP1 pin.
4. The ICAP1 pin can not be used to perform input capture. The ICAP2 pin can be used to perform input capture (ICF2 can be set and IC2R can be loaded) but the user must take care that the counter is reset each time a valid edge occurs on the ICAP1 pin and ICF1 can also generates interrupt if ICIE is set.
5. When one pulse mode is used OC1R is dedicated to this mode. Nevertheless OC2R and OCF2 can be used to indicate a period of time has been elapsed but cannot generate an output waveform because the level OLVL2 is dedicated to the one pulse mode.

SERIAL PERIPHERAL INTERFACE (cont'd)

10.6.4 Clock Phase and Clock Polarity

Four possible timing relationships may be chosen by software, using the CPOL and CPHA bits (See Figure 74).

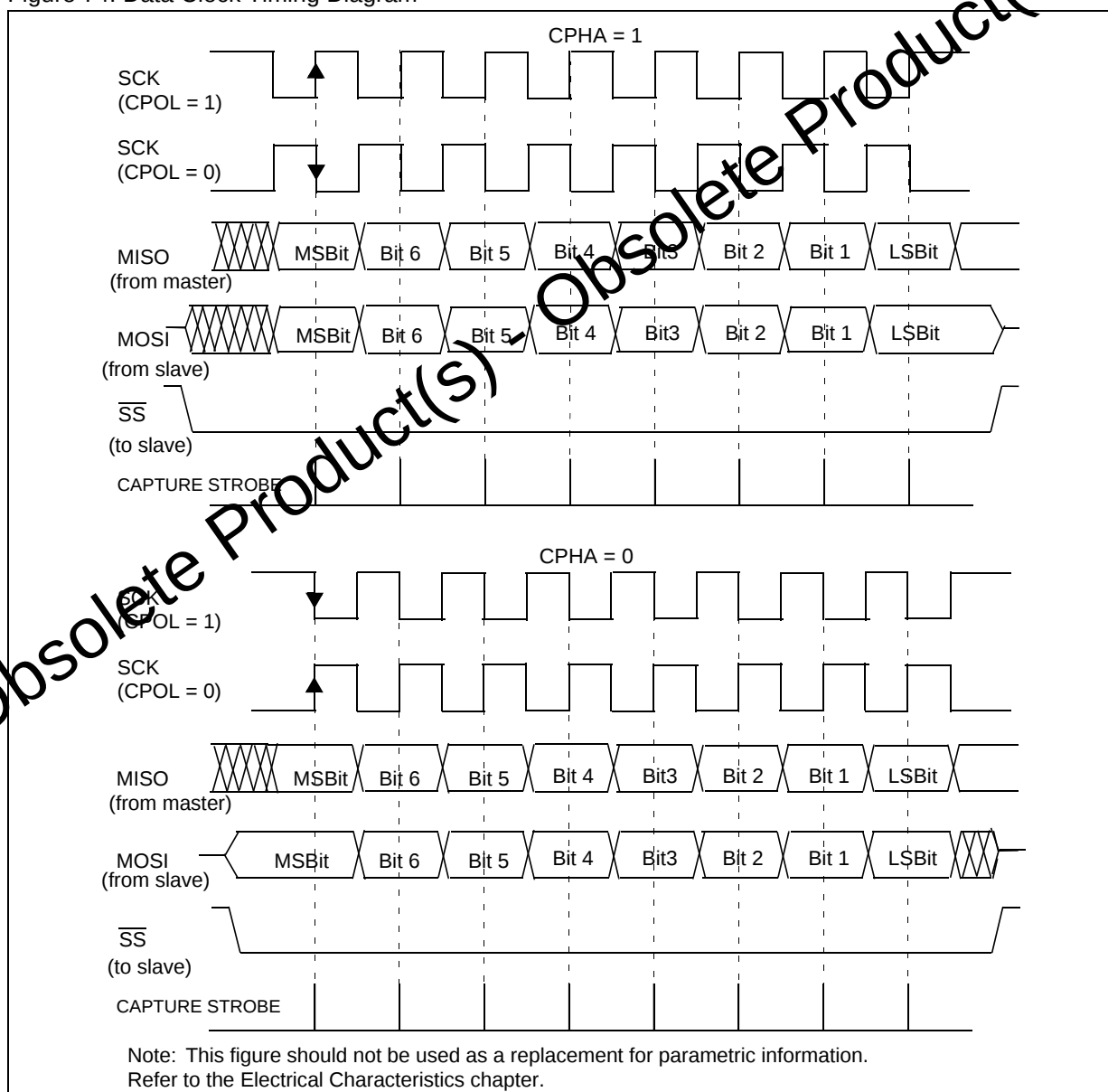
Note: The idle state of SCK must correspond to the polarity selected in the SPICSR register (by pulling up SCK if CPOL = 1 or pulling down SCK if CPOL = 0).

The combination of the CPOL clock polarity and CPHA (clock phase) bits selects the data capture clock edge.

Figure 74 shows an SPI transfer with the four combinations of the CPHA and CPOL bits. The diagram may be interpreted as a master or slave timing diagram where the SCK pin, the MISO pin and the MOSI pin are directly connected between the master and the slave device.

Note: If CPOL is changed at the communication byte boundaries, the SPI must be disabled by resetting the SPE bit.

Figure 74. Data Clock Timing Diagram



10.6.8 Register Description

SPI CONTROL REGISTER (SPICR)

Read/Write

Reset Value: 0000 xxxx (0xh)

7							0
SPIE	SPE	SPR2	MSTR	CPOL	CPHA	SPR1	SPR0

Bit 7 = SPIE Serial Peripheral Interrupt Enable

This bit is set and cleared by software.

0: Interrupt is inhibited

1: An SPI interrupt is generated whenever an End of Transfer event, Master Mode Fault or Over-run error occurs (SPIF = 1, MODF = 1 or OVR = 1 in the SPICSR register)

Bit 6 = SPE Serial Peripheral Output Enable

This bit is set and cleared by software. It is also cleared by hardware when, in master mode, $SS = 0$ (see Section 10.6.5.1 "Master Mode Fault (MODF)"). The SPE bit is cleared by reset, so the SPI peripheral is not initially connected to the external pins.

0: I/O pins free for general purpose I/O

1: SPI I/O pin alternate functions enabled

Bit 5 = SPR2 Divider Enable

This bit is set and cleared by software and is cleared by reset. It is used with the SPR[1:0] bits to set the baud rate. Refer to Table 20 SPI Master Mode SCK Frequency.

0: Divider by 2 enabled

1: Divider by 2 disabled

Note: This bit has no effect in slave mode.

Bit 4 = MSTR Master Mode

This bit is set and cleared by software. It is also cleared by hardware when, in master mode, $SS = 0$ (see Section 10.6.5.1 "Master Mode Fault (MODF)").

0: Slave mode

1: Master mode. The function of the SCK pin changes from an input to an output and the functions of the MISO and MOSI pins are reversed.

Bit 3 = CPOL Clock Polarity

This bit is set and cleared by software. This bit determines the idle state of the serial Clock. The CPOL bit affects both the master and slave modes.

0: SCK pin has a low level idle state

1: SCK pin has a high level idle state

Note: If CPOL is changed at the communication byte boundaries, the SPI must be disabled by re-setting the SPE bit.

Bit 2 = CPHA Clock Phase

This bit is set and cleared by software.

0: The first clock transition is the first data capture edge.

1: The second clock transition is the first capture edge.

Note: The slave must have the same CPOL and CPHA settings as the master.

Bits 1:0 = SPR[1:0] Serial Clock Frequency

These bits are set and cleared by software. Used with the SPR2 bit, they select the baud rate of the SPI serial clock SCK output by the SPI in master mode.

Note: These 2 bits have no effect in slave mode.

Table 21. SPI Master Mode SCK Frequency

Serial Clock	SPR2	SPR1	SPR0
$f_{CPU}/4$	1	0	0
$f_{CPU}/8$	0		1
$f_{CPU}/16$	1	1	0
$f_{CPU}/32$			1
$f_{CPU}/64$			0
$f_{CPU}/128$	0	0	1

LINSPI ¥ SERIAL COMMUNICATION INTERFACE (SCI Mode) (cont'd)

CONTROL REGISTER 2 (SCICR2)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
TIE	TCIE	RIE	ILIE	TE	RE	RWU ¹⁾	SBK ¹⁾

¹⁾This bit has a different function in LIN mode, please refer to the LIN mode register description.

Bit 7 = TIE Transmitter interrupt enable

This bit is set and cleared by software.

0: Interrupt is inhibited

1: In SCI interrupt is generated whenever TDRE = 1 in the SCISR register

Bit 6 = TCIE Transmission complete interrupt enable

This bit is set and cleared by software.

0: Interrupt is inhibited

1: An SCI interrupt is generated whenever TC = 1 in the SCISR register

Bit 5 = RIE Receiver interrupt enable

This bit is set and cleared by software.

0: Interrupt is inhibited

1: An SCI interrupt is generated whenever OR = 1 or RDRF = 1 in the SCISR register

Bit 4 = ILIE Idle line interrupt enable

This bit is set and cleared by software.

0: Interrupt is inhibited

1: An SCI interrupt is generated whenever IDLE = 1 in the SCISR register.

Bit 3 = TE Transmitter enable

This bit enables the transmitter. It is set and cleared by software.

0: Transmitter is disabled

1: Transmitter is enabled

Notes:

- During transmission, a “0” pulse on the TE bit (“0” followed by “1”) sends a preamble (idle line) after the current word.
- When TE is set there is a 1 bit-time delay before the transmission starts.

Bit 2 = RE Receiver enable

This bit enables the receiver. It is set and cleared by software.

0: Receiver is disabled in the SCISR register

1: Receiver is enabled and begins searching for a start bit

Bit 1 = RWU Receiver wake-up

This bit determines if the SCI is in mute mode or not. It is set and cleared by software and can be cleared by hardware when a wake-up sequence is recognized.

0: Receiver in active mode

1: Receiver in mute mode

Notes:

- Before selecting Mute mode (by setting the RWU bit) the SCI must first receive a data byte, otherwise it cannot function in Mute mode with wake-up by Idle line detection.
- In Address Mark Detection Wake-Up configuration (WAKE bit = 1) the RWU bit cannot be modified by software while the RDRF bit is set.

Bit 0 = SBK Send break

This bit is used to send break characters. It is set and cleared by software.

0: No break character is transmitted

1: Break characters are transmitted

Note: If the SBK bit is set to “1” and then to “0”, the transmitter will send a BREAK word at the end of the current word.

DATA REGISTER (SCIDR)

Read/Write

Reset Value: Undefined

Contains the Received or Transmitted data character, depending on whether it is read from or written to.

7							0
DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0

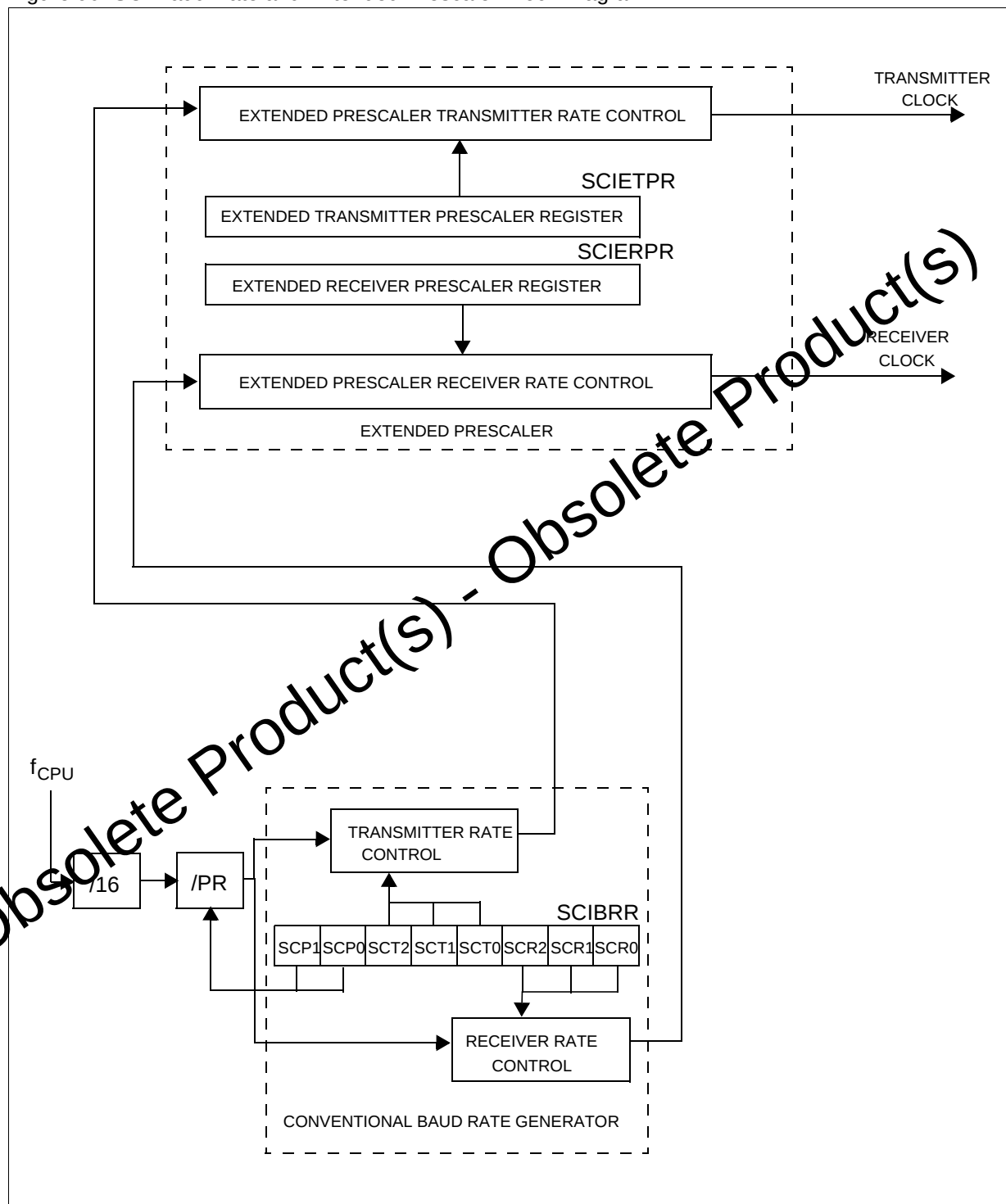
The Data register performs a double function (read and write) since it is composed of two registers, one for transmission (TDR) and one for reception (RDR).

The TDR register provides the parallel interface between the internal bus and the output shift register (see Figure 1).

The RDR register provides the parallel interface between the input shift register and the internal bus (see Figure 1).

LINSPI ¥ SERIAL COMMUNICATION INTERFACE (LIN Master Only) (Cont'd)

Figure 90. SCI Baud Rate and Extended Prescaler Block Diagram



beCAN CONTROLLER (Cont'd)

10.9.8.2 Mailbox Registers

This chapter describes the registers of the transmit and receive mailboxes. Refer to Section 0.1.4.4 Message Storage for detailed register mapping.

Transmit and receive mailboxes have the same registers except:

- MCSR register in a transmit mailbox is replaced by MFMI register in a receive mailbox.
- A receive mailbox is always write protected.
- A transmit mailbox is write enable only while empty, corresponding TME bit in the CTPR register set.

MAILBOX CONTROL STATUS REGISTER (MCSR)

Read / Write

Reset Value: 0000 0000 (00h)

7							0
0	0	TERR	ALST	TXOK	RQCP	ABRQ	TXRQ

Bits 7:6 = Reserved. Forced to 0 by hardware.

Bit 5 = TERR Transmission Error

- Read

This bit is updated by hardware after each transmission attempt.

0: The previous transmission was successful

1: The previous transmission failed due to an error

Bit 4 = ALST Arbitration Lost

- Read

This bit is updated by hardware after each transmission attempt.

0: The previous transmission was successful

1: The previous transmission failed due to an arbitration lost

Bit 3 = TXOK Transmission OK

- Read

The hardware updates this bit after each transmission attempt.

0: The previous transmission failed

1: The previous transmission was successful

Note: This bit has the same value as the corresponding TXOKx bit in the CTSR register.

Bit 2 = RQCP Request Completed

- Read/Clear

Set by hardware when the last request (transmit or abort) has been performed.

Cleared by software writing a "1" or by hardware on transmission request.

Note: This bit has the same value as the corresponding RQCPx bit of the CTSR register.

Clearing this bit clears all the status bits (TXOK, ALST and TERR) in the MCSR register and the RQCP and TXOK bits in the CTSR register.

Bit 1 = ABRQ Abort Request for Mailbox

- Read/Set

Set by software to abort the transmission request for the corresponding mailbox.

Cleared by hardware when the mailbox becomes empty.

Setting this bit has no effect when the mailbox is not pending for transmission.

Bit 0 = TXRQ Transmit Mailbox Request

- Read/Set

Set by software to request the transmission for the corresponding mailbox.

Cleared by hardware when the mailbox becomes empty.

Note: This register is implemented only in transmit mailboxes. In receive mailboxes, the MFMI register is mapped at this location.

12.2 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

12.2.1 Voltage Characteristics

Symbol	Ratings	Maximum value	Unit	
V _{DD} - V _{SS}	Supply voltage	6.5	V	
V _{PP} - V _{SS}	Programming Voltage	13		
V _{IN}	Input voltage on any pin ¹⁾²⁾	V _{SS} - 0.3 to V _{DD} + 0.3		
'V _{DDx} and 'V _{SSx}	Variations between different digital power pins	50	mV	
V _{SSA} - V _{SSx}	Variations between digital and analog ground pins	50		
V _{ESD(HBM)}	Electro-static discharge voltage (Human Body Model)	see Section 13.2.3 on page 233		
V _{ESD(MM)}	Electro-static discharge voltage (Machine Model)			

12.2.2 Current Characteristics

Symbol	Ratings	Maximum value	Unit
I _{VDD}	Total current into V _{DD} power lines (source) ³⁾	150	mA
I _{VSS}	Total current out of V _{SS} ground lines (sink) ³⁾		
I _{IO}	Output current sunk by any standard I/O and control pin	25	
	Output current sunk by any high sink I/O pin	50	
	Output current source by any I/Os and control pin	- 25	
I _{INJ(PIN)} ²⁾⁴⁾	Injected current on V _{DD} pin	± 5	
	Injected current on RESET pin		
	Injected current on OSC1 and OSC2 pins		
	Injected current on PB3 (on Flash devices)	+5	
	Injected current on any other pin ⁵⁾	± 5	
θ _{INJ(PIN)} ²⁾	Total injected current (sum of all I/O and control pins) ⁵⁾	± 25	

12.2.3 Thermal Characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature (see Section 13.2 "THERMAL CHARACTERISTICS")		

Notes:

1. Directly connecting the $\overline{RESET}$ and I/O pins to V_{DD} or V_{SS} could damage the device if an unintentional internal reset is generated or an unexpected change of the I/O configuration occurs (for example, due to a corrupted program counter). To guarantee safe operation, this connection has to be done through a pull-up or pull-down resistor (typical: 4.7k : for RESET, 10k : for I/Os). Unused I/O pins must be tied in the same way to V_{DD} or V_{SS} according to their reset configuration.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected.
3. All power (V_{DD}) and ground (V_{SS}) lines must always be connected to the external supply.
4. Negative injection disturbs the analog performance of the device. See note in "10-BIT ADC CHARACTERISTICS" on page 245.
5. When several inputs are submitted to a current injection, the maximum $\theta_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\theta_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

12.3.2 Operating Conditions with Low Voltage Detector (LVD)

Subject to general operating conditions for T_A .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IT+(LVD)}$	Reset release threshold (V_{DD} rise)		4.0 ¹⁾	4.2	4.5	V
$V_{IT-(LVD)}$	Reset generation threshold (V_{DD} fall)		3.8	4.0	4.25 ¹⁾	
$V_{hys(LVD)}$	LVD voltage threshold hysteresis ¹⁾	$V_{IT+(LVD)} - V_{IT-(LVD)}$	150	200	250	mV
V_{tPOR}	V_{DD} rise time rate ¹⁾		6			µs/V
					100	ms/V
$t_g(V_{DD})$	V_{DD} glitches filtered (not detected) by LVD ¹⁾	Measured at $V_{IT-(LVD)}$			40	ns

Notes:

1. Data based on characterization results, not tested in production.

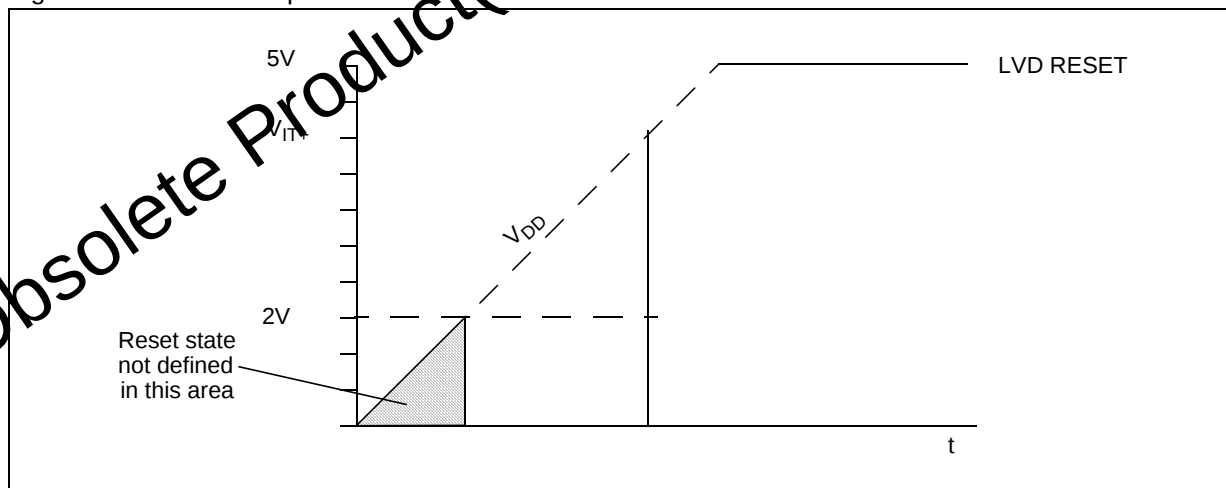
12.3.3 Auxiliary Voltage Detector (AVD) Thresholds

Subject to general operating conditions for T_A .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IT+(AVD)}$	1 Y0 AVDF flag toggle threshold (V_{DD} rise)		4.4 ¹⁾	4.6	4.9	V
$V_{IT-(AVD)}$	0 Y1 AVDF flag toggle threshold (V_{DD} fall)		4.2	4.4	4.65 ¹⁾	
$V_{hys(AVD)}$	AVD voltage threshold hysteresis	$V_{IT+(AVD)} - V_{IT-(AVD)}$		250		mV
V_{IT-}	Voltage drop between AVD flag set and LVD reset activated	$V_{IT-(AVD)} - V_{IT-(LVD)}$		450		

1. Data based on characterization results, not tested in production.

Figure 120. LVD Startup Behavior



Note: When the LVD is enabled, the MCU reaches its authorized operating voltage from a reset state. However, in some devices, the reset signal may be undefined until V_{DD} is approximately 2V. As a consequence, the I/Os may toggle when V_{DD} is below this voltage.

Because Flash write access is impossible below this voltage, the Flash memory contents will not be corrupted.

12.9 I/O PORT PIN CHARACTERISTICS

12.9.1 General Characteristics

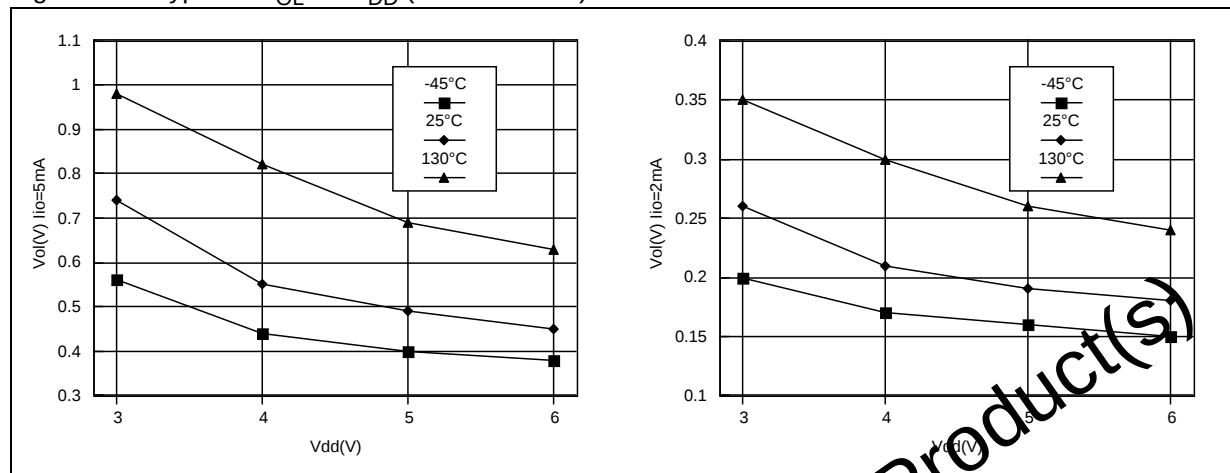
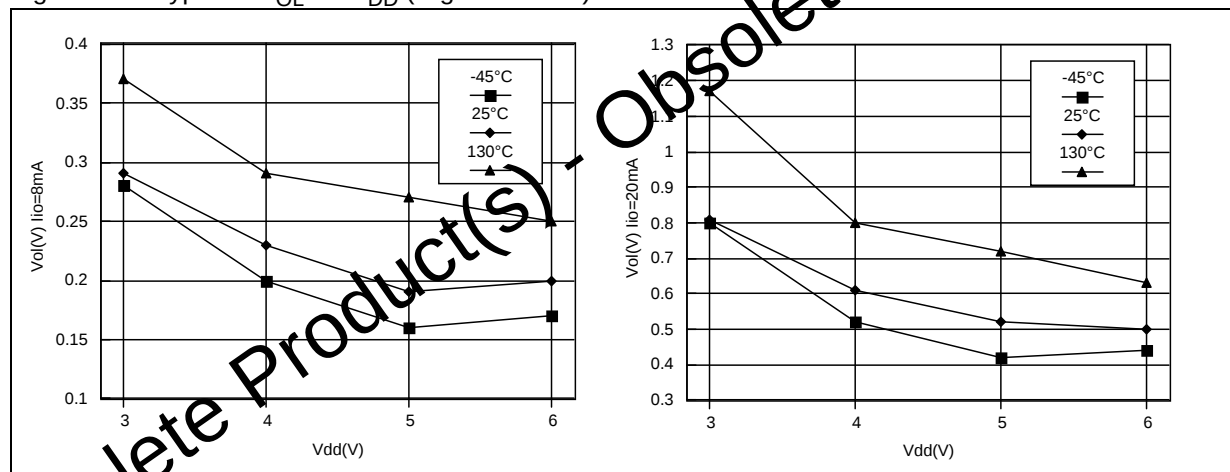
Subject to general operating conditions for V_{DD} , f_{OSC} , and T_A unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage ¹⁾	CMOS ports			$0.3 \times V_{DD}$	V
V_{IH}	Input high level voltage ¹⁾		$0.7 \times V_{DD}$			
V_{hys}	Schmitt trigger voltage hysteresis ²⁾			1		
V_{IL}	Input low level voltage ¹⁾	TTL ports			0.8	mV
V_{IH}	Input high level voltage ¹⁾		2			
V_{hys}	Schmitt trigger voltage hysteresis ²⁾			400		
$I_{INJ(PIN)}$	Injected Current on PB3	$V_{DD} = 5V$	Flash devices	0	+4	mA
	Injected Current on any other I/O pin		ROM devices		±4	
$a_{IINJ(PIN)}$ ³⁾	Total injected current (sum of all I/O and control pins) ⁷⁾				±4	
I_{lkg}	Input leakage current on robust pins	See "10-BIT ADC CHARACTERISTICS" on page 245				fA
	Input leakage current ⁴⁾	V_{SS} dV_{IN} dV_{DD}			±1	
I_S	Static current consumption ⁵⁾	Floating input mode		200		
R_{PU}	Weak pull-up equivalent resistor ⁶⁾	V_{IN} V_{SS} $V_{DD} = 5V$	50	90	250	k :
C_{IO}	I/O pin capacitance			5		pF
$t_{f(IO)out}$	Output high to low level fall time	$C_L = 50nF$		25		ns
$t_{r(IO)out}$	Output low to high level rise time	Between 10% and 90%				
$t_{w(IT)in}$	External interrupt pulse time ⁷⁾		1			t_{CPU}

Notes:

1. Data based on characterization results, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
3. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. Refer to Section 12.2 on page 220 for more details.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Configuration not recommended, all unused pins must be kept at a fixed voltage: Using the output mode of the I/O, for example, with an external pull-up or pull-down resistor (see Figure 125). Data based on design simulation and/or technology characteristics, not tested in production.
6. The R_{PU} pull-up equivalent resistor is based on a resistive transistor (corresponding I_{PU} current characteristics described in Figure 126).
7. To generate an external interrupt, a minimum pulse width must be applied on an I/O port pin configured as an external interrupt source.

I/O PORT PIN CHARACTERISTICS (Cont'd)

Figure 131. Typical V_{OL} vs V_{DD} (Standard I/Os)Figure 132. Typical V_{OL} vs V_{DD} (High-sink I/Os)

12.10 CONTROL PIN CHARACTERISTICS

12.10.1 Asynchronous $\overline{\text{RESET}}$ Pin

Subject to general operating conditions for V_{DD} , f_{OSC} , and T_A unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage ¹⁾				$0.3 \times V_{DD}$	V
V_{IH}	Input high level voltage ¹⁾		$0.7 \times V_{DD}$			
V_{hys}	Schmitt trigger voltage hysteresis ²⁾	$V_{DD} = 5V$		1.5		
V_{OL}	Output low level voltage ³⁾	$V_{DD} = 5V$	$I_{IO} = +5mA$	0.68	0.95	
			$I_{IO} = +2mA$	0.28	0.45	
R_{ON}	Weak pull-up equivalent resistor ⁴⁾	$V_{IN} \quad V_{SS}$	20	40	80	k Ω
$t_{w(RSTL)out}$	Generated reset pulse duration	Internal reset source		30		μs
$t_{h(RSTL)in}$	External reset pulse hold time ⁵⁾		2.5			μs
$t_{g(RSTL)in}$	Filtered glitch duration ⁶⁾			200		ns

Notes:

1. Data based on characterization results, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels.
3. The I_{IO} current sunk must always respect the absolute maximum rating specified in Section 12.2.2 and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
4. To guarantee the reset of the device, a minimum pulse has to be applied to the $\overline{\text{RESET}}$ pin. All short pulses applied on the $\overline{\text{RESET}}$ pin with a duration below $t_{h(RSTL)in}$ can be ignored.
5. The reset network (the resistor and two capacitors) protects the device against parasitic resets, especially in noisy environments.
6. Data guaranteed by design, not tested in production.

IMPORTANT NOTES (Cont'd)

Occurrence

The occurrence of the problem is random and proportional to the baud rate. With a transmit frequency of 19200 baud ($f_{CPU} = 8 \text{ MHz}$ and $SCIBRR = 0xC9$), the wrong break duration occurrence is around 1%.

Analysis

The LIN protocol specifies a minimum of 13 bits for the break duration, but there is no maximum value. Nevertheless, the maximum length of the header is specified as $(14+10+10+1) \times 1.4 = 49$ bits. This is composed of:

- the synch break field (14 bits)
- the synch field (10 bits)
- the identifier field (10 bits)

Every LIN frame starts with a break character. Adding an idle character increases the length of each header by 10 bits. When the problem occurs, the header length is increased by 11 bits and becomes $((14+11)+10+10+1) = 45$ bits.

To conclude, the problem is not always critical for LIN communication if the software keeps the time between the sync field and the ID smaller than 4 bits, that is, 208µs at 19200 baud.

The workaround is the same as for SCI mode but considering the low probability of occurrence (1%), it may be better to keep the break generation sequence as it is.

16.2.2 16-bit and 8-bit Timer PWM Mode

In PWM mode, the first PWM pulse is missed after writing the value FFFCh in the OC1R or OC2R register.

16.3 ROM DEVICES ONLY

16.3.1 16-bit Timer PWM Mode (Buffering Feature Change)

In all devices, the frequency and period of the PWM signal are controlled by comparing the counter with a 16-bit buffer updated by the OCiHR and OCiLR registers. In ROM devices, contrary to the description in Section 10.5.3.5 on page 103, the output compare function is not inhibited after a write instruction to the OCiHR register. Instead the buffer update at the end of the PWM period is inhibited until OCiLR is written. This improved buffering is fully compatible with applications written for Flash devices.