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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-R5F
Core Size	32-Bit Single-Core
Speed	96MHz
Connectivity	CANbus, CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	116
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	88K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.25V
Data Converters	A/D 56x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6j311ahaase2000a

Pin No. S6J311xHAC	Pin Name	Polarity	I/O Circuit Type	Function
18	P020 SOT0_0 SDA0_0 TIOB1_0 TEXT1_0	- - - - -	P	General-purpose I/O port Multi-function serial ch.0 serial data output pin (0) I2C bus ch.0 serial data I/O pin Base timer ch.1 TIOB input pin (0) Free-run timer 1 clock input pin (0)
19	P021 SCK0_0 SCL0_0 TIOB2_0	- - - -	P	General-purpose I/O port Multi-function serial ch.0 clock I/O pin (0) I2C bus ch.0 serial clock I/O pin Base timer ch.2 TIOB input pin (0)
20	P022 SIN0_0 TIOB3_0 INT3_0	- - - -	P	General-purpose I/O port Multi-function serial ch.0 serial data input pin (0) Base timer ch.3 TIOB input pin (0) INT3 external interrupt input pin (0)
21	P023 SCS0_0 TIOB4_0	- - -	P	General-purpose I/O port Multi-function serial ch.0 serial chip select I/O pin (0) Base timer ch.4 TIOB input pin (0)
22	P024 TIOB5_0	- -	P	General-purpose I/O port Base timer ch.5 TIOB input pin (0)
23	P027 TIOA4_1 TIOB6_0 INT1_1 TEXT0_1	- - - - -	P	General-purpose I/O port Base timer ch.4 TIOA output pin (1) Base timer ch.6 TIOB input pin (0) INT1 external interrupt input pin (1) Free-run timer 0 clock input pin (1)
24	P028 SIN1_0 TIOB7_0 INT4_0 OUT0_1	- - - - -	P	General-purpose I/O port Multi-function serial ch.1 serial data input pin (0) Base timer ch.7 TIOB input pin (0) INT4 external interrupt input pin (0) Output compare ch.0 output pin (1)
25	P029 SOT1_0 SDA1_0 AN0 OUT1_1	- - - - -	A	General-purpose I/O port Multi-function serial ch.1 serial data output pin (0) I2C bus ch.1 serial data I/O pin ADC analog 0 input pin Output compare ch.1 output pin (1)
26	P030 OUT2_1	- -	P	General-purpose I/O port Output compare ch.2 output pin (1)
27	P031 SCS1_0 AN1 OUT3_1	- - - -	A	General-purpose I/O port Multi-function serial ch.1 serial chip select I/O pin (0) ADC analog 1 input pin Output compare ch.3 output pin (1)
28	P100 SCK1_0 SCL1_0 AN2 OUT4_1	- - - - -	A	General-purpose I/O port Multi-function serial ch.1 clock I/O pin (0) I2C bus ch.1 serial clock I/O pin ADC analog 2 input pin Output compare ch.4 output pin (1)
29	P101 AN3 OUT5_1	- - -	A	General-purpose I/O port ADC analog 3 input pin Output compare ch.5 output pin (1)
30	P103 AN5 OUT6_1	- - -	A	General-purpose I/O port ADC analog 5 input pin Output compare ch.6 output pin (1)
31	P105 TIOA9_0 OUT7_1	- - -	P	General-purpose I/O port Base timer ch.9 TIOA I/O pin (0) Output compare ch.7 output pin (1)
32	P106 OUT8_1	- -	P	General-purpose I/O port Output compare ch.8 output pin (1)
33	P107 TIOA10_0 INT2_1 OUT9_1	- - - -	P	General-purpose I/O port Base timer ch.10 TIOA output pin (0) INT2 external interrupt input pin (1) Output compare ch.9 output pin (1)

Pin No. S6J311xHAC	Pin Name	Polarity	I/O Circuit Type	Function
117	MD	-	C	Mode pin
118	X0	-	G	Main clock oscillation input pin
119	X1	-	G	Main clock oscillation output pin
121	P331	-	P	General-purpose I/O port
122	P400	-	P	General-purpose I/O port
123	RSTX	N	F	External reset input pin
127	P401 IN0_0	- -	Q	General-purpose I/O port Input capture ch.0 input pin (0)
128	P402 IN1_0 INT2_0	- - -	Q	General-purpose I/O port Input capture ch.1 input pin (0) INT2 external interrupt input pin (0)
129	P403 IN2_0 TRACEDATA0	- - -	Q	General-purpose I/O port Input capture ch.2 input pin (0) Trace data 0 output pin
130	P404 IN3_0 TRACEDATA1	- - -	Q	General-purpose I/O port Input capture ch.3 input pin (0) Trace data 1 output pin
131	P405 IN4_0 INT11_0 TRACEDATA2	- - - -	Q	General-purpose I/O port Input capture ch.4 input pin (0) INT11 external interrupt input pin (0) Trace data 2 output pin
132	P406 TRACEDATA3	- -	Q	General-purpose I/O port Trace data 3 output pin
133	P407 TRACEDATA4	- -	Q	General-purpose I/O port Trace data 4 output pin
134	P408 SIN2_0 INT12_0 TRACEDATA5	- - - -	Q	General-purpose I/O port Multi-function serial ch.2 serial data input pin (0) INT12 external interrupt input pin (0) Trace data 5 output pin
135	P409 SOT2_0 SDA2_0 TIOA24_1 TRACEDATA6	- - - - -	Q	General-purpose I/O port Multi-function serial ch.2 serial data output pin (0) I2C bus ch.2 serial data I/O pin Base timer ch.24 TIOA output pin (1) Trace data 6 output pin
136	P411 SCK2_0 SCL2_0 INT13_1 TRACEDATA7	- - - - -	Q	General-purpose I/O port Multi-function serial ch.2 clock I/O pin (0) I2C bus ch.2 serial clock I/O pin INT13 external interrupt input pin (1) Trace data 7 output pin
137	P413 SCS20_0 INT14_1	- - -	Q	General-purpose I/O port Multi-function serial ch.2 serial chip select 0 I/O pin (0) INT14 external interrupt input pin (1)
138	P414 SCS21_0	- -	Q	General-purpose I/O port Multi-function serial ch.2 serial chip select 1 output pin (0)
139	P416 IN5_0 TIOA22_1	- - -	Q	General-purpose I/O port Input capture ch.5 input pin (0) Base timer ch.22 TIOA output pin (1)
140	P417 TIOA23_1 INT15_1	- - -	Q	General-purpose I/O port Base timer ch.23 TIOA I/O pin (1) INT15 external interrupt input pin (1)
141	P418 SCS22_0 INT14_0	- - -	Q	General-purpose I/O port Multi-function serial ch.2 serial chip select 2 output pin (0) INT14 external interrupt input pin (0)

6. Handling Devices

For Latch-up Prevention

The latch-up phenomenon may occur on a CMOS IC in the following cases: the voltage applied to an input or output pin is higher than V_{CC} or lower than V_{SS}; or the voltage applied between a VCC pin and a VSS pin exceeds the rating. A latch-up causes a rapid increase in the power supply current, possibly resulting in thermal damage to an element. When using the device, take sufficient care not to exceed the maximum rating.

Also be careful that analog power supplies (AVCC0, AVCC1, AVRH0, and AVRH1) and analog inputs do not exceed the digital power supply (VCC) at the analog system power-on and power-off times.
The power-on sequence is as follows. Simultaneously turn on the digital supply voltage (VCC) and analog supply voltages (AVCC0, AVCC1, AVRH0, and AVRH1), or turn on the digital supply voltage (VCC) and then the analog supply voltages (AVCC0, AVCC1, AVRH0, and AVRH1).

About Handling Unused Pins

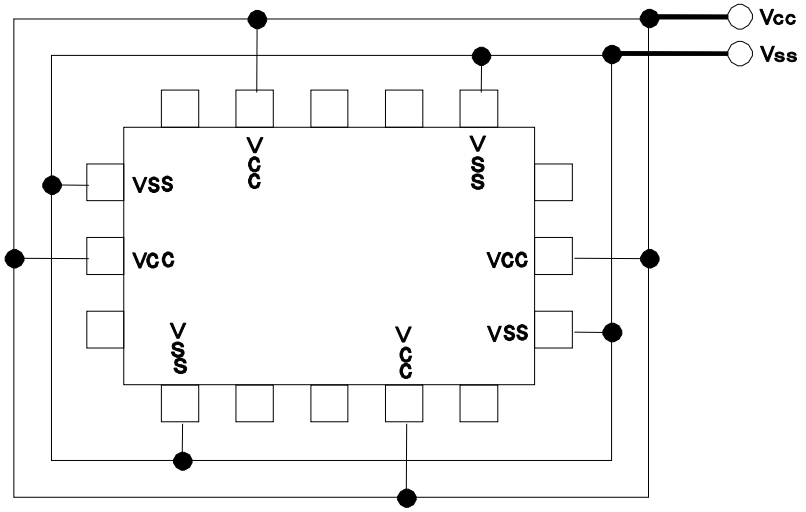
Leaving unused input pins open may cause permanent damage from a malfunction or latch-up. Take measures for unused pins, such as pulling up or pulling down the voltage with resistors of 2 kiloohms or higher.

If there are any unused input/output pins, set them to the output state and then open them, or set them to the input state and handle them in the same way as input pins.

About Power Supply Pins

If the device has multiple VCC and VSS pins, the device is designed in such a way that the pins that should be at the same potential are connected to each other inside the device to prevent malfunctions such as latch-up. However, to reduce unwanted emissions, prevent malfunctions of strobe signals caused by an increase of the ground level, and observe standards on total output current, be sure to connect all the VCC and VSS pins to the power source and ground externally. Also handle all the VSS power supply pins in this way as shown in the following diagram. If there are multiple VCC or VSS systems, the device does not operate normally even within the guaranteed operating range.

Figure 6-1. Pin Assignment



In addition, consider connecting with low impedance from the power supply source to the VCC and VSS of this device.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between the VCC pin and the VSS pin.

About the Crystal Oscillation Circuit

Noise entering the X0 or X1 pin may cause a malfunction. Design the printed circuit board in such a way that the X0 and X1 pins, the crystal oscillator (or ceramic resonator), and a bypass capacitor to ground are located very close to the device.

We recommend that the printed circuit board artwork have the X0 and X1 pins enclosed by ground.

9. Pin Status in CPU Status

Table 9-1. Pin State Table (1/2)

Pin No.	Pin Name	GPORTEN Control	External Reset Factor 1			External Reset Factor 2				External Reset Factor 3		Internal Reset Factor *2	Sleep mode	Stop mode *4		Timer mode *4	
			External factor generation in progress	After external factor releasing		While Generating External Factor		After Releasing External Factor									
			Internal reset issuance in progress	Internal reset issuance in progress	After internal reset issuance (Before GPORT setting)	Before internal reset issuance	Internal reset issuance in progress	Internal reset issuance in progress	After internal reset issuance (Before GPORT setting)	Internal reset issuance in progress	After internal reset issuance (Before GPORT setting)		CPU Sleep	High impedance disabled (SYSCO_SPECFGR: PSSPADCTRL=0)	High impedance enabled (SYSCO_SPECFGR: PSSPADCTRL=1)	High impedance disabled (SYSCO_SPECFGR: PSSPADCTRL=0)	High impedance enabled (SYSCO_SPECFGR: PSSPADCTRL=1)
2	P000/SOT2_1	With control	Hi-Z/Input blocked			Hi-Z/ Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Status immediately before the shutdown retaine	Last state retained	Last state retained (*3)	Hi-Z/Input blocked	Last state retained (*3)	Hi-Z/Input blocked
3	P001/SCS20_1																
4	P003/SCS22_1																
5	P005/IN6_0/SIN3_0														Hi-Z/Input blocked		Hi-Z/Input blocked
6	P006/SOT3_0/SDA3_0/IN7_0																
7	P007/SCK3_0/SCL3_0/IN8_0																
8	P008/IN9_0/SCS30_0/TIOA0_0																
9	P009/IN10_0/TIOA1_0/INT0_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
10	P010/IN11_0/TIOA2_0														Hi-Z/Input blocked		Hi-Z/Input blocked
11	P012/OUT5_0/TIOA3_0																
12	P013/OUT6_0/TIOA4_0																
13	P015/OUT7_0/TIOA5_0																
14	P016/OUT8_0/TIOA6_0																
15	P017/OUT9_0/TIOA7_0																
16	P018/OUT10_0/TIOA8_0																
17	P019/OUT11_0/TIOB0_0/TEXT0_0																
18	P020/SOT0_0/SDA0_0/TEXT1_0/TIOB1_0																
19	P021/SCK0_0/SCL0_0/TIOB2_0																
20	P022/SIN0_0/TIOB3_0/INT3_0														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
21	P023/SCS0_0/TIOB4_0														Hi-Z/Input blocked		Hi-Z/Input blocked
22	P024/TIOB5_0																
23	P027/TIOA4_1/TIOB6_0/INT1_1/TEXT0_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
24	P028/OUT0_1/SIN1_0/TIOB7_0/INT4_0																
25	P029/AN0/SOT1_0/SDA1_0/OUT1_1														Hi-Z/Input blocked		Hi-Z/Input blocked
26	P030/OUT2_1																
27	P031/OUT3_1/SCS1_0/AN1																
28	P100/AN2/SCK1_0/SCL1_0/OUT4_1																
29	P101/OUT5_1/AN3																
30	P103/OUT6_1/AN5																
31	P105/OUT7_1/TIOA9_0																
32	P106/OUT8_1																
33	P107/OUT9_1/TIOA10_0/INT2_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
34	P108/OUT10_1/AN6/TIOA11_0/INT3_1																
35	P109/OUT11_1/TIOA12_0														Hi-Z/Input blocked		Hi-Z/Input blocked
39	P112/AN9/TIOA13_0																
40	P113/TIOA5_1																
41	P114/AN10/TIOA6_1																
45	P115																
46	P117/AN12/INT4_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
47	P118/AN13/INT5_1																
48	P119/AN14														Hi-Z/Input blocked		Hi-Z/Input blocked
49	P120/AN15																
50	P122/AN17/TIOA11_1																
51	P123/AN18/TIOA12_1																
52	P126/AN19																
53	P127/AN20/TEXT1_1																
54	P128/AN21/TEXT2_1																
55	P129/IN6_1/AN22																
56	P130/IN7_1/AN23/INT5_0														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
57	P131/IN8_1/AN24														Hi-Z/Input blocked		Hi-Z/Input blocked
58	P202/IN9_1/INT6_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
59	P203/IN10_1																
60	P204/IN11_1/AN27														Hi-Z/Input blocked		Hi-Z/Input blocked
61	P205/AN28/TEXT3_1																
62	P206/AN29/TEXT4_1																
63	P207/AN30/IN7_1/TEXT5_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
64	P208/AN31/TIOA19_0														Hi-Z/Input blocked		Hi-Z/Input blocked
65	P209/AN32/TIOA20_0																
66	P210/IN0_2/AN33/TIOA21_0/INT6_0														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
67	P211/IN1_2/AN34/TIOA22_0														Hi-Z/Input blocked		Hi-Z/Input blocked
68	P212/IN2_2/AN35/TIOA13_1																
69	P213/IN3_2/TIOA14_1/INT8_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
70	P214/IN4_2/TIOA15_1														Hi-Z/Input blocked		Hi-Z/Input blocked
71	P215/IN5_2/TIOA16_1/INT9_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)

Table 9-2. Pin State Table (2/2)

Pin No.	Pin Name	GPORTEN Control	External Reset Factor 1			External Reset Factor 2				External Reset Factor 3		Internal Reset Factor *2	Sleep mode	Stop mode *4		Timer mode *4	
			External factor generation in progress	After external factor releasing		While Generating External Factor		After Releasing External Factor									
			Internal reset issuance in progress	Internal reset issuance in progress	After internal reset issuance (Before GPORT setting)	Before internal reset issuance	Internal reset issuance in progress	Internal reset issuance in progress	After internal reset issuance (Before GPORT setting)	Internal reset issuance in progress	After internal reset issuance (Before GPORT setting)		CPU Sleep	High impedance disabled (SYSCI0_SPECFGR. PSSPADCTRL=0)	High impedance enabled (SYSCI0_SPECFGR. PSSPADCTRL=1)	High impedance disabled (SYSCI0_SPECFGR. PSSPADCTRL=0)	High impedance enabled (SYSCI0_SPECFGR. PSSPADCTRL=1)
74	P218/AN36/TEXT2_0	With control	Hi-Z/Input blocked			Hi-Z/ Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Status immediately before the shutdown retaine	Last state retained	Last state retained (*3)	Hi-Z/Input blocked	Last state retained (*3)	Hi-Z/Input blocked
75	P219/AN37/TEXT3_0																
76	P220/IN6_2/AN38																
77	P222/IN7_2/AN39/INT7_0														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
78	P223/IN8_2/AN40/PWU_AN0														Hi-Z/Input blocked		Hi-Z/Input blocked
79	P224/IN9_2/TX0_2/AN41/PWU_AN1																
80	P225/IN10_2/RX0_2/AN42/INT0_0/PWU_AN2														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
81	P226/IN11_2/AN43/TIOA17_1/PWU_AN3																
85	P227/AN44/TIOA23_0/PWU_AN4																
86	P228/TX0_1/AN45/TIOA24_0/PWU_AN5																
87	P229/OUT0_0/RX0_1/AN46/TIOA25_0/INT8_0/PWU_AN6														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
88	P230/OUT1_0/AN47/TIOA26_0/PWU_AN7																
89	P231/OUT2_0/AN48/TIOA27_0																
90	P300/OUT3_0/AN49/TIOA28_0																
91	P301/OUT4_0/AN50/TIOA18_1																
92	P302/AN51/TIOA19_1																
93	P304/AN52/TIOA20_1/TEXT4_0																
94	P305/AN53/TIOA29_0/TEXT5_0																
95	NMIX	-	Input enabled			Input enabled		Input enabled		Input enabled		Input enabled	Input enabled	Input enabled		Input enabled	
96	P306/TX0_0/AN54	With control	Hi-Z/Input blocked			Hi-Z /Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Status immediately before the shutdown retaine	Last state retained	Last state retained (*3)	Hi-Z/Input blocked	Last state retained (*3)	Hi-Z/Input blocked
97	P307/RX0_0/AN55/INT1_0														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
98	P308/IN0_1/AN56/TIOA28_1																
99	P309/IN1_1/AN57/TIOA29_1																
100	P312/IN2_1/AN58														Hi-Z/Input blocked		Hi-Z/Input blocked
101	P313/IN3_1/AN59/INT10_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
102	P314/IN4_1/AN60/TIOA7_1																
103	P315/IN5_1/AN61/TIOA8_1														Hi-Z/Input blocked		Hi-Z/Input blocked
104	P317/AN62/TIOA9_1/INT11_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
107	P321/PWUTRG	-	Hi-Z/Input blocked			Hi-Z/Input blocked		Hi-Z/Input blocked		Hi-Z/Input blocked		Hi-Z/Input blocked *7 (Status immediately before the shutdown retaine) *6 (PWUTRG output/Input blocked *5)	Hi-Z/Input blocked *7 (Last state retained) *6 (PWUTRG output/Input blocked *5)	Hi-Z/Input blocked *7 (Last state retained) *6 (PWUTRG output/Input blocked *5)	Hi-Z/Input blocked	Hi-Z/Input blocked (Last state retained) *3 *6 (*5)	Hi-Z/Input blocked
110	TRST/P322		Input enabled			Input enabled		Input enabled		Input enabled		Input enabled (Status immediately before the shutdown retaine) *6	Input enabled (Last state retained) *6	Input enabled (Last state retained (*3)) *6	Input enabled (Hi-Z/Input blocked) (*6)	Input enabled (Last state retained (*3)) *6	Input enabled (Hi-Z/Input blocked) (*6)
111	TDO/P323		-			-		-		-							
112	TDI/P324		Input enabled			Input enabled		Input enabled		Input enabled							
113	TMS											Input enabled	Input enabled	Input enabled		Input enabled	
114	TCK																
115	P327	With control	Hi-Z/Input blocked			Hi-Z /Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Status immediately before the shutdown retaine	Last state retained	Last state retained (*3)	Hi-Z/Input blocked	Last state retained (*3)	Hi-Z/Input blocked
116	P330																
117	MD	-	Input enabled			Input enabled		Input enabled		Input enabled		Input enabled	Input enabled	Input enabled		Input enabled	
118	X0		-			-		-		-		-	-	-		-	
119	X1																
121	P331	With control	Hi-Z/Input blocked			Hi-Z /Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Status immediately before the shutdown retaine	Last state retained	Last state retained (*3)	Hi-Z/Input blocked	Last state retained (*3)	Hi-Z/Input blocked
122	P400																
123	RSTX	-	Input enabled			Input enabled		Input enabled		Input enabled		Input enabled	Input enabled	Input enabled		Input enabled	
127	P401/IN0_0	With control	Hi-Z/Input blocked			Hi-Z /Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Status immediately before the shutdown retaine	Last state retained	Last state retained (*3)	Hi-Z/Input blocked	Last state retained (*3)	Hi-Z/Input blocked
128	P402/IN1_0/INT2_0														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
129	P403/IN2_0/TRACEDATA0														Hi-Z/Input blocked		Hi-Z/Input blocked
130	P404/IN3_0/TRACEDATA1																
131	P405/IN4_0/INT11_0/TRACEDATA2														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
132	P406/TRACEDATA3														Hi-Z/Input blocked		Hi-Z/Input blocked
133	P407/TRACEDATA4																
134	P408/SIN2_0/INT12_0/TRACEDATA5														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
135	P409/SOT2_0/SDA2_0/TIOA24_1/TRACEDATA6														Hi-Z/Input blocked		Hi-Z/Input blocked
136	P411/INT13_1/SCK2_0/SCL2_0/TRACEDATA7														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
137	P413/SCS20_0/INT14_1																
138	P414/SCS21_0														Hi-Z/Input blocked		Hi-Z/Input blocked
139	P416/IN5_0/TIOA22_1																
140	P417/TIOA23_1/INT15_1														Hi-Z/Input blocked (*1)		Hi-Z/Input blocked (*1)
141	P418/SCS22_0/INT14_0																
142	P420/SCK2_1/TRACECLK														Hi-Z/Input blocked		Hi-Z/Input blocked
143	P421/SIN2_1/TRACECTL																

Notes:

- *The following condition should be satisfied in order to facilitate heat dissipation.*

1. *4 or more layers PCB should be used.*
2. *The area of PCB should be 114.3 mm x 76.2 mm or more, and the thickness should be 1.6 mm or more. (JEDEC standard)*
3. *1 layer of middle layers at least should be used for dedicated layer to radiate heat with residual copper rate 90% or more. The layer can be used for system ground.*
4. *35~50% of the die stage area which is exposed at back surface of package should be soldered to a part of 1st layer.*
5. *The part of 1st layer should be connected to the dedicated heat radiation layer with more than 10 thermal via holes.*

Figure10.2-1: Example thermal via holes on PCB.

Notes:

- *Figure 10.2-1 is a schematic diagram showing PCB in section.*
- *Figure 10.2-2 in the following pages are recommended land patterns for each package series. Thermal via holes should closely be placed and aligned with lands.*
- *If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.*

10.4 AC Characteristics

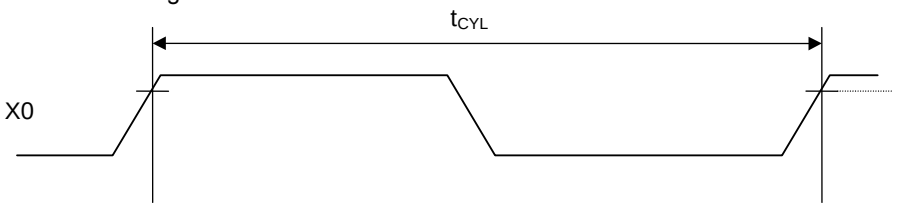
10.4.1 Source Clock Timing

(T_A: Recommended operating conditions, V_{CC}=5.0 V +5%/-10%, V_{SS}=AV_{SS}=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_C	X0, X1	-	-	4	-	MHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1	-	-	250	-	ns	
CAN PLL jitter (during lock)	t_{PJ}	-	-	-10	-	+10	ns	*
Built-in slow-CR oscillation frequency	F_{CRS}	-	-	50	100	150	kHz	
Built-in fast-CR oscillation frequency	F_{CRF}	-	-	2.4	4	6.0	MHz	
PLL input clock frequency	F_{PLLI}	-	-	-	4	-	MHz	
PLL macro oscillation clock frequency	F_{PLLO}	-	-	400	-	576	MHz	
SSCG-PLL input clock frequency	$F_{SSCGPLLI}$	-	-	-	4	-	MHz	
SSCG-PLL macro oscillation clock frequency	$F_{SSCGPLLO}$	-	-	400	-	576	MHz	

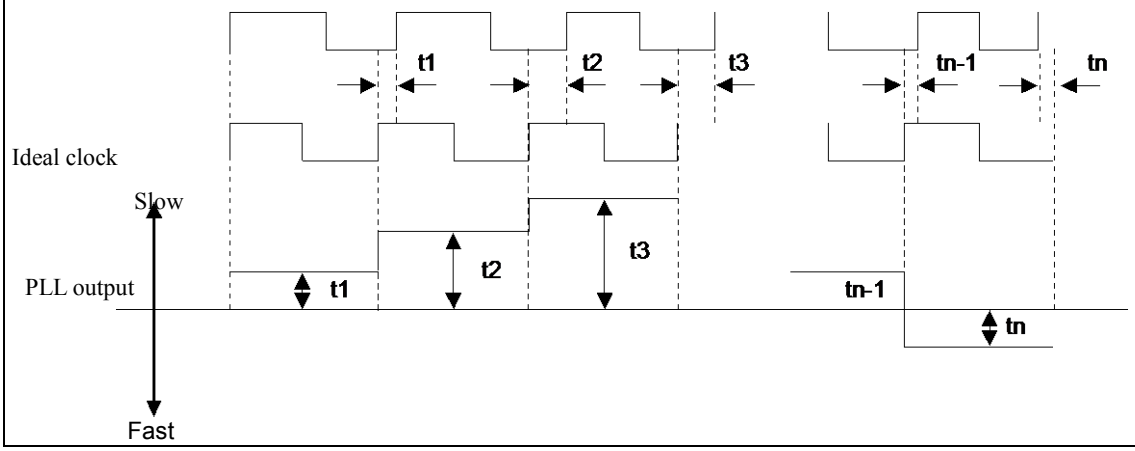
*: The maximum/minimum values have been standardized with the main clock and PLL clock in use.

• X0 and X1 clock timing



• CAN PLL jitter

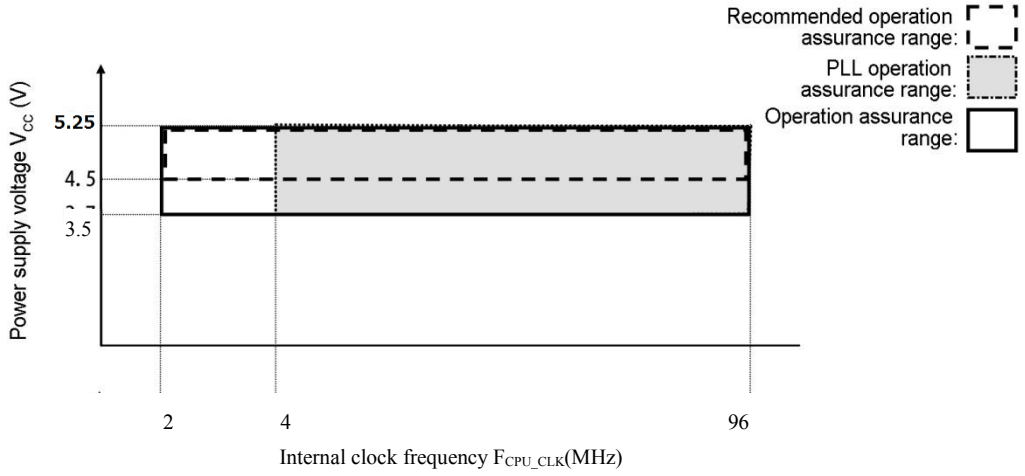
A time difference from the ideal clock is guaranteed for each cycle period within 20,000 cycles.



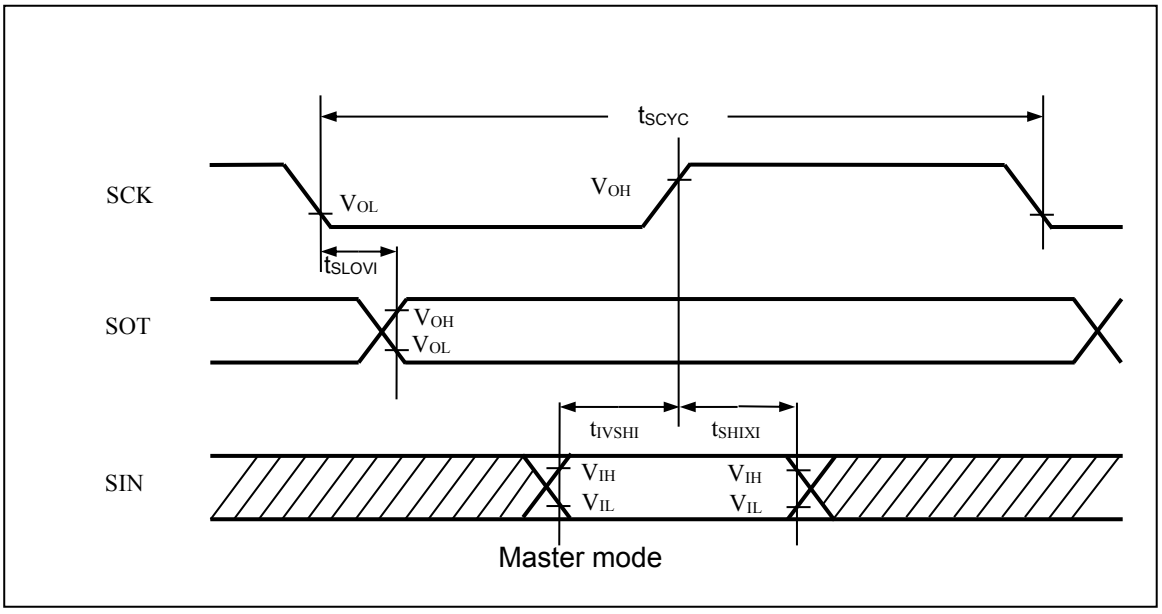
Parameter	Symbol	Pin Name	Conditions	S6J311xHAC* Value * x:A/9			Unit	Remarks
				Min	Typ	Max		
	t_{CLK_LCP0A}	-	-	41.6	-	-	ns	CLK_LCP0A
	t_{CLK_LCP1}	-	-	41.6	-	-	ns	CLK_LCP1
	t_{CLK_LCP1A}	-	-	41.6	-	-	ns	CLK_LCP1A
	t_{CLK_LAPP0}	-	-	41.6	-	-	ns	CLK_LAPP0
	t_{CLK_LAPP0A}	-	-	41.6	-	-	ns	CLK_LAPP0A
	t_{CLK_LAPP1}	-	-	41.6	-	-	ns	CLK_LAPP1
	t_{CLK_LAPP1A}	-	-	41.6	-	-	ns	CLK_LAPP1A
	t_{CLK_TRC}	-	-	20.8	-	-	ns	CLK_TRC
	t_{CLK_HSSPI}	-	-	41.6	-	-	ns	CLK_HSSPI
	t_{CLK_SYSC0H}	-	-	41.6	-	-	ns	CLK_SYSC0H
	t_{CLK_COMH}	-	-	41.6	-	-	ns	CLK_COMH
	t_{CLK_RAM0H}	-	-	41.6	-	-	ns	CLK_RAM0H
	t_{CLK_RAM1H}	-	-	41.6	-	-	ns	CLK_RAM1H
	t_{CLK_SYSC0P}	-	-	41.6	-	-	ns	CLK_SYSC0P
	t_{CLK_COMP}	-	-	41.6	-	-	ns	CLK_COMP
	t_{CANFD_CCLK}	-	-	25.0	-	-	ns	CANFD_CCLK

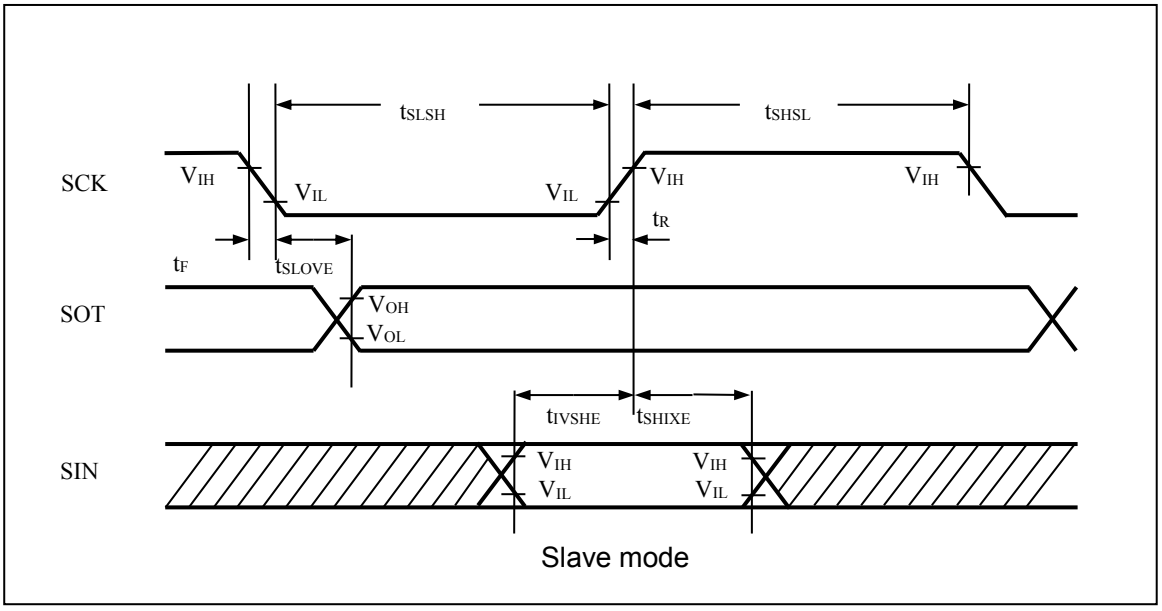
• Guaranteed operation range

Internal operation clock frequency vs. Power supply voltage



Note: A supply voltage that is equal to or less than the set voltage for low-voltage detection causes a reset.


tSCYC
SCK
VOL
VOH
tSLOVI
SOT
VOH
VOL
tIVSHI
tSHIXI
SIN
VIH
VIL
VIH
VIL
Master mode


tSLSH
tSHSL
SCK
VIH
VIL
VIL
VIH
VIH
tR
tF
tSLOVE
SOT
VOH
VOL
tIVSHE
tSHIXE
SIN
VIH
VIL
VIH
VIL
Slave mode

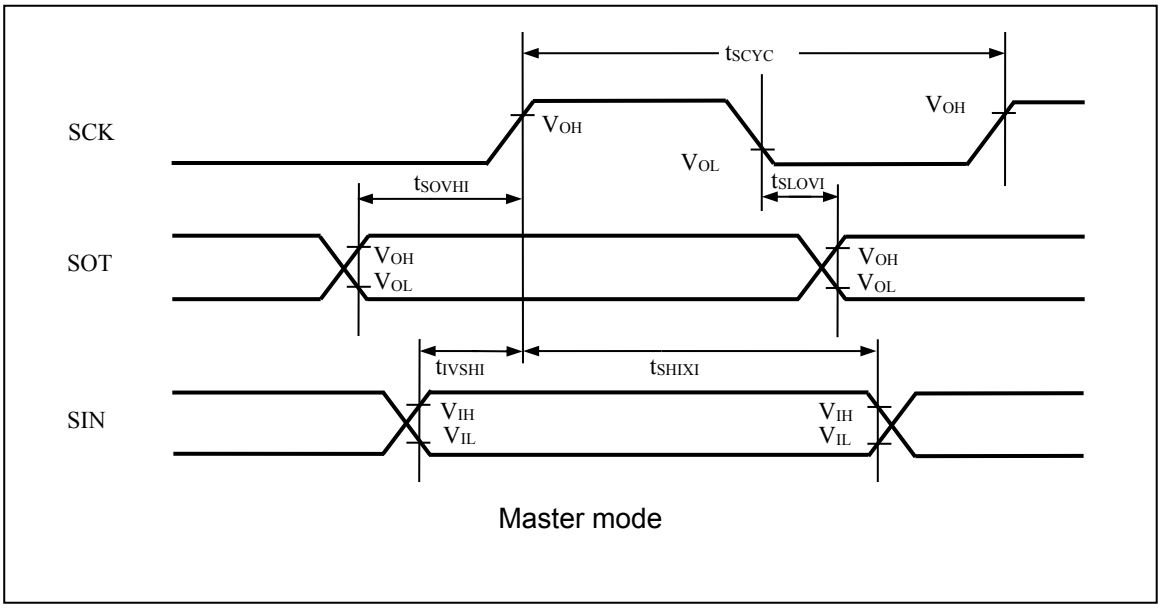
(5-1-4) SPI Supported (SCR:SPI=1), and Serial Clock Output Signal Detect Level "L" (SMR:SCINV=1)

(T_A: Recommended operating conditions, V_{CC}=5.0 V +5%/-10%, V_{SS}=AV_{SS}=0.0 V)

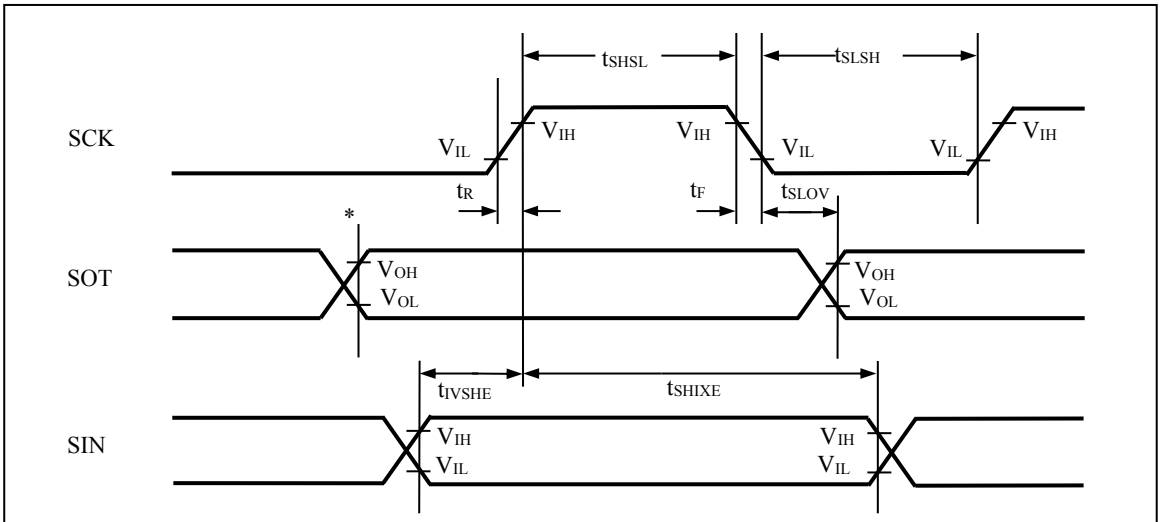
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Master mode (CL=50pF, I_{OL}=-2mA, I_{OH}=2mA), (CL=20pF, I_{OL}=-1mA, I_{OH}=1mA)	$4t_{CLK\_LCP0A}$	-	ns	
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		-30	+30	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		30	-	ns	
SCK ↑→ Valid SIN hold time	t_{SHIXI}			0	-	ns	
SOT → SCK ↑ delay time	t_{SOVHI}	SCK0 to SCK3, SOT0 to SOT3		$2t_{CLK\_LCP0A}$ -30	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK3	Slave mode (CL=50pF, I_{OL}=-2mA, I_{OH}=2mA), (CL=20pF, I_{OL}=-1mA, I_{OH}=1mA)	t_{CLK_LCP0A} +10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CLK\_LCP0A}$ -10	-	ns	
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK3, SOT0 to SOT3		-	45	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		10	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK3		-	5	ns	
SCK rise time	t_R	SCK0 to SCK3		-	5	ns	

Notes:

- This is the AC characteristic in CLK synchronized mode.
- CL is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.

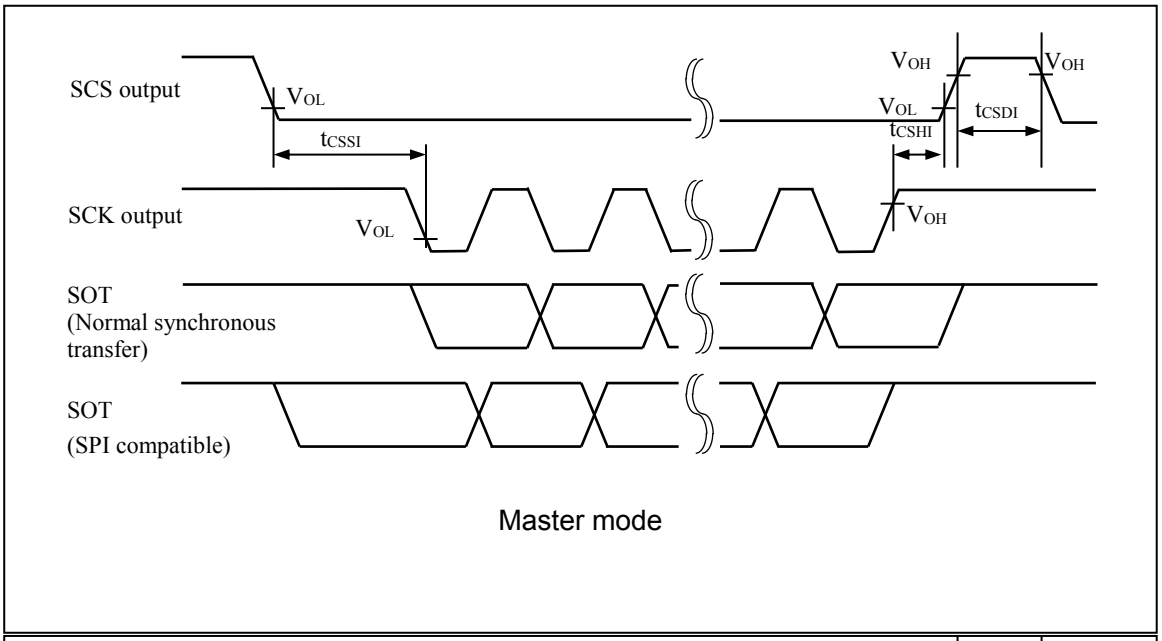


Master mode

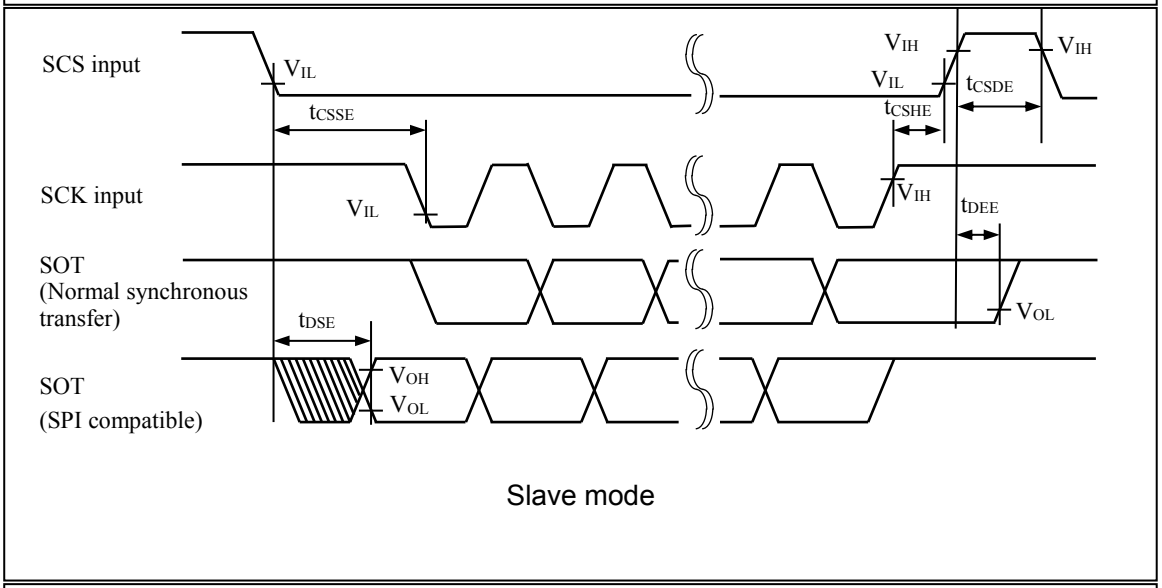


* Changes when writing to the TDR register

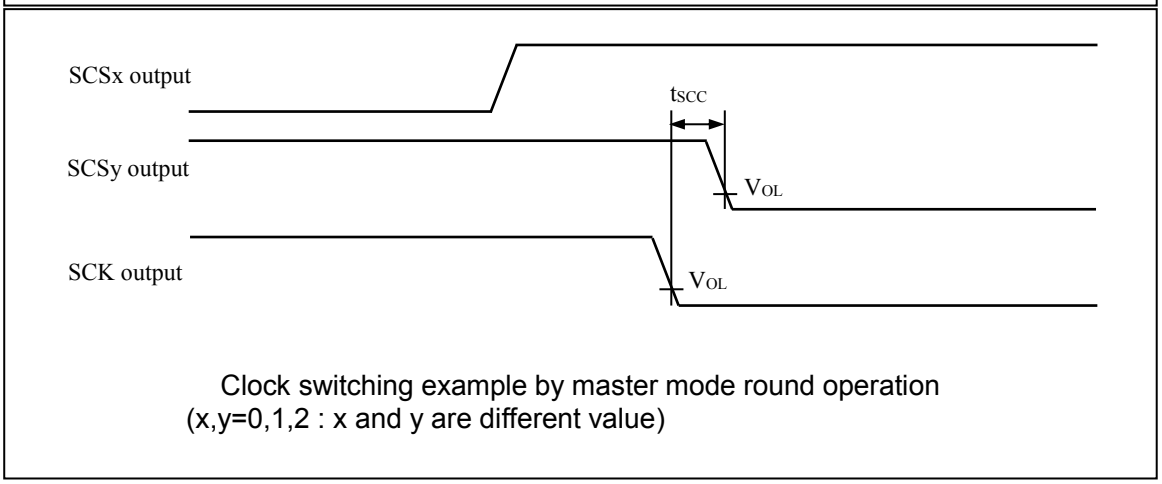
Slave mode



Master mode



Slave mode



Clock switching example by master mode round operation
(x,y=0,1,2 : x and y are different value)

(5-1-6) Serial Chip Select Used (SCSCR:CSEN=1)

■Serial clock output signal detect level "L" (SMR, SCSFR:SCINV=1)

■Serial chip select inactive level "H" (SCSCR, SCSFR:CSLVL=1)

(T_A: Recommended operating conditions, V_{CC}=5.0 V +5%/-10%, V_{SS}=AV_{SS}=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↓→ SCK ↑ setup time	t_{CSSI}	SCK0 to SCK3, SCS0x to SCS3x	Master mode (CL=50pF, I_{OL}=-2mA, I_{OH}=2mA), (CL=20pF, I_{OL}=-1mA, I_{OH}=1mA)	t_{CSSU}*1-50	-	ns	
SCK ↓→ SCS ↑ hold time	t_{CSHI}			t_{CSHD}*2+0	-	ns	
SCS deselect time	t_{CSDI}	SCS0x to SCS3x		t_{CSDS}*3-50+5 t_{CLK_LCP0A}	-	ns	
SCS ↓ → SCK ↑ setup time	t_{CSSE}	SCK0 to SCK3, SCS0x to SCS3x	Slave mode (CL=50pF, I_{OL}=-2mA, I_{OH}=2mA), (CL=20pF, I_{OL}=-1mA, I_{OH}=1mA)	$3t_{CLK\_LCP0A}$ +30	-	ns	
SCK ↓ → SCS ↑ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}	SCS0x to SCS3x		$3t_{CLK\_LCP0A}$ +30	-	ns	
SCS ↓ → SOT delay time	t_{DSE}	SCS0x to SCS3x, SOT0 to SOT3		-	50	ns	
SCS ↑ → SOT delay time	t_{DEE}			0	-	ns	
SCK ↑ → SCS ↓ clock switching time	t_{SCC}	SCK0 to SCK3, SCS0x to SCS3x	Master mode round operation (CL=50pF, I_{OL}=-2mA, I_{OH}=2mA), (CL=20pF, I_{OL}=-1mA, I_{OH}=1mA)	$3t_{CLK\_LCP0A}$ +0	$3t_{CLK\_LCP0A}$ +50	ns	

*1: t_{CSSU}=SCSTR:CSSU[7:0] x serial chip select timing operating clock

*2: t_{CSHD}=SCSTR:CSHD[7:0] x serial chip select timing operating clock

*3: t_{CSDS}=SCSTR:CSDS[15:0] x serial chip select timing operating clock

For details on *1, *2, and *3 above, see the hardware manual.

Notes:

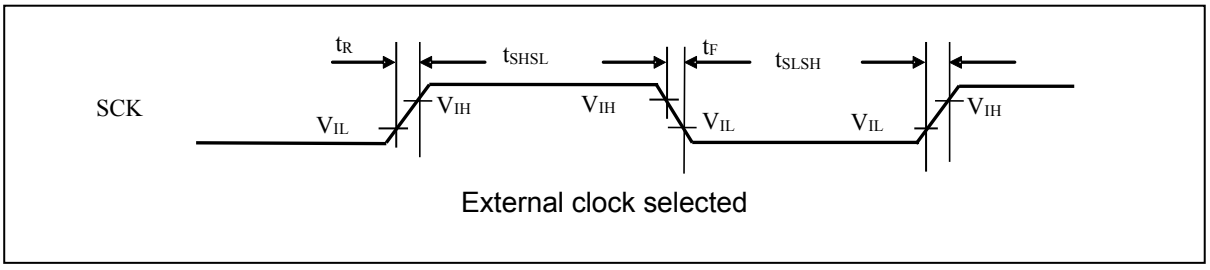
- This is the AC characteristic in CLK synchronized mode.
- CL is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.

10.4.5.3 LIN Interface (v2.1) (LIN Communication Control Interface (v2.1)) Timing (SMR:MD[2:0]=011$_B$)

(5-3-1) External Clock Selected (BGR:EXT=1)

(T_A: Recommended operating conditions, V_{CC}=5.0 V +5%/-10%, V_{SS}=AV_{SS}=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK3	(CL=50pF, I_{OL}=-2mA, I_{OH}=2mA), (CL=20pF, I_{OL}=-1mA, I_{OH}=1mA)	t_{CLK_LCP0A}+10	-	ns	
Serial clock "H" pulse width	t_{SHSL}			t_{CLK_LCP0A}+10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	



External clock selected

10.4.5.4 I^2C timing (SMR:MD[2:0]=100B)

(T_A: Recommended operating conditions, Vcc=5.0 V +5%/-10%, Vss=AVss=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Standard Mode		Unit	Remarks
				Min	Max		
SCL clock frequency	f_{SCL}	SCL0 to SCL3	C_L=50pF, R=(Vp/I_{OL})*1	0	100	kHz	
Repeat "start" condition hold time SDA ↓ → SCL ↓	t_{HDSTA}	SDA0 to SDA3 SCL0 to SCL3		4.0	-	µs	
Period of "L" for SCL clock	t_{LOW}	SCL0 to SCL3		4.7	-	µs	
Period of "H" for SCL clock	t_{HIGH}			4.0	-	µs	
Repeat "start" condition setup time SCL ↑ → SDA ↓	t_{SUSTA}	SDA0 to SDA3 SCL0 to SCL3		4.7	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}			0	3.45*2	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}			250	-	ns	
"Stop" condition setup time SCL ↑ → SDA ↑	t_{SUSTO}			4.0	-	µs	
Bus-free time between "stop" condition and "start" condition	t_{BUF}	-		4.7	-	µs	
Noise filter	t_{SP}	-		t_{NFT}*3	-	ns	

*1: R and CL represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively Vp shows that the power-supply voltage of the pull-up resistor and IOL shows the VOL guarantee current.

*2: The maximum tHDDAT only has to be met if the device does not extend the "L" width (tLOW) of the SCL signal.

*3: tNFT=(NFCR:NFT[4:0]+1) x 2 x tCLK_LCP0A

Notes:

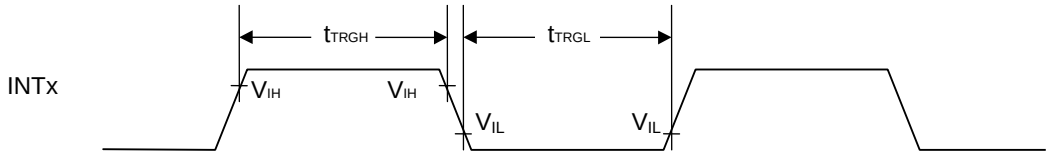
- In this device, Standard mode (Max. 100kbps) is supported only.
- This model does not support high-speed mode. (Max. 400kbps).
- This model does not support Min. I_{OL} = 3mA with V_{OL} = 0.4V.

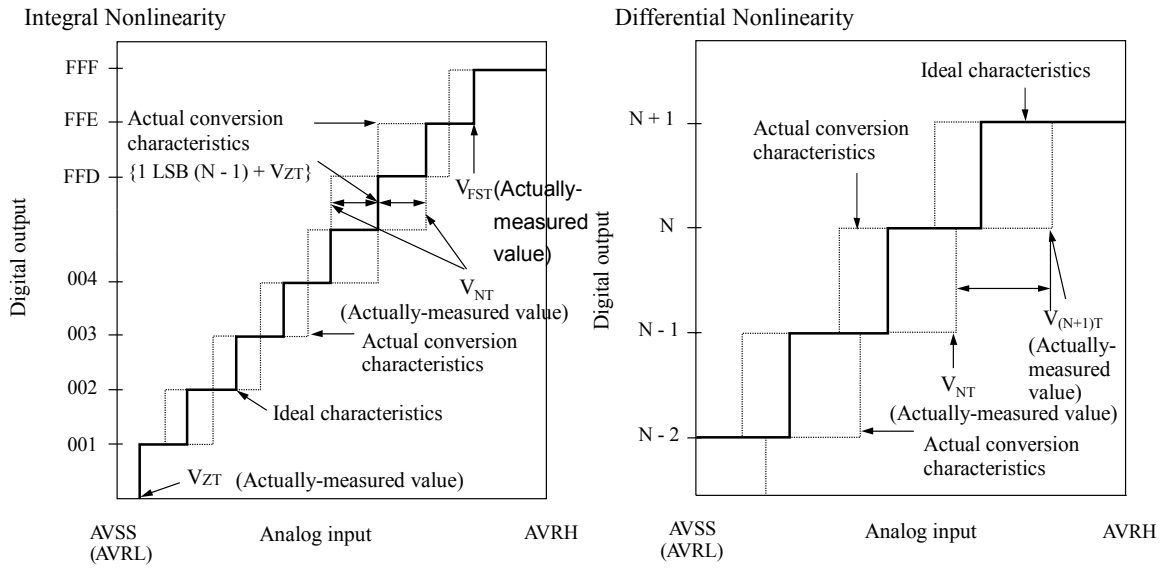
10.6 Trigger Input Timing

(T_A: Recommended operating conditions, V_{CC}=5.0 V +5%/-10%, V_{SS}=AV_{SS}=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT15	-	100	-	ns	
		INT0 to INT15	-	1	-	µs	Stop mode

- Trigger input timing





$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + V_{ZT}\}}{1\text{LSB}}\ [\text{LSB}]$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)}T - V_{NT}}{1\text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\text{LSB} = \frac{V_{FST} - V_{ZT}}{4094}\ [\text{V}]$$

V_{ZT}: Voltage for which digital output changes from "0x000" to "0x001"

V_{FST}: Voltage for which digital output changes from "0xFFE" to "0xFFF".

11. Ordering Information

Part Number	Package
S6J311xHzCSEy0000	144-pin Plastic TEQFP (LEU144)

Note:

- "x"/"y" is a part number option. For the part number option, see the following table. For details on each package, see "PACKAGE DIMENSIONS."
  * z: A

12. Part Number Option

Part Number Option "x"	FLASH Memory
A	1MByte
9	768KByte

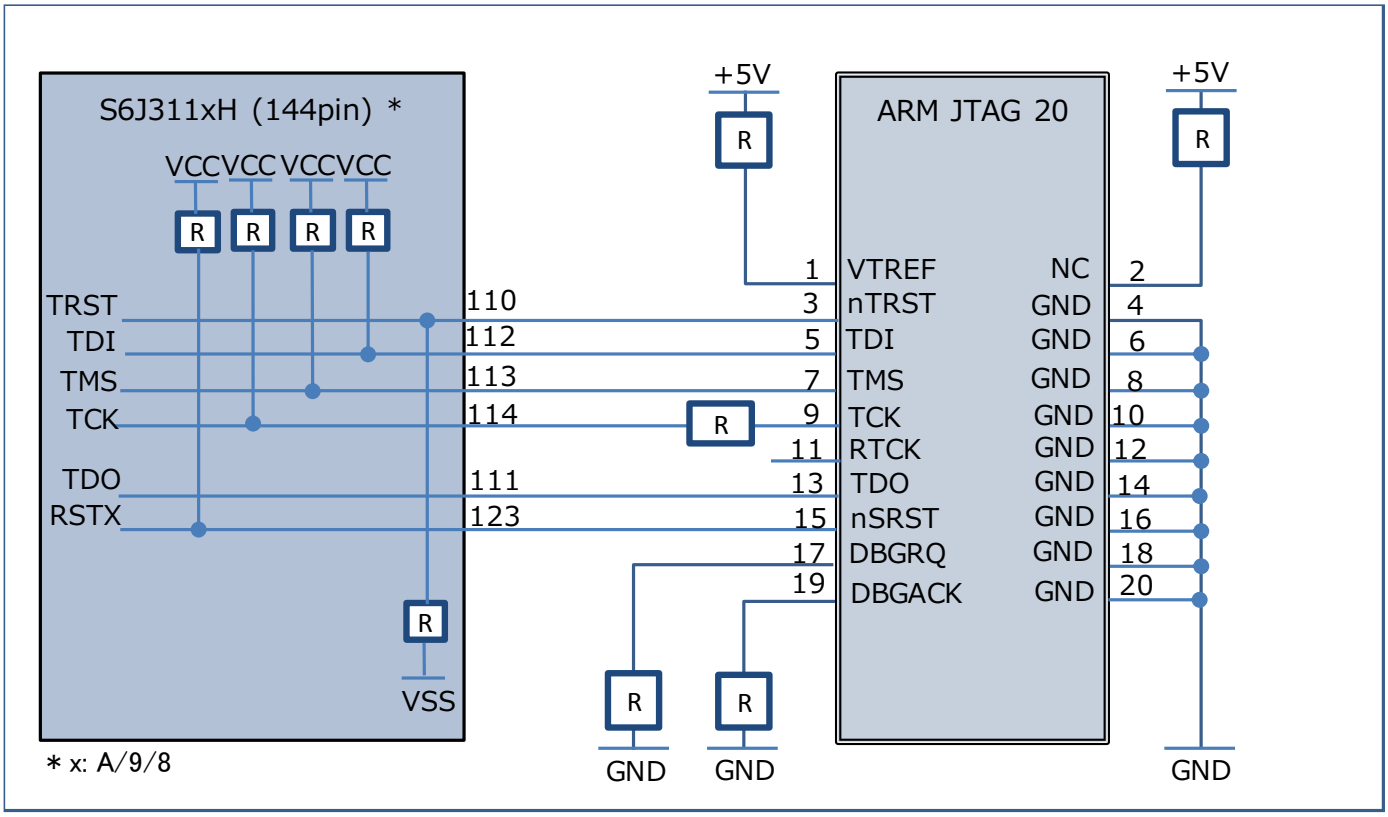
Part Number Option "y"	
2	PureSn & Halogen Free

Part Number Option "z"	SHE
A	SHE ON

14. Appendix

14.1 Application 1: JTAG tool connection

This is an application example of JTAG tool connection. See the relevant application note AN203911 in detail.



15. Major Changes

Spansion Publication Number: S6J311A_DS708-00004

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 1.0		
1,3	Cover	Added the family product names(S6J3119HAA / S6J3118HAA)
1,3	Cover	Revised the level of this data sheet as full production
6	2. Features 2.2 Peripheral Functions	Added the information about the memory capacity expansion
7	2. Features 2.2 Peripheral Functions	Revised the CAN transfer speed to 5Mbps
9	3. Product Lineup	Added the specifications as full production
11	4. Pin Assignment	Revised the product names of title S6J311AHAA-> S6J311xHAA
12	5. Pin Description	Revised the product names of title S6J311AHAA-> S6J311xHAA
12~21	5. Pin Description	Revised the product names of Pin No. S6J311AHAA-> S6J311xHAA
30	8. Handling Devices	Revised the note of “About power supply pins”
32	8. Handling Devices	Revised the note of “About C pin processing”(Delete “and pin 38”)
33	9. Block Diagram	Revised the block diagram of S6J311xHAA as full production
34	10. Memory Map	Revised the memory map of S6J311xHAA (added information of S6J3119HAA / S6J3118HAA)
36	10.Memory Map	Revised the product names of title S6J311AHAA-> S6J311xHAA
42,44,52,55	12. Electrical Characteristics	Added the product names S6J311AHAA-> S6J311xHAA
42	12. Electrical Characteristics 12.1 Absolute Maximum Ratings	Revised “Remarks” of Analog supply voltage to “AV_{CC}=V_{CC}”
42	12. Electrical Characteristics 12.1 Absolute Maximum Ratings	Revised the note of *2
42	12. Electrical Characteristics 12.1 Absolute Maximum Ratings	Revised the symbol of Maximum clamp current
43	12. Electrical Characteristics 12.1 Absolute Maximum Ratings	Moved the note of *8 to the bottom of note
44	12. Electrical Characteristics 12.2 Recommended Operating Conditions	Delete the information about CS2
44	12. Electrical Characteristics 12.2 Recommended Operating Conditions	Revised C pin connection diagram
44	12. Electrical Characteristics 12.2 Recommended Operating Conditions	Added “Remarks” of Smoothing capacitor
45	12. Electrical Characteristics 12.3 DC Characteristics	Revised the minimum value of VIH6 2.0 -> 2.3
52	12. Electrical Characteristics 12.3 DC Characteristics	Revised the following DC characteristics I_{CC5}, I_{CCS5}, I_{CCT52}, I_{CCH52}
55	12. Electrical Characteristics 12.4.2 Internal Clock Timing	Revised the product names in the table S6J311AHAA-> S6J311xHAA
55	12. Electrical Characteristics 12.4.2 Internal Clock Timing	Delete the line of FCD0_CLK and tCD0_CLK
57	12. Electrical Characteristics 12.4.2 Internal Clock Timing	Revised the note as follow FCDO_CLK->FCPU_CLK
58	12. Electrical Characteristics 12.4.2 Internal Clock Timing	Revised the voltage value of Hysteresis input pin (TTL). 2.0V -> 2.3V
60	12. Electrical Characteristics 12.4.4 Power-on Conditions	Revised the value of Level detection voltage
60	12. Electrical Characteristics 12.4.4 Power-on Conditions	Added the line of Level release voltage