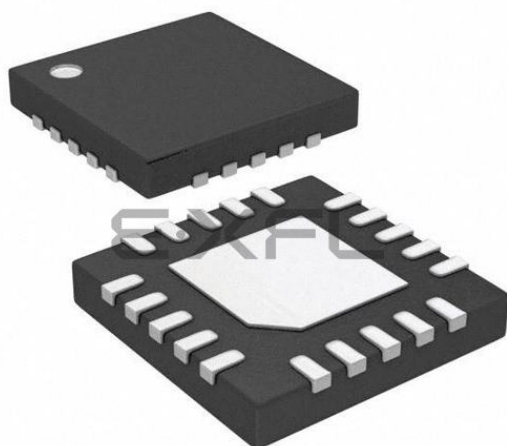




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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                                                                     |
|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Active                                                                                                                                                              |
| Core Processor             | PIC                                                                                                                                                                 |
| Core Size                  | 8-Bit                                                                                                                                                               |
| Speed                      | 32MHz                                                                                                                                                               |
| Connectivity               | I <sup>2</sup> C, LINbus, SPI, UART/USART                                                                                                                           |
| Peripherals                | Brown-out Detect/Reset, POR, PWM, WDT                                                                                                                               |
| Number of I/O              | 17                                                                                                                                                                  |
| Program Memory Size        | 7KB (4K x 14)                                                                                                                                                       |
| Program Memory Type        | FLASH                                                                                                                                                               |
| EEPROM Size                | 256 x 8                                                                                                                                                             |
| RAM Size                   | 512 x 8                                                                                                                                                             |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 5.5V                                                                                                                                                         |
| Data Converters            | A/D 17x12b; D/A 1x5b                                                                                                                                                |
| Oscillator Type            | Internal                                                                                                                                                            |
| Operating Temperature      | -40°C ~ 125°C (TA)                                                                                                                                                  |
| Mounting Type              | Surface Mount                                                                                                                                                       |
| Package / Case             | 20-UFQFN Exposed Pad                                                                                                                                                |
| Supplier Device Package    | 20-UQFN (4x4)                                                                                                                                                       |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16f18444-e-gz">https://www.e-xfl.com/product-detail/microchip-technology/pic16f18444-e-gz</a> |



# PIC16(L)F184XX

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## Full-Featured, Low Pin Count Microcontrollers with XLP

### Product Brief

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### Description

PIC16(L)F184XX microcontrollers feature Intelligent Analog, Core Independent Peripherals (CIPs) and communication peripherals combined with eXtreme Low-Power (XLP) for a wide range of general purpose and low-power applications. Features such as a 12-bit Analog-to-Digital Converter with Computation (ADC<sup>2</sup>), Memory Access Partitioning (MAP), the Device Information Area (DIA), Power-saving operating modes, and Peripheral Pin Select (PPS), offer flexible solutions for a wide variety of custom applications.

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### Core Features

- C Compiler Optimized RISC Architecture
- Only 48 instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Timers:
  - Up to two 24-bit timers
  - Up to four 8-bit timers
  - Up to four 16-bit timers
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRTE)
- Brown-out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Variable prescaler selection
  - Variable window size selection
  - Configurable in hardware (Configuration Words) and/or software
- Programmable Code Protection

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### Memory

- Up to 28 KB Program Flash Memory
- Up to 2 KB Data SRAM Memory
- 256B Data EEPROM

- Direct, Indirect and Relative Addressing modes
- Memory Access Partition (MAP):
  - Write-protect
  - Customizable partition
- Device Information Area (DIA)
- Device Configuration Information (DCI)

## Operating Characteristics

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- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF184XX)
  - 2.3V to 5.5V (PIC16F184XX)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

## Power-Saving Operation Modes

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- Doze: CPU and Peripherals Running at Different Cycle Rates (typically CPU is lower)
- Idle: CPU Halted While Peripherals Operate
- Sleep: Lowest Power Consumption
- Peripheral Module Disable (PMD):
  - Ability to selectively disable hardware module to minimize active power consumption of unused peripherals

## eXtreme Low-Power (XLP) Features

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- Sleep mode: 50 nA @ 1.8, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical

## Digital Peripherals

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- Configurable Logic Cell (CLC):
  - 4 CLCs
  - Integrated combinational and sequential logic
- Complementary Waveform Generator (CWG):
  - Up to 3 CWGs
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
- Capture/Compare/PWM (CCP) modules:

- Up to 5 CCPs
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- Pulse-Width Modulators (PWM):
  - 2 10-bit PWMs
- Numerically Controlled Oscillator (NCO):
  - Precision linear frequency generator (@50% duty cycle) with 0.0001% step size of source input clock
  - Input Clock:  $0 \text{ Hz} < f_{\text{NCO}} < 32 \text{ MHz}$
  - Resolution:  $f_{\text{NCO}}/2^{20}$
- Peripheral Pin Select (PPS):
  - I/O pin remapping of digital peripherals
- Serial Communications:
  - EUSART
    - Up to 2 EUSARTs
    - RS-232, RS-485, LIN compatible
    - Auto-Baud Detect, Auto-wake-up on Start.
  - Master Synchronous Serial Port (MSSP)
    - Up to 2 MSSPs
    - SPI
    - I<sup>2</sup>C, SMBus and PMBus™ compatible
- Data Signal Modulator (DSM)
  - Modulates a carrier signal with digital data to create custom carrier synchronized output waveforms
- Up to 26 I/O Pins:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change with edge-select
  - Input level selection control (ST or TTL)
  - Digital open-drain enable
- Timer modules:
  - Timer0:
    - 8/16-bit timer/counter
    - Synchronous or asynchronous operation
    - Programmable prescaler/postscaler
    - Time base for capture/compare function
  - Timer1/3/5 with gate control:
    - 16-bit timer/counter
    - Programmable internal or external clock sources
    - Multiple gate sources
    - Multiple gate modes
    - Time base for capture/compare function
  - Timer2/4/6 with Hardware Limit Timer:
    - 8-bit timers

- Programmable prescaler/postscaler
- Time base for PWM function
- Hardware Limit (HLT) and one-shot extensions
- Selectable clock sources
- Signal Measurement Timer (SMT)
  - Up to 2 SMTs
  - 24-bit timer/counter with programmable prescaler

## Analog Peripherals

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- Analog-to-Digital Converter (ADC):
  - 12-bit with up to 24 external channels
  - Conversion available during Sleep
  - Automated post-processing
  - Automated math functions on input signals:
    - Averaging, filter calculations, oversampling and threshold comparison
  - Integrated charge pump for low-voltage operation
  - CVD support
- Zero-Cross Detect (ZCD):
  - AC high voltage zero-crossing detection for simplifying TRIAC control
  - Synchronized switching control and timing
- Temperature Sensor Circuit
- Comparator:
  - 2 Comparators
  - Fixed Voltage Reference at (non)inverting input(s)
  - Comparator outputs externally accessible
- Digital-to-Analog Converter (DAC):
  - 5-bit resolution, rail-to-rail
  - Positive Reference Selection
  - Unbuffered I/O pin output
  - Internal connections to ADCs and comparators
- Fixed Voltage Reference (FVR) module:
  - 1.024V, 2.048V and 4.096V output levels

## Flexible Oscillator Structure

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- High-Precision Internal Oscillator:
  - Software-selectable frequency range up to 32 MHz
  - $\pm 2\%$  at calibration (nominal)
- 4x PLL for use with external sources
  - up to 32 MHz (4-8 MHz input)
- 2x PLL for use with the HFINTOSC
  - up to 32 MHz
- Low-Power Internal 31 kHz Oscillator (LFINTOSC)
- External 32.768 kHz Crystal Oscillator (SOCS)

- External Oscillator Block with:
  - Three crystal/resonator modes up to 20 MHz
  - Three external clock modes up to 32 MHz
  - Fail-Safe Clock Monitor
    - Detects clock source failure
  - Oscillator Start-up Timer (OST)
    - Ensures stability of crystal oscillator sources

## Family Types

Table 1. PIC16(L)F184XX Family Types

| Device         | Program Flash Memory (Words) | Program Flash Memory (Kbytes) | Data Memory (EEPROM) (bytes) | Data SRAM (bytes) | I/O's <sup>(2)</sup> | 12-bit ADC (ch) | 5-bit DAC | Comparators | CWG | Clock Ref | Timers (8/16-bit) | CCP | PWM | NCO | EUSART | MSSP (I <sup>2</sup> C/SPI) | CLC | DSM | PPS | XLP | PMD | Windowed Watchdog Timer | Memory Access Partition | Device Information Area | Debug <sup>(1)</sup> |
|----------------|------------------------------|-------------------------------|------------------------------|-------------------|----------------------|-----------------|-----------|-------------|-----|-----------|-------------------|-----|-----|-----|--------|-----------------------------|-----|-----|-----|-----|-----|-------------------------|-------------------------|-------------------------|----------------------|
| PIC16(L)F18424 | 4096                         | 7                             | 256                          | 512               | 12                   | 11              | 1         | 2           | 2   | 1         | 4/4               | 4   | 2   | 1   | 1      | 1                           | 4   | 1   | Y   | Y   | Y   | Y                       | Y                       | Y                       | I                    |
| PIC16(L)F18425 | 8192                         | 14                            | 256                          | 1024              | 12                   | 11              | 1         | 2           | 2   | 1         | 4/4               | 4   | 2   | 1   | 1      | 2                           | 4   | 1   | Y   | Y   | Y   | Y                       | Y                       | Y                       | I                    |
| PIC16(L)F18426 | 16384                        | 28                            | 256                          | 2048              | 12                   | 11              | 1         | 2           | 2   | 1         | 4/4               | 4   | 2   | 1   | 1      | 2                           | 4   | 1   | Y   | Y   | Y   | Y                       | Y                       | Y                       | I                    |
| PIC16(L)F18444 | 4096                         | 7                             | 256                          | 512               | 12                   | 17              | 1         | 2           | 2   | 1         | 4/4               | 4   | 2   | 1   | 1      | 1                           | 4   | 1   | Y   | Y   | Y   | Y                       | Y                       | Y                       | I                    |
| PIC16(L)F18445 | 8192                         | 14                            | 256                          | 1024              | 12                   | 17              | 1         | 2           | 2   | 1         | 4/4               | 4   | 2   | 1   | 1      | 2                           | 4   | 1   | Y   | Y   | Y   | Y                       | Y                       | Y                       | I                    |
| PIC16(L)F18446 | 16384                        | 28                            | 256                          | 2048              | 12                   | 17              | 1         | 2           | 2   | 1         | 4/4               | 4   | 2   | 1   | 1      | 2                           | 4   | 1   | Y   | Y   | Y   | Y                       | Y                       | Y                       | I                    |
| PIC16(L)F18455 | 8192                         | 14                            | 256                          | 1024              | 26                   | 24              | 1         | 2           | 3   | 1         | 4/4               | 5   | 2   | 1   | 2      | 2                           | 4   | 1   | Y   | Y   | Y   | Y                       | Y                       | Y                       | I                    |
| PIC16(L)F18456 | 16384                        | 28                            | 256                          | 2048              | 26                   | 24              | 1         | 2           | 3   | 1         | 4/4               | 5   | 2   | 1   | 2      | 2                           | 4   | 1   | Y   | Y   | Y   | Y                       | Y                       | Y                       | I                    |

**Note:**

1. I - Debugging integrated on chip.
2. One pin is input-only.

## Packages

| Packages       | PDIP | SOIC | SSOP | TSSOP | UQFN (4x4) |
|----------------|------|------|------|-------|------------|
| PIC16(L)F18424 | •    | •    |      | •     | •          |
| PIC16(L)F18425 | •    | •    |      | •     | •          |
| PIC16(L)F18426 | •    | •    |      | •     | •          |
| PIC16(L)F18444 | •    | •    | •    |       | •          |

| Packages       | PDIP | SOIC | SSOP | TSSOP | UQFN (4x4) |
|----------------|------|------|------|-------|------------|
| PIC16(L)F18445 | •    | •    | •    |       | •          |
| PIC16(L)F18446 | •    | •    | •    |       | •          |
| PIC16(L)F18455 | •    | •    | •    |       | •          |
| PIC16(L)F18456 | •    | •    | •    |       | •          |

**Note:** Pin details are subject to change.

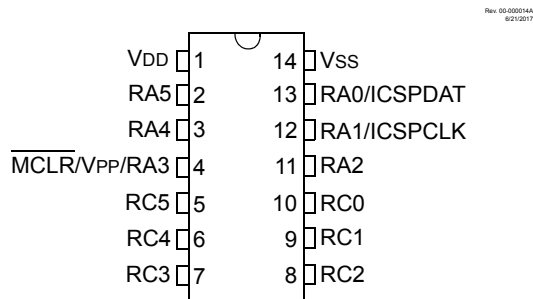


**Important:** For other small form-factor package availability and marking information, visit [www.microchip.com/packaging](http://www.microchip.com/packaging) or contact your local sales office.

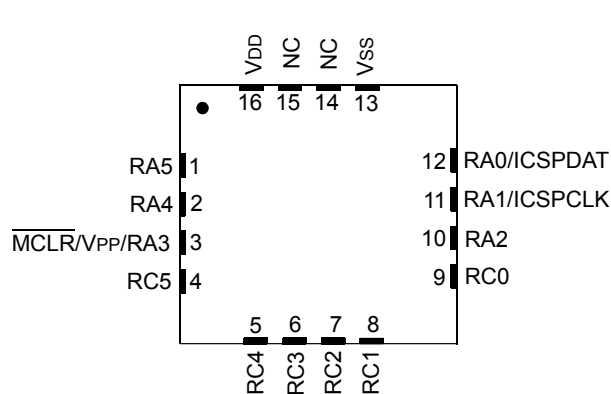
## Pin Diagrams

### 1 14/16-Pin Diagrams

**Figure 1. 14-Pin PDIP, SOIC, TSSOP**



**Figure 2. 16-Pin UQFN (4x4)**



**Note:** It is recommended that the exposed bottom pad be connected to V<sub>SS</sub>.

### Related Links

[14/16-Pin Allocation Table](#)

## 2 20-Pin Diagrams

Figure 3. 20-Pin PDIP, SOIC, TSSOP

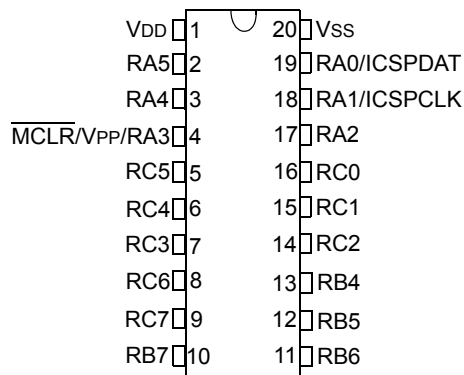
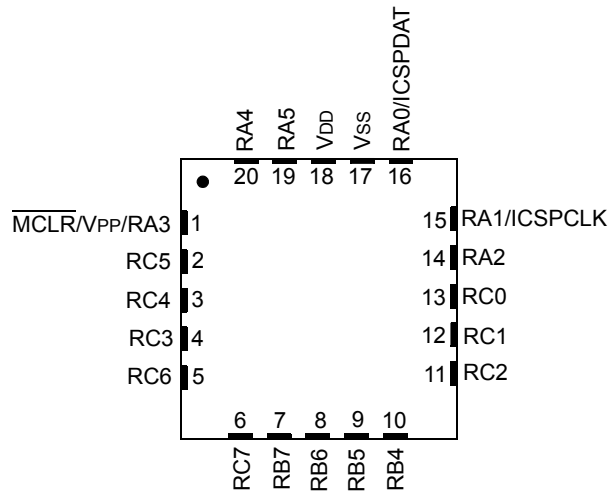


Figure 4. 20-Pin UQFN (4x4)



**Note:** It is recommended that the exposed bottom pad be connected to V<sub>SS</sub>.

### Related Links

[20-Pin Allocation Table](#)



## 3 28-Pin Diagrams

Figure 5. 28-pin SPDIP, SSOP, SOIC

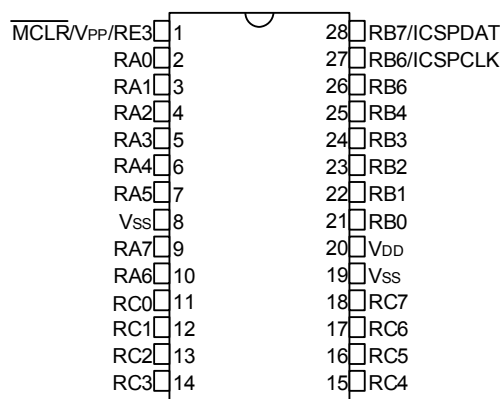
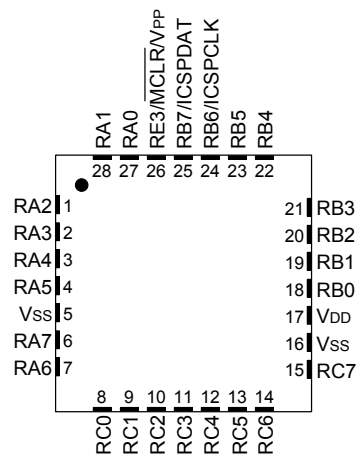


Figure 6. 28-pin UQFN



**Note:** It is recommended that the exposed bottom pad be connected to  $V_{SS}$ .

### Related Links

[28-Pin Allocation Table](#)

## Pin Allocation Tables

### 1 14/16-Pin Allocation Table

| I/O                | 14-pin PDIP/SOIC/TSSOP | 16-pin UQFN | ADC                          | Reference | Comparator       | NCO     | DAC       | DSM                   | Timers                                                                | CCP                   | PWM     | CWG                                            | MSSP                                               | ZCD  | EUSART                                     | CLC                   | CLKR | Interrupts | Pull-up | Basic                   |
|--------------------|------------------------|-------------|------------------------------|-----------|------------------|---------|-----------|-----------------------|-----------------------------------------------------------------------|-----------------------|---------|------------------------------------------------|----------------------------------------------------|------|--------------------------------------------|-----------------------|------|------------|---------|-------------------------|
| RA0                | 13                     | 12          | ANA0                         | —         | C1IN0+           | —       | DAC1OUT1  | MDSRC <sup>(1)</sup>  | —                                                                     | —                     | —       | —                                              | SS2 <sup>(1)</sup>                                 | —    | —                                          | —                     | —    | IOCA0      | Y       | ICDDAT<br>ICSPDAT       |
| RA1                | 12                     | 11          | ANA1                         | ADCVREF+  | C1IN0<br>C2IN0-  | —       | DAC1VREF+ | —                     | —                                                                     | —                     | —       | —                                              | —                                                  | —    | —                                          | —                     | —    | IOCA1      | Y       | ICDCLK<br>ICSPCLK       |
| RA2                | 11                     | 10          | ANA2                         | ADCVREF-  | —                | —       | DAC1VREF- | —                     | T0CKI <sup>(1)</sup>                                                  | CCP3IN <sup>(1)</sup> | —       | CWG1IN <sup>(1)</sup><br>CWG2IN <sup>(1)</sup> | —                                                  | ZCD1 | —                                          | —                     | —    | IOCA2      | Y       | INT0 <sup>(1)</sup>     |
| RA3                | 4                      | 3           | —                            | —         | —                | —       | —         | —                     | T6IN <sup>(1)</sup>                                                   | —                     | —       | —                                              | —                                                  | —    | —                                          | —                     | —    | IOCA3      | Y       | MCLR<br>Vpp             |
| RA4                | 3                      | 2           | ANA4                         | —         | —                | —       | —         | —                     | T1G <sup>(1)</sup><br>SMT1WIN <sup>(1)</sup>                          | —                     | —       | —                                              | —                                                  | —    | —                                          | —                     | —    | IOCA4      | Y       | CLKOUT<br>SOSCO<br>OSC2 |
| RA5                | 2                      | 1           | ANA5                         | —         | —                | —       | —         | —                     | T1CKI <sup>(1)</sup><br>T2IN <sup>(1)</sup><br>SMT1SIG <sup>(1)</sup> | —                     | —       | —                                              | —                                                  | —    | —                                          | CLCIN3 <sup>(1)</sup> | —    | IOCA5      | Y       | CLKIN<br>SOSCI<br>OSC1  |
| RC0                | 10                     | 9           | ANC0                         | —         | C2IN0+           | —       | —         | —                     | T5CKI <sup>(1)</sup>                                                  | —                     | —       | —                                              | SCK1 <sup>(1)</sup><br>SCL1 <sup>(1,3,4)</sup>     | —    | —                                          | —                     | —    | IOCC0      | Y       | —                       |
| RC1                | 9                      | 8           | ANC1                         | —         | C1IN1-<br>C2IN1- | —       | —         | —                     | T4IN <sup>(1)</sup>                                                   | CCP4IN <sup>(1)</sup> | —       | —                                              | SDI1 <sup>(1)</sup><br>SDA1 <sup>(1,3,4)</sup>     | —    | —                                          | CLCIN2 <sup>(1)</sup> | —    | IOCC1      | Y       | —                       |
| RC2                | 8                      | 7           | ANC2<br>ADACT <sup>(1)</sup> | —         | C1IN2-<br>C2IN2- | —       | —         | MDCARL <sup>(1)</sup> | —                                                                     | —                     | —       | —                                              | —                                                  | —    | —                                          | —                     | —    | IOCC2      | Y       | —                       |
| RC3                | 7                      | 6           | ANC3                         | —         | C1IN3-<br>C2IN3- | —       | —         | —                     | T5G <sup>(1)</sup>                                                    | CCP2IN <sup>(1)</sup> | —       | —                                              | SS1 <sup>(1)</sup>                                 | —    | —                                          | CLCIN0 <sup>(1)</sup> | —    | IOCC3      | Y       | —                       |
| RC4                | 6                      | 5           | ANC4                         | —         | —                | —       | —         | —                     | T3G <sup>(1)</sup>                                                    | —                     | —       | —                                              | SCK2 <sup>(1,5)</sup><br>SCL2 <sup>(1,3,4,5)</sup> | —    | CK1 <sup>(1,3)</sup>                       | CLCIN1 <sup>(1)</sup> | —    | IOCC4      | Y       | —                       |
| RC5                | 5                      | 4           | ANC5                         | —         | —                | —       | —         | MDCARH <sup>(1)</sup> | T3CKI <sup>(1)</sup>                                                  | CCP1IN <sup>(1)</sup> | —       | —                                              | SDI2 <sup>(1,5)</sup><br>SDA2 <sup>(1,3,4,5)</sup> | —    | RX1 <sup>(1)</sup><br>DT1 <sup>(1,3)</sup> | —                     | —    | IOCC5      | Y       | —                       |
| VDD                | 1                      | 16          | —                            | —         | —                | —       | —         | —                     | —                                                                     | —                     | —       | —                                              | —                                                  | —    | —                                          | —                     | —    | —          | —       | VDD                     |
| VSS                | 14                     | 13          | —                            | —         | —                | —       | —         | —                     | —                                                                     | —                     | —       | —                                              | —                                                  | —    | —                                          | —                     | —    | —          | —       | VSS                     |
| OUT <sup>(2)</sup> | —                      | —           | ADCGRDA                      | —         | C1OUT            | NCO1OUT | —         | DSM1OUT               | TMR0OUT                                                               | CCP1OUT               | PWM6OUT | CWG1A<br>CWG2A                                 | SDO1<br>SDO2                                       | —    | DT1 <sup>(3)</sup>                         | CLC1OUT               | CLKR | —          | —       | —                       |

| I/O | 14-pin PDIP/SOIC/TSSOP | 16-pin UQFN | ADC     | Reference | Comparator | NCO | DAC | DSM | Timers | CCP     | PWM     | CWG            | MSSP                                       | ZCD | EUSART             | CLC     | CLKR | Interrupts | Pull-up | Basic |
|-----|------------------------|-------------|---------|-----------|------------|-----|-----|-----|--------|---------|---------|----------------|--------------------------------------------|-----|--------------------|---------|------|------------|---------|-------|
|     | —                      | —           | ADCGRDB | —         | C2OUT      | —   | —   | —   | —      | CCP2OUT | PWM7OUT | CWG1B<br>CWG2B | SCK1<br>SCK2                               | —   | CK1 <sup>(3)</sup> | CLC2OUT | —    | —          | —       | —     |
|     | —                      | —           | —       | —         | —          | —   | —   | —   | —      | CCP3OUT | —       | CWG1C<br>CWG2C | SCL1 <sup>(3)</sup><br>SCL2 <sup>(3)</sup> | —   | TX1                | CLC3OUT | —    | —          | —       | —     |
|     | —                      | —           | —       | —         | —          | —   | —   | —   | —      | CCP4OUT | —       | CWG1D<br>CWG2D | SDA1 <sup>(3)</sup><br>SDA2 <sup>(3)</sup> | —   | —                  | CLC4OUT | —    | —          | —       | —     |

## Note:

1. This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2. All digital output signals shown in these rows are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
3. This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4. These pins are configured for I<sup>2</sup>C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBUS input buffer thresholds.
5. MSSP2 is not available on the PIC16(L)F18424 or PIC16(L)F18444 devices.

## 2 20-Pin Allocation Table

| I/O | 20-pin PDIP/SOIC/TSSOP | 20-pin UQFN | ADC  | Reference    | Comparator       | NCO | DAC           | DSM                  | Timers               | CCP                   | PWM | CWG                                            | MSSP               | ZCD  | EUSART | CLC                   | CLKR | Interrupts | Pull-up | Basic               |
|-----|------------------------|-------------|------|--------------|------------------|-----|---------------|----------------------|----------------------|-----------------------|-----|------------------------------------------------|--------------------|------|--------|-----------------------|------|------------|---------|---------------------|
| RA0 | 19                     | 16          | ANA0 | —            | C1IN0+           | —   | DAC1OUT1      | —                    | —                    | —                     | —   | —                                              | —                  | —    | —      | —                     | —    | IOCA0      | Y       | ICDDAT/<br>ICSPDAT  |
| RA1 | 18                     | 15          | ANA1 | ADCVREF<br>+ | C1IN0-<br>C2IN0- | —   | DAC1VREF<br>+ | MDSRC <sup>(1)</sup> | —                    | —                     | —   | —                                              | SS2 <sup>(1)</sup> | —    | —      | —                     | —    | IOCA1      | Y       | ICDCLK/<br>ICSPCLK  |
| RA2 | 17                     | 14          | ANA2 | ADCVREF-     | —                | —   | DAC1VREF-     | —                    | T0CKI <sup>(1)</sup> | —                     | —   | CWG1IN <sup>(1)</sup><br>CWG2IN <sup>(1)</sup> | —                  | ZCD1 | —      | CLCIN0 <sup>(1)</sup> | —    | IOCA2      | Y       | INT0 <sup>(1)</sup> |
| RA3 | 4                      | 1           | —    | —            | —                | —   | —             | —                    | —                    | —                     | —   | —                                              | —                  | —    | —      | —                     | —    | IOCA3      | Y       | MCLR<br>Vpp         |
| RA4 | 3                      | 20          | ANA4 | —            | —                | —   | —             | —                    | T1G <sup>(1)</sup>   | CCP4IN <sup>(1)</sup> | —   | —                                              | —                  | —    | —      | —                     | —    | IOCA4      | Y       | CLKOUT              |

# PIC16(L)F184XX

| I/O                | 20-pin PDIP/SOIC/TSSOP | 20-pin UQFN | ADC                          | Reference | Comparator       | NCO     | DAC | DSM                   | Timers                                                                | CCP                   | PWM     | CWG            | MSSP                                               | ZCD | EUSART                                     | CLC                   | CLKR | Interrupts | Pull-up | Basic                  |
|--------------------|------------------------|-------------|------------------------------|-----------|------------------|---------|-----|-----------------------|-----------------------------------------------------------------------|-----------------------|---------|----------------|----------------------------------------------------|-----|--------------------------------------------|-----------------------|------|------------|---------|------------------------|
|                    |                        |             |                              |           |                  |         |     |                       | SMT1WIN <sup>(1)</sup>                                                |                       |         |                |                                                    |     |                                            |                       |      |            |         | SOSCO<br>OSC2          |
| RA5                | 2                      | 19          | ANA5                         | —         | —                | —       | —   | —                     | T1CKI <sup>(1)</sup><br>T2IN <sup>(1)</sup><br>SMT1SIG <sup>(1)</sup> | —                     | —       | —              | —                                                  | —   | —                                          | —                     | —    | IOCA5      | Y       | CLKIN<br>SOSCI<br>OSC1 |
| RB4                | 13                     | 10          | ANB4                         | —         | —                | —       | —   | —                     | T5G <sup>(1)</sup>                                                    | —                     | —       | —              | SDI1 <sup>(1)</sup><br>SDA1 <sup>(1,3,4)</sup>     | —   | —                                          | CLCIN2 <sup>(1)</sup> | —    | IOCB4      | Y       | —                      |
| RB5                | 12                     | 9           | ANB5                         | —         | —                | —       | —   | —                     | —                                                                     | CCP3IN <sup>(1)</sup> | —       | —              | SCK2 <sup>(1,5)</sup><br>SCL2 <sup>(1,3,4,5)</sup> | —   | RX1 <sup>(1)</sup><br>DT1 <sup>(1,3)</sup> | CLCIN3 <sup>(1)</sup> | —    | IOCB5      | Y       | —                      |
| RB6                | 11                     | 8           | ANB6                         | —         | —                | —       | —   | —                     | —                                                                     | —                     | —       | —              | SCK1 <sup>(1)</sup><br>SCL1 <sup>(1,3,4)</sup>     | —   | —                                          | —                     | —    | IOCB6      | Y       | —                      |
| RB7                | 10                     | 7           | ANB7                         | —         | —                | —       | —   | —                     | T6IN <sup>(1)</sup>                                                   | —                     | —       | —              | SDI2 <sup>(1,5)</sup><br>SDA2 <sup>(1,3,4,5)</sup> | —   | CK1 <sup>(1,3)</sup>                       | —                     | —    | IOCB7      | Y       | —                      |
| RC0                | 16                     | 13          | ANC0                         | —         | C2IN0+           | —       | —   | —                     | T3CKI <sup>(1)</sup><br>T3G <sup>(1)</sup>                            | —                     | —       | —              | —                                                  | —   | —                                          | —                     | —    | IOCC0      | Y       | —                      |
| RC1                | 15                     | 12          | ANC1                         | —         | C1IN1-<br>C2IN1- | —       | —   | —                     | —                                                                     | —                     | —       | —              | —                                                  | —   | —                                          | —                     | —    | IOCC1      | Y       | —                      |
| RC2                | 14                     | 11          | ANC2<br>ADACT <sup>(1)</sup> | —         | C1IN2-<br>C2IN2- | —       | —   | MDCARL <sup>(1)</sup> | T5CKI <sup>(1)</sup>                                                  | —                     | —       | —              | —                                                  | —   | —                                          | —                     | —    | IOCC2      | Y       | —                      |
| RC3                | 7                      | 4           | ANC3                         | —         | C1IN3-<br>C2IN3- | —       | —   | —                     | —                                                                     | CCP2IN <sup>(1)</sup> | —       | —              | —                                                  | —   | —                                          | CLCIN1 <sup>(1)</sup> | —    | IOCC3      | Y       | —                      |
| RC4                | 6                      | 3           | ANC4                         | —         | —                | —       | —   | —                     | —                                                                     | —                     | —       | —              | —                                                  | —   | —                                          | —                     | —    | IOCC4      | Y       | —                      |
| RC5                | 5                      | 2           | ANC5                         | —         | —                | —       | —   | MDCARH <sup>(1)</sup> | T4IN <sup>(1)</sup>                                                   | CCP1IN <sup>(1)</sup> | —       | —              | —                                                  | —   | —                                          | —                     | —    | IOCC5      | Y       | —                      |
| RC6                | 8                      | 5           | ANC6                         | —         | —                | —       | —   | —                     | —                                                                     | —                     | —       | —              | SS1 <sup>(1)</sup>                                 | —   | —                                          | —                     | —    | IOCC6      | Y       | —                      |
| RC7                | 9                      | 6           | ANC7                         | —         | —                | —       | —   | —                     | —                                                                     | —                     | —       | —              | —                                                  | —   | —                                          | —                     | —    | IOCC7      | Y       | —                      |
| VDD                | 1                      | 18          | —                            | —         | —                | —       | —   | —                     | —                                                                     | —                     | —       | —              | —                                                  | —   | —                                          | —                     | —    | —          | —       | VDD                    |
| VSS                | 20                     | 17          | —                            | —         | —                | —       | —   | —                     | —                                                                     | —                     | —       | —              | —                                                  | —   | —                                          | —                     | —    | —          | —       | VSS                    |
| OUT <sup>(2)</sup> | —                      | —           | ADCGRDA                      | —         | C1OUT            | NCO1OUT | —   | DSM1OUT               | TMR0OUT                                                               | CCP1OUT               | PWM6OUT | CWG1A<br>CWG2A | SDO1<br>SDO2                                       | —   | DT1 <sup>(3)</sup>                         | CLC1OUT               | CLKR | —          | —       | —                      |
|                    | —                      | —           | ADCGRDB                      | —         | C2OUT            | —       | —   | —                     | —                                                                     | CCP2OUT               | PWM7OUT | CWG1B<br>CWG2B | SCK1<br>SCK2                                       | —   | CK1 <sup>(3)</sup>                         | CLC2OUT               | —    | —          | —       | —                      |

| I/O | 20-pin PDIP/SOIC/TSSOP | 20-pin UQFN | ADC | Reference | Comparator | NCO | DAC | DSM | Timers | CCP     | PWM | CWG            | MSSP                                       | ZCD | EUSART | CLC     | CLKR | Interrupts | Pull-up | Basic |
|-----|------------------------|-------------|-----|-----------|------------|-----|-----|-----|--------|---------|-----|----------------|--------------------------------------------|-----|--------|---------|------|------------|---------|-------|
|     | —                      | —           | —   | —         | —          | —   | —   | —   | —      | CCP3OUT | —   | CWG1C<br>CWG2C | SCL1 <sup>(3)</sup><br>SCL2 <sup>(3)</sup> | —   | TX1    | CLC3OUT | —    | —          | —       | —     |
|     | —                      | —           | —   | —         | —          | —   | —   | —   | —      | CCP4OUT | —   | CWG1D<br>CWG2D | SDA1 <sup>(3)</sup><br>SDA2 <sup>(3)</sup> | —   | —      | CLC4OUT | —    | —          | —       | —     |

## Note:

1. This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2. All digital output signals shown in these rows are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
3. This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4. These pins are configured for I<sup>2</sup>C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBUS input buffer thresholds.
5. MSSP2 is not available on the PIC16(L)F18424 or PIC16(L)F18444 devices.

## 3 28-Pin Allocation Table

| I/O | 28-pin PDIP/SOIC/TSSOP | 28-pin UQFN | ADC  | Reference | Comparator       | NCO | DAC                   | DSM                   | Timers               | CCP                   | PWM | CWG                   | MSSP               | ZCD  | EUSART | CLC                   | CLKR | Interrupts | Pull-up | Basic               |
|-----|------------------------|-------------|------|-----------|------------------|-----|-----------------------|-----------------------|----------------------|-----------------------|-----|-----------------------|--------------------|------|--------|-----------------------|------|------------|---------|---------------------|
| RA0 | 2                      | 27          | ANA0 | —         | C1IN0-<br>C2IN0- | —   | —                     | —                     | —                    | —                     | —   | —                     | —                  | —    | —      | CLCIN0 <sup>(1)</sup> | —    | IOCA0      | Y       | —                   |
| RA1 | 3                      | 28          | ANA1 | —         | C1IN1-<br>C2IN1- | —   | —                     | —                     | —                    | —                     | —   | —                     | —                  | —    | —      | CLCIN1 <sup>(1)</sup> | —    | IOCA1      | Y       | —                   |
| RA2 | 4                      | 1           | ANA2 | ADCVREF-  | C1IN0+<br>C2IN0+ | —   | DAC1VREF-<br>DAC1OUT1 | —                     | —                    | —                     | —   | —                     | —                  | —    | —      | —                     | —    | IOCA2      | Y       | —                   |
| RA3 | 5                      | 2           | ANA3 | ADCVREF+  | C1IN1+           | —   | DAC1VREF+             | MDCARL <sup>(1)</sup> | —                    | —                     | —   | —                     | —                  | —    | —      | —                     | —    | IOCA3      | Y       | —                   |
| RA4 | 6                      | 3           | ANA4 | —         | —                | —   | —                     | MDCARH <sup>(1)</sup> | T0CKI <sup>(1)</sup> | CCP5IN <sup>(1)</sup> | —   | —                     | —                  | —    | —      | —                     | —    | IOCA4      | Y       | —                   |
| RA5 | 7                      | 4           | ANA5 | —         | —                | —   | —                     | MDSRC <sup>(1)</sup>  | —                    | —                     | —   | —                     | SS1 <sup>(1)</sup> | —    | —      | —                     | —    | IOCA5      | Y       | —                   |
| RA6 | 10                     | 7           | ANA6 | —         | —                | —   | —                     | —                     | —                    | —                     | —   | —                     | —                  | —    | —      | —                     | —    | IOCA6      | Y       | OSC2<br>CLKOUT      |
| RA7 | 9                      | 6           | ANA7 | —         | —                | —   | —                     | —                     | —                    | —                     | —   | —                     | —                  | —    | —      | —                     | —    | IOCA7      | Y       | OSC1<br>CLKIN       |
| RB0 | 21                     | 18          | ANB0 | —         | C2IN1+           | —   | —                     | —                     | —                    | CCP4IN <sup>(1)</sup> | —   | CWG1IN <sup>(1)</sup> | —                  | ZCD1 | —      | —                     | —    | IOCB0      | Y       | INT0 <sup>(1)</sup> |

# PIC16(L)F184XX

| I/O    | 28-pin PDIP/SOIC/TSSOP | 28-pin UQFN | ADC              | Reference | Comparator       | NCO | DAC      | DSM     | Timers                                       | CCP       | PWM     | CWG                     | MSSP                       | ZCD | EUSART             | CLC                | CLKR | Interrupts | Pull-up | Basic             |
|--------|------------------------|-------------|------------------|-----------|------------------|-----|----------|---------|----------------------------------------------|-----------|---------|-------------------------|----------------------------|-----|--------------------|--------------------|------|------------|---------|-------------------|
| RB1    | 22                     | 19          | ANB1             | —         | C1IN3-<br>C2IN3- | —   | —        | —       | —                                            | —         | —       | CWG2IN(1)               | SCK2(1)<br>SCL2(1,3)       | —   | —                  | —                  | —    | IOCB1      | Y       | —                 |
| RB2    | 23                     | 20          | ANB2             | —         | —                | —   | —        | —       | —                                            | —         | —       | CWG3IN(1)               | SDI2(1)<br>SDA2(1,3)SS2(1) | —   | —                  | —                  | —    | IOCB2      | Y       | —                 |
| RB3    | 24                     | 21          | ANB3             | —         | C1IN2-<br>C2IN2- | —   | —        | —       | —                                            | —         | —       | —                       | —                          | —   | —                  | —                  | —    | IOCB3      | Y       | —                 |
| RB4    | 25                     | 22          | ANB4<br>ADACT(1) | —         | —                | —   | —        | —       | T5G(1)<br>SMT2WIN(1)                         | —         | —       | —                       | —                          | —   | —                  | —                  | —    | IOCB4      | Y       | —                 |
| RB5    | 26                     | 23          | ANB5             | —         | —                | —   | —        | —       | T1G(1)<br>SMT2SIG(1)                         | CCP3IN(1) | —       | —                       | —                          | —   | —                  | —                  | —    | IOCB5      | Y       | —                 |
| RB6    | 27                     | 24          | ANB6             | —         | —                | —   | —        | —       | —                                            | —         | —       | —                       | —                          | —   | CK2(1,3)           | CLCIN2(1)          | —    | IOCB6      | Y       | ICSPCLK<br>ICDCLK |
| RB7    | 28                     | 25          | ANB7             | —         | —                | —   | DAC1OUT2 | —       | T6IN(1)                                      | —         | —       | —                       | —                          | —   | RX2(1)<br>DT2(1,3) | —                  | —    | IOCB7      | Y       | ICSPDAT<br>ICDDAT |
| RC0    | 11                     | 8           | ANC0             | —         | —                | —   | —        | —       | T1CKI(1)<br>T3CKI(1)<br>T3G(1)<br>SMT1WIN(1) | —         | —       | —                       | —                          | —   | —                  | —                  | —    | IOCC0      | Y       | SOSCO             |
| RC1    | 12                     | 9           | ANC1             | —         | —                | —   | —        | —       | SMT1SIG(1)                                   | CCP2IN(1) | —       | —                       | —                          | —   | —                  | —                  | —    | IOCC1      | Y       | SOSCI             |
| RC2    | 13                     | 10          | ANC2             | —         | —                | —   | —        | —       | T5CKI(1)                                     | CCP1IN(1) | —       | —                       | —                          | —   | —                  | —                  | —    | IOCC2      | Y       | —                 |
| RC3    | 14                     | 11          | ANC3             | —         | —                | —   | —        | —       | T2IN(1)                                      | —         | —       | —                       | SCK1(1)<br>SCL1(1,3)       | —   | —                  | —                  | —    | IOCC3      | Y       | —                 |
| RC4    | 15                     | 12          | ANC4             | —         | —                | —   | —        | —       | —                                            | —         | —       | —                       | SDI1(1)<br>SDA1(1,3)       | —   | —                  | —                  | —    | IOCC4      | Y       | —                 |
| RC5    | 16                     | 13          | ANC5             | —         | —                | —   | —        | —       | T4IN(1)                                      | —         | —       | —                       | —                          | —   | —                  | —                  | —    | IOCC5      | Y       | —                 |
| RC6    | 17                     | 14          | ANC6             | —         | —                | —   | —        | —       | —                                            | —         | —       | —                       | —                          | —   | —                  | CK1(1,3)           | —    | IOCC6      | Y       | —                 |
| RC7    | 18                     | 15          | ANC7             | —         | —                | —   | —        | —       | —                                            | —         | —       | —                       | —                          | —   | —                  | RX1(1)<br>DT1(1,3) | —    | IOCC7      | Y       | —                 |
| RE3    | 1                      | 26          | —                | —         | —                | —   | —        | —       | —                                            | —         | —       | —                       | —                          | —   | —                  | —                  | —    | IOCE3      | Y       | MCLR<br>VPP       |
| VDD    | 20                     | 17          | —                | —         | —                | —   | —        | —       | —                                            | —         | —       | —                       | —                          | —   | —                  | —                  | —    | —          | —       | VDD               |
| VSS    | 8                      | 5           | —                | —         | —                | —   | —        | —       | —                                            | —         | —       | —                       | —                          | —   | —                  | —                  | —    | —          | —       | VSS               |
| VSS    | 19                     | 16          | —                | —         | —                | —   | —        | —       | —                                            | —         | —       | —                       | —                          | —   | —                  | —                  | —    | —          | —       | VSS               |
| OUT(2) | —                      | —           | ADCGRDA          | —         | C1OUT<br>NCO1OUT | —   | —        | DSM1OUT | TMR0OUT                                      | CCP1OUT   | PWM6OUT | CWG1A<br>CWG2A<br>CWG3A | SDO1<br>SDO2               | —   | DT1(3)<br>DT2(3)   | CLC1OUT            | CLKR | —          | —       | —                 |

| I/O | 28-pin PDIP/SOIC/TSSOP | 28-pin UQFN | ADC     | Reference | Comparator | NCO | DAC | DSM | Timers | CCP     | PWM     | CWG                     | MSSP               | ZCD | EUSART           | CLC     | CLKR | Interrupts | Pull-up | Basic |
|-----|------------------------|-------------|---------|-----------|------------|-----|-----|-----|--------|---------|---------|-------------------------|--------------------|-----|------------------|---------|------|------------|---------|-------|
| —   | —                      | —           | ADCGRDB | —         | C2OUT      | —   | —   | —   | —      | CCP2OUT | PWM7OUT | CWG1B<br>CWG2B<br>CWG3B | SCK1<br>SCK2       | —   | CK1(3)<br>CK2(3) | CLC2OUT | —    | —          | —       | —     |
| —   | —                      | —           | —       | —         | —          | —   | —   | —   | —      | CCP3OUT | —       | CWG1C<br>CWG2C<br>CWG3C | SCL1(3)<br>SCL2(3) | —   | TX1<br>TX2       | CLC3OUT | —    | —          | —       | —     |
| —   | —                      | —           | —       | —         | —          | —   | —   | —   | —      | CCP4OUT | —       | CWG1D<br>CWG2D<br>CWG3D | SDA1(3)<br>SDA2(3) | —   | —                | CLC4OUT | —    | —          | —       | —     |
| —   | —                      | —           | —       | —         | —          | —   | —   | —   | —      | CCP5OUT | —       | —                       | —                  | —   | —                | —       | —    | —          | —       | —     |

**Note:**

1. This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2. All digital output signals shown in these rows are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
3. This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

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