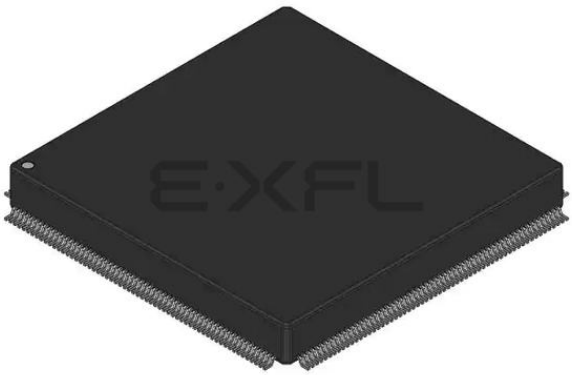

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QMC Supplement to
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If a clock pulse is missing in a given frame N, the counter will fail to reach its end state before the next sync pulse (N+1) arrives, causing that sync pulse to be ignored. When the counter finally reaches its end state, it waits for the next sync pulse (N+2) before resetting. Correct routing is thus resumed in frame (N+2). In the case of an extra clock pulse, the counter reaches its end state too early and resumes synchronized routing upon detecting the next sync pulse (N+1).

Synchronization pulse errors are similar to clock pulse errors. If the frame pulse comes too late, this is similar to having missed a clock pulse in the last time slot. If the frame pulse is too early, it is similar to having one additional clock pulse.

1.9 E1/T1 Frame Description

The primary rate ISDN connections offer a cost-effective, high-speed interface. The physical connections in North America offer 24 connections over a T1 interface; in Europe an E1 (or CEPT) connection gives 32 connections of 64 Kbps each with a time-division-multiplexed architecture.

Time-division-multiplexing (TDM) allows several communication channels to share the same physical media. The data stream of each channel is divided into a number of subpackages. Each channel is then assigned a subdivision of the TDM line called a time slot. This time slot is repeated over time in a regular pattern. A concatenation of the channels' subpackages comprises a frame. The frequency of frame repetition depends on the particular communication interface. Two examples—the T1 line used in North America and the E1 interface used in Europe illustrate TDM.

For both E1 and T1, the frames must be repeated at a frequency of 8 KHz, or every 125 µs. In many applications the required channel speed is 64 Kbps. For example, almost all voice channels use 8-KHz sampling with 8-bit resolution. Each channel in a T1 or E1 interface occupies 8 bits per time slot. The T1 interface multiplexes 24 channels, requiring 24 time slots per frame. In addition to the channels' bits, one more bit, for frame signaling and synchronization, is added to create a frame totaling 193 bits. The resulting T1 physical interface is thus 1.544 Mbps (8 KHz * 193 bits). The E1 frame consists of multiplexing 32 channels resulting in a speed of 2.048 Mbps (8 KHz * 256 bits). These two frames are illustrated in Figure 1-8.

2.4 Channel-Specific Parameters

The channel-specific parameters are located in the lower part of the dual-ported RAM. Each channel occupies 64 bytes of parameters. Physical time slots can be matched to logical channels in several combinations. Unused logical channels leave a hole in the channel-specific parameters that can be used for buffer descriptors for the other SCCs.

The channel-specific area determines the operating mode—HDLC or transparent. Several entries take on different meanings depending on the protocol chosen.

2.4.1 Channel-Specific HDLC Parameters

Table 2-4 describes the channel-specific HDLC parameters. Boldfaced parameters must be initialized by the user.

Table 2-4. Channel-Specific HDLC Parameters

Offset	Name	Width (Bits)	Description
00	**TBASE**	16	Tx buffer descriptor base address—Offset of the channel's transmit buffer descriptor table relative to MCBASE, host-initialized. See Figure 2-2.
02	**CHAMR**	16	Channel mode register. See Section 2.4.1.1, "CHAMR—Channel Mode Register (HDLC)."
04	**TSTATE**	32	Tx internal state —TSTATE defines the internal Tx state. Host-initialized to 0x3800_0000—FC = 8, Motorola mode for MH360. Host-initialized to 0x3000_0000— AT = 0, Motorola mode for 860MH. Initialize before enabling the channel. See Section 2.4.1.2, "TSTATE—Tx Internal State (HDLC)."
08	—	32	Tx internal data pointer—Points to current absolute address of channel.
0C	**TBPTR**	16	Tx buffer descriptor pointer (host-initialized to TBASE before enabling the channel or after a fatal error before reinitializing the channel again)—Offset of current BD relative to MCBASE. See Table 2-1. MCBASE + TBPTR gives the address for the BD in use.
0E	—	16	Tx internal byte count—Number of remaining bytes
10	TUPACK	32	(Tx Temp) Unpack 4 bytes from 1 long word
14	**ZISTATE**	32	Zero-insertion state (host-initialized to 0x0000_0100 for HDLC or transparent operation)—Contains the previous state of the zero-insertion state machine.
18	TCRC	32	Temp transmit CRC—Temp value of CRC calculation result
1C	**INTMSK**	16	Channel's interrupt mask flags—See Section 2.4.1.3, "INTMSK—Interrupt Mask (HDLC)."
1E	BDFlags	16	Temp
20	**RBASE**	16	Rx buffer descriptor offset (host-initialized)— Defines the offset of the channel's receive BD table relative to MCBASE (64-Kbyte table). See Figure 2-2.

Table 2-5 describes the channel mode register's fields for HDLC operation. Boldfaced parameters must be initialized by the user.

Table 2-5. CHAMR Field Descriptions (HDLC)

Field	Name	Description
0	**MODE**	Mode—Each channel has a programmable option whether to use transparent mode or HDLC mode. 0 Transparent mode 1 HDLC mode
1	—	0
2	**IDLM**	Idle mode. 0 Idle mode is disabled. No idle patterns are transmitted between frames. After transmitting the NOF + 1 flags, the transmitter starts the data of the frame. If between frames and the frame buffer is not ready, the transmitter sends flags until it can start transmitting the data. The NOF shall be greater or equal to the PAD setting; see Section 5.2, "Transmit Buffer Descriptor." If NOF = 0, this is identical to flag sharing in HDLC mode. For a high CPM load or with long bus latencies, the QMC protocol may insert additional flags. 1 Idle mode enabled. At least one idle pattern is transmitted between adjacent frames. If between frames and the frame buffer is not ready, the transmitter sends idle characters. When data is ready, the NOF + 1 flags are sent followed by the data frame. If in IDLE mode and NOF = 1, the following sequence is transmitted: .....init value, FF, FF, flag, flag, data,..... The init value before the idle will be 1's, in this case it is assumed the transmitter was uninitialized. An uninitialized SCC transmits 1s in every position.
3	**ENT**	Enable transmit. 0 Disable transmitter. If this bit is cleared and the channel's transmitter is routed to a certain time slot (within TSATTx, see Figure 2-3) the transmitter sends 1's on this time slot. 1 The transmit portion of the channel is enabled and data is sent according to protocol and to other control settings. Note that there is no ENR bit in the QMC protocol. To enable the receiver, the ZDSTATE and RSTATE parameters shall be set to their initial values.
4–6	—	Reserved
7	**POL**	Enable polling. This bit enables the transmitter to poll the transmit buffer descriptors. 0 The CPM does not check the ready bit (R) in the transmit buffer descriptor. 1 The CPM checks the ready bit (R) in the transmit buffer descriptor. The user can use this bit to prevent unnecessary external bus cycles when checking the ready bit (R) in the buffer descriptor. This bit should always be set by the software at the beginning of a transmit sequence of one or more frames. This bit is cleared (0) by the RISC processor when no more buffers are ready in the transmit queue when it finds a buffer descriptor with the R bit cleared (0), i. e., at the end of a frame or at the end of a multiframe transmission. In order to prevent deadlock the software should always prepare the new BD, or multiple BDs, and set (1) the ready bit in the BD, before setting (1) the POL bit. Note that as this bit is automatically cleared by the CPM; the user should not attempt to clear this bit in software.
8	**CRC**	This bit selects the type of CRC when using the HDLC channel mode. 0 16-bit CCITT-CRC is selected for this channel. 1 32-bit CCITT-CRC is selected.
9	—	0

For the 860MH, RSTATE should be initialized to 0x3100_0000 before enabling the channel —AT = 1. Note that for the 860MH, bit 4 should always be zero as only bits 5–7 map to AT[1–3]. Table 2-15 describes the RSTATE fields for the 860MH with boldfaced parameters to be initialized by the user.

Table 2-15. RSTATE Field Descriptions for 860MH (Transparent Mode)

Field	Name	Description
0–1	—	0
2	—	1
3	**MOT**	Motorola/Intel bit 0 = The bus format is Intel format (little-endian). 1 = The system bus is considered to be organized in Motorola format (big-endian).
4	—	0
5–7	**AT[1–3]**	Address type—This field contains the address type for the transmitter DMA channel for data buffers in external memory (transmit buffers). Address types are needed by the memory controller to decode a correct memory cycle and activate the correct handshaking.

0	1	2	3	4	5	6	7
				IQOV	GINT	GUN	GOV

Note: For the 68360, the bit numbering is reversed. See Appendix A for more information.

Figure 4-3. SCCM Register

4.3 Interrupt Table Entry

The interrupt table contains information about channel-specific events. Its flags are shown in Figure 4-4. Note that some bits have no meaning when operating in transparent mode. For more detailed description on which bits are used in HDLC and transparent operation, refer to Section 2.4, “Channel-Specific Parameters.” Table 4-2 describes the fields of an interrupt table entry.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
V	W	NID	IDL	—	CHANNEL NUMBER					MRF	UN	RXF	BSY	TXB	RXB
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: For the 68360, the bit numbering is reversed. See Appendix A for more information.

Figure 4-4. Interrupt Table Entry

Table 4-2. Interrupt Table Entry Field Descriptions

Field	Name	Description
0	V	Valid bit 0 = Entry is not valid. 1 = Valid entry containing interrupt information. Upon generating a new entry, the RISC processor sets this bit. The V bit is cleared by the host immediately after it reads the interrupt flags in this entry (before processing the interrupt). The V bits in the queue are host-initialized. During the initialization procedure, the host must clear those bits in all queue entries.
1	W	Wrap bit 0 = This is not the last entry in the circular interrupt table. 1 = This is the last circular interrupt table entry. The next event’s entry is written/read (by RISC/host) from the address contained in INTBASE. During initialization, the host must clear all W bits in the queue except the last one which must be set. The length of the queue is left to the user and can be a maximum of 64 Kbytes.
2	NID	Not idle 0 = No NID event has occurred. 1 = A pattern which is not an idle pattern was identified. NID interrupts are not generated in transparent mode.

Table 4-2. Interrupt Table Entry Field Descriptions (Continued)

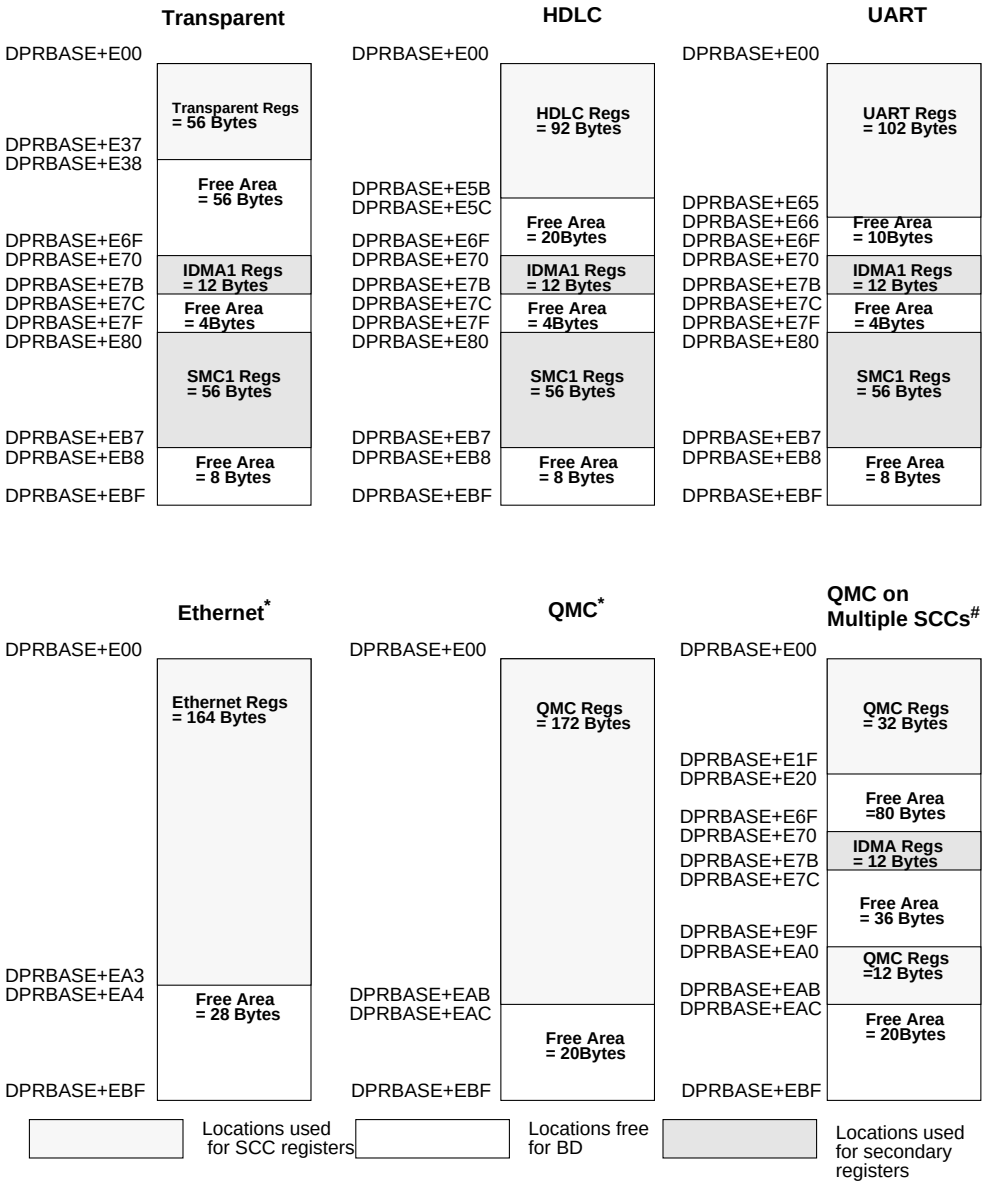
Field	Name	Description
3	IDL	Idle 0 = No IDL event has occurred. 1 = The channel's receiver has identified the first occurrence of HDLC idle (FFFE) after any non-idle pattern. IDL interrupts are not generated in transparent mode.
4		Reserved
5–9	Channel Number	This 5-bit field identifies the requesting logical channel index (0–31).
10	MRF	Maximum receive frame length violation—This interrupt occurs in HDLC mode when more than MFLR number bytes are received. As soon as MFLR is exceeded, this interrupt is generated and the remainder of the frame is discarded. At this point the receive buffer is not closed and the reception process continues. The receive buffer is closed upon detecting a flag. The length field written to this buffer descriptor is the entire number of bytes received between the two flags. MRF interrupts are not generated in transparent mode. **Note**: The MRF interrupt is generated directly when the MFLR value is a multiple of 4 bytes. The checking of this is done on a long-word boundary whenever the SDMA transfers 32 bits to memory. If MFLR is not aligned to 4x bytes, this interrupt may be 1- to 3-byte timings late for this channel. In any case, the violation can be checked to any number of bytes. The last entry in the data buffer is always a full long word.
11	UN	Tx no data 0 = No UN event has occurred. 1 = There is no valid data to send to the transmitter. The transmitter sends an abort indication consisting of 16 consecutive 1's and then sends idles or flags according to the protocol and the channel mode register setting. This error occurs when a transmit channel has no data buffer ready for a multibuffer transmission already in progress. Transmission of a frame is a continuous bitstream without gaps or interruption. When a buffer is not ready in the middle of this sequence, it is an error situation. This can be viewed as channel underrun. The transmitter for this channel is stopped. See Section 6.3, "Restarting the Transmitter," for recovery information.
12	RXF	Rx frame 0 = No RXF event has occurred. 1 = A complete HDLC frame is received. Data is stored in external memory and the buffer descriptor is updated. If during frame reception an abort sequence of at least seven 1's is detected, the buffer is closed and both RXB and RXF are reported along with the AB in the buffer descriptor. As a result of end-of-frame, the global frame counter GRFCNT is decremented for interrupt generation. This counter is decremented on RXF only, regardless if the RXF was caused by correct closing or due to an error. RXF interrupts are not generated in transparent mode.
13	BSY	Busy 0 = No BSY event has occurred. 1 = A frame was received but was discarded due to lack of buffers. This can be viewed as channel overrun. After a busy condition, the receiver for this channel is disabled and no more data is transferred to memory. Receiver restart is described in Section 6.4, "Restarting the Receiver."

Table 4-2. Interrupt Table Entry Field Descriptions (Continued)

Field	Name	Description
14	TXB	Tx buffer 0 = No TXB event has occurred. 1 = A buffer has been completely transmitted. This bit is set (and an interrupt request is generated) as soon as the programmed number of PAD characters (or the closing flag, for PAD = 0) is written to the SCC's transmit FIFO. The number of PAD characters determines the timing of the TXB interrupt in relation to the closing flag sent out at TXD. See Chapter 5, “Buffer Descriptors,” for an explanation of PAD characters and their use.
15	RXB	Rx buffer 0 = No RXB event has occurred. 1 = A buffer has been received on this channel.

4.4 Channel Interrupt Processing Flow

Figure 4-5 illustrates the flow of a channel interrupt. Note that this does not describe the processing of the global interrupts GUN and GOV.



 # - TSATRx & TSATTx are mapped to an alternative SCC's parameter RAM, SMC1 is not available in this configuration due to memory conflict.

*** - SMC1 and IDMA1 not available in these configurations due to memory conflict.**

Figure 5-9. MC68MH360 SCC3 Parameter RAM Usage

If the QMC operates with a full 64 channels, no space is left in the lower 4-Kbyte area. In this case, the only free areas are in the RAM pages, each 256-bytes large. Depending on the functions, channels and protocols used, some areas remain free for buffer descriptors. Also, if a particular function is not enabled, its parameter RAM area may also be used.

If fewer than 64 logical channels are used or if physical channels are concatenated to super channels, space is freed in the dual-ported RAM. Each unused logical channel creates a 64-byte hole in the dual-ported RAM. This area is free for buffer descriptors for any SCC. QMC channels can also use this space instead of external memory for buffer descriptors, reducing the load on the external bus.

Figure 5-11 shows the internal memory map for the MPC860MH. Figure 5-12 to Figure 5-15 show a more detailed memory map for each SCC, showing the parameter RAM usage for different functions.

- RAM page one is dedicated to SCC1, I^2C, IDMA1 and for miscellaneous storage.
- RAM page two is dedicated for SCC2, SPI, IDMA2 and RISC timers
- RAM page three is dedicated for SCC3, SMC1 and DSP1 operations.
- RAM page four is dedicated for SCC4, SMC2 and DSP2 operations.

Table 5-4 shows the functions available for various protocols on each SCC for the MPC860MH.

Table 5-4. MPC860MH Functions Available

	Function Available?	Transparent	HDLC	UART	Ethernet	QMC	Shared QMC
SCC1	Yes	Misc, I^2C, IDMA1	Misc, I^2C, IDMA1	Misc, I^2C, IDMA1	Misc, IDMA1	Misc, IDMA1	Misc, IDMA1
	No				I^2C	I^2C	I^2C
SCC2	Yes	SPI, Timer, IDMA2	SPI, Timer, IDMA2	SPI, Timer, IDMA2	Timer, IDMA2	Timer, IDMA2	Timer, IDMA2
	No				SPI	SPI	SPI
SCC3	Yes	SMC1, DSP1	SMC1, DSP1	SMC1, DSP1	DSP1	DSP1	DSP1
	No				SMC1	SMC1	SMC1
SCC4	Yes	SMC2, DSP2	SMC2, DSP2	SMC2, DSP2	DSP2	DSP2	DSP2
	No				SMC2	SMC2	SMC2

Figure 5-12 to Figure 5-15 show that not all the functions available on each SCC can be used simultaneously due to overlaps of the register locations stored in the parameter RAM.

```
struct  descs {
      rxbdq recvbd0;               /* receive buffer 0 */
      txbdq xmitbd0;               /* transmit buffer 0 */
      } chbd[4];                   /* 4 sets of chan descriptors */
static char *poem[6];              /* poem area */
short linecntr;                    /* line counter */
struct intrpten {
      unsigned V:1;                /* entry valid bit */
      unsigned W:1;                /* entry wrap bit */
      unsigned NID:1;              /* not-an-idle has occurred */
      unsigned IDL:1;              /* an idle has occurred */
      unsigned :1;
      unsigned CHNMBR:5;           /* channel number */
      unsigned MRF:1;              /* maximum frame length violation */
      unsigned UN:1;               /* Tx underrun */
      unsigned RXF:1;              /* receive frame */
      unsigned BSY:1;              /* frame discarded, no buffers */
      unsigned TXB:1;              /* buffer transmitted */
      unsigned RXB:1;              /* receive buffer closed */
      }  intrpt[10];               /* interrupt table */
short recvcnt,xmitcnt,othrcnt = 0;  /* interrupt counters */

main()
{
      void SCC1esr();              /* exception service rtn */
      int *pvec;                   /* exception vector pntr */
      char vecblk = 3;             /* vector number block */
      char intlvl = 4;             /* interrupt level */
      pdpr = (struct dprbase *) (getmbar() & 0xFFFFE000);/*  init  dual-ported
      RAM ptr */
      pdpr->CICR.VBA2_VBA0 = (unsigned) (vecblk);/* vecs at vec num 0x60-7F */
      pdpr->CICR.IRL2_IRL0 = (unsigned) (intlvl);/* CPM interrupts level 4 */
      pdpr->CICR.HP4_HP0 = 0x1F;    /* no int priority change */
/* SCdP is zero from reset */
      pdpr->CICR.SCcP = 1;         /* SCC2 to SCCC position */
      pdpr->CICR.SCbP = 2;         /* SCC3 to SCCB position */
      pdpr->CICR.SCaP = 3;         /* SCC4 to SCCA position */
```

Table 8-1. Common QMC Configurations (Continued)

Protocols Selected	Frequency Supported			
	25 MHz	33 MHz	40 MHz	50 MHz
SCC1: 10-Mbps Ethernet; SCC2: 16 x 64-Kbps QMC; SCC3: 16 x 64-Kbps QMC; SCC4: 64-Kbps HDLC. TDM bit rate = 2.048 Mbps	No	Yes	Yes	Yes
SCC1: 10-Mbps Ethernet; SCC2: 12 x 64-Kbps QMC; SCC3: 12 x 64-Kbps QMC; SCC4: 64-Kbps HDLC. TDM bit rate = 1.544 Mbps	No	Yes	Yes	Yes
SCC1: 24-channel QMC; SCC2: 24-channel QMC. Serial bit rate 2 x 1.544 Mbps — 2 x T1	No	No	Yes	Yes
SCC1: 10-Mbps Ethernet SCC2: 24-channel QMC; SCC3: 24 Channel QMC. Serial bit rate 2 x 1.544 Mbps — 2 x T1	No	No	No	Yes
SCC1: 32-channel QMC; SCC2: 32-channel QMC. Serial bit rate 2 x 2.048 Mbps (E1/CEPT)	No	No	No	Yes

8.2 CPM Loading

This section primarily deals with the CPM loading of the MH360 and 860MH. As the CPM architecture is identical on both devices, the performance for a given clock frequency is identical. Compared to standard protocols, the QMC protocol places more demands on the CPM RISC because it requires the CPM to handle all of the bit manipulation normally implemented with hardware support built into the SCCs.

The SCC operates transparently in QMC mode. The SCC's main function is serial-to-parallel conversion of the data stream out of the time slot assigner, and parallel-to-serial conversion of the data stream gated into the time slot assigner. All bit manipulating is done in the CPM RISC software or hardware. Thus, the CPM has a much higher load when operating in QMC mode, even if all time slots are concatenated to one logical channel. This loading is reflected in the measured performance.

Table 8-2 gives loading guidelines. The table assumes a single SCC running at 100% of the CPM bandwidth. For each protocol supported, the table gives the ratio of the SCC bit rate versus clock frequency, and the maximum serial throughput at standard frequencies.

Table 8-2. CPM Performance Table

Protocol	SCC Rate: Clock Frequency Mbps: MHz	Maximum Serial Throughput			
		25 MHz Mbps	33 MHz Mbps	40 MHz Mbps	50 MHz Mbps
Transparent	1 : 3.125 FD	8	10.56	12.8	16
HDLC	1 : 3.125 FD	8	10.56	12.8	16
UART	1 : 10.4 FD	2.4	3.168	3.84	4.8

Chapter 9
Multi-Subchannel (MSC) Microcode

The RISC processor in the PowerQUICC has an option to execute microcode from the internal dual-ported RAM. Motorola uses this feature to enhance existing protocols or implement additional protocols. Customers can purchase RAM microcodes in an object-code format and download it to the PowerQUICC dual-ported RAM during system initialization.

The RAM microcode is provided by Motorola as a set of S records that can be downloaded directly to an application development system or stored in a system EPROM; for more information on S records, see Appendix C of the *M68000 Family Programmer's Reference Manual*. After system reset, the binary of the microcode should be copied to the dual-ported RAM. The QUICC registers, including the RISC controller configuration register (RCCR), should be initialized as specified in the microcode RAM documentation. Before the RISC is used in the system, the user should issue a reset command to the communications processor command register (CR). The microcode RAM functions are available in addition to all protocols available in the standard QUICC microcode ROM.

9.1 MSC Microcode Features

The multi-subchannel (MSC) microcode is a downloadable microcode for the MPC860MH and has the following key features:

- General
  - Multiple subchannels within a single 8-bit time slot
  - Bit resolution for subchannels
  - Up to 32 independent communications channels for both Rx and Tx
  - Supports either transparent or HDLC protocols per subchannel
- Performance
  - 32 channels + 10-Mbps ethernet support at 40-MHz system clock

Using on-chip time slot assigners, the S/T and U interfaces in IDL2 mode can match the QMC bus structure—both interfaces can be connected to a 2.048-MHz IDL2 bus and route the B1 channel, B2 channel and D channel to any time slot.

Figure C-1 shows the IDL2 bus configured to match the QMC protocol.

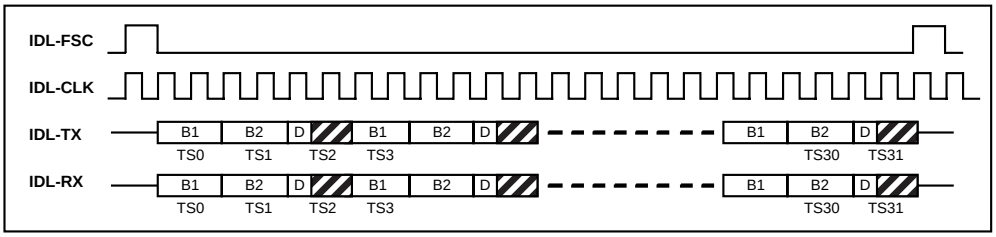


Figure C-1. IDL2 Bus Structure for a Connection to the QMC Bus

C.2 Control and Status Information

Using the SPI port, the QUICC32 and the ISDN interfaces exchange control and status information via out-of-band signaling. Optionally, the MC145572s could use an 8-bit parallel port for control and status transfer, allowing the U interfaces to be connected to the processor bus.

Figure C-2 shows the connection between the QUICC32 and an S/T interface.

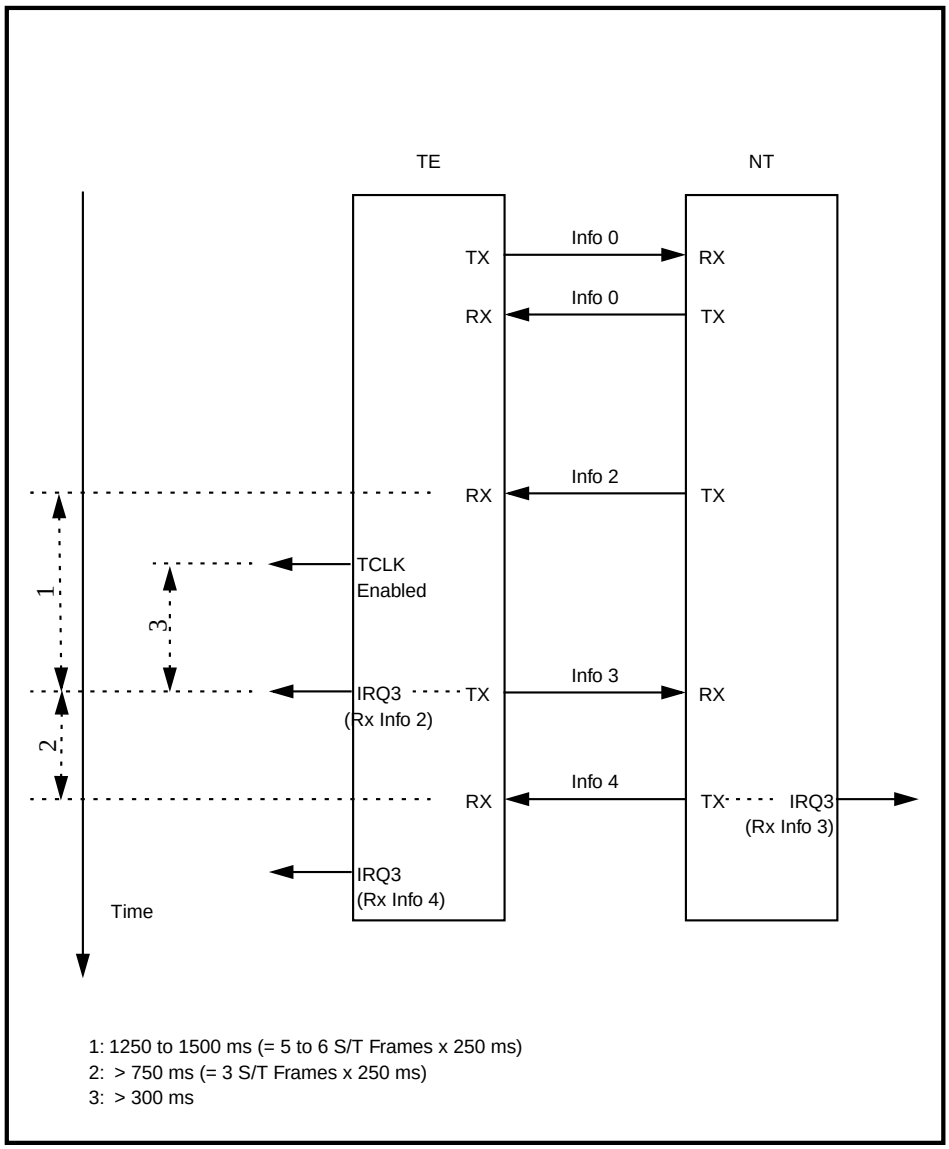


Figure C-7. Timing Diagram for an Activation Initiated by the NT

C.3.1.2 Deactivation Procedure

When the clock-master S/T interface is deactivated, the QUICC32 receives an interrupt indicating the deactivation status (IRQ3 —register NR3 bit 3— meaning Info 0 of Figure C-9 has been received). Then, if another S/T interface is active, its TCLK signal must be selected to become the clock master; otherwise, the QUICC32 can select the BRG to be the clock master.

As shown in Figure C-9, the TCLK signal is disabled about 72.8 µs after the interruption. Therefore, the QUICC32 has 72.8 µs to react to the IRQ and to select another clock master.

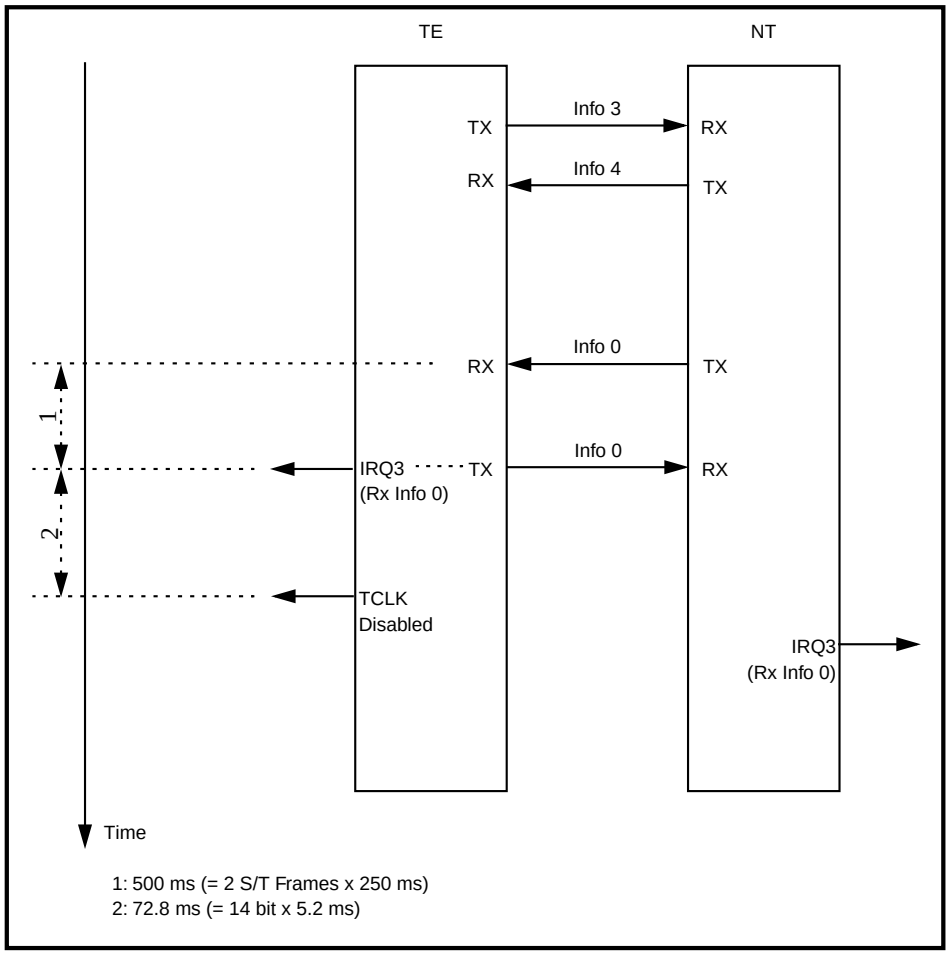


Figure C-9. Timing Diagram for a Deactivation (Always Initiated by the NT)

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