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Co-Processors/DSP	Communications; CPM
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Graphics Acceleration	No
Display & Interface Controllers	-
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Chapter 2
QMC Memory Organization

This section describes the operation specific to the QMC protocol. When not running the QMC protocol, SCCs operate as described in the MC68360 and MPC860 user's manuals.

Figure 2-1 shows the dual-ported RAM structure for the MC68MH360 and the MPC860MH. The MC68MH360 and the MPC860MH have similar functionality but are organized in a different manner.

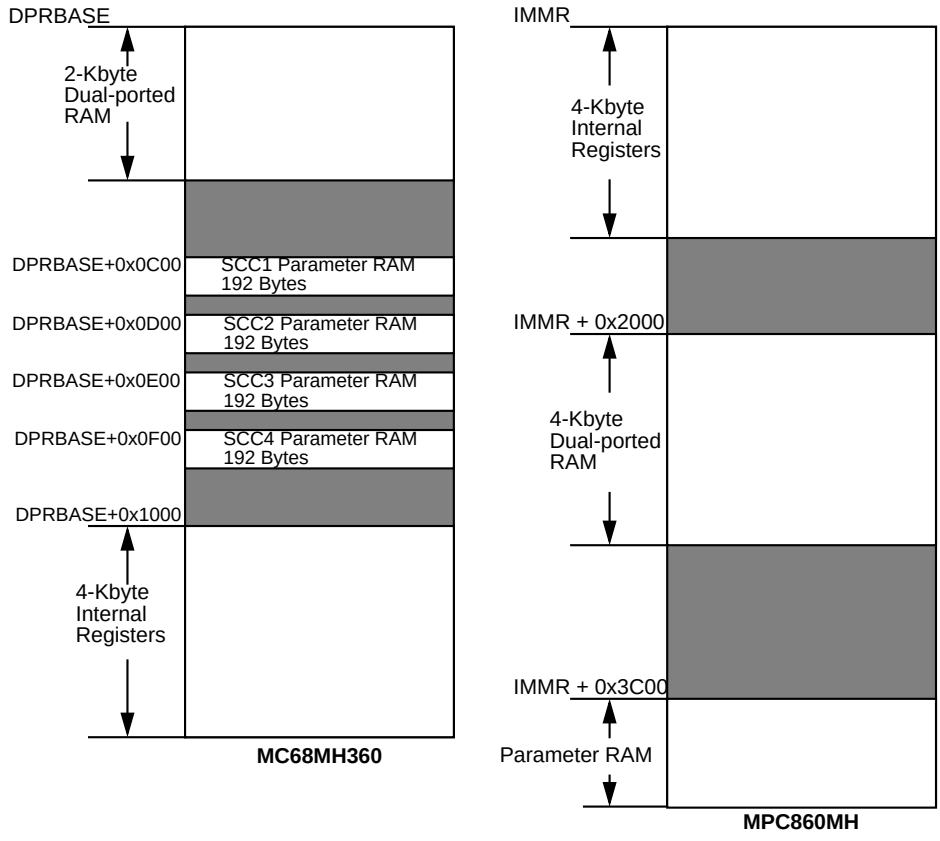


Figure 2-1. MC68MH360 and MPC860MH Internal Memory Structures

Table 2-2 describes the fields in the time slot assignment table for receive.

Table 2-2. Time Slot Assignment Table Entry Fields for Receive Section

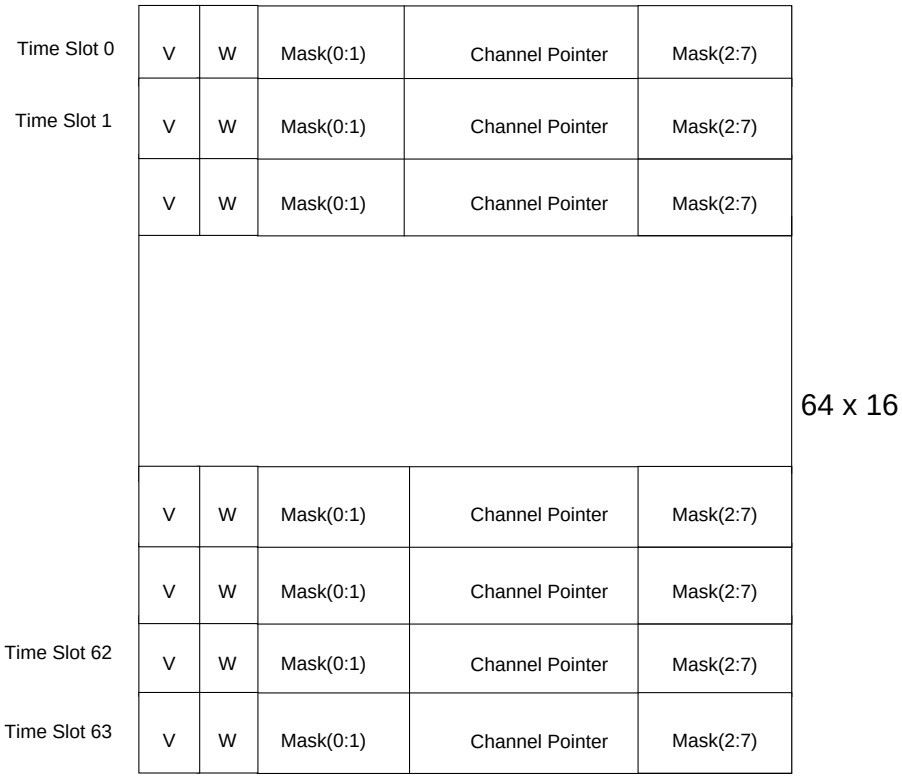
Field	Description
V	Valid bit—The valid bit indicates whether this time slot is valid. 0 The data in this 8-bit time slot is totally ignored and not written to any buffer. 1 The data in this 8-bit time slot is valid and written to the current buffer, pointed to by the channel pointer entry, after protocol processing (e.g. zero deletion in HDLC). Individual bits can be masked out as described later.
W	Wrap bit—Identifies the last entry in TSATRx. 0 This is not the last time slot in the frame. 1 The RISC processor wraps around and handles time slot 0 or the first 8 bits transferred from the TSA in the next request. The next request is identified by a frame synchronization pulse.
Rx channel pointer	This 6-bit field of the TSATRx entry identifies the data channel routed to this time slot. The actual channel pointer is 12 bits long, and contains the starting address of the channel-specific parameter area (address of RBASE). The 6 most-significant bits are taken from the TSATRx channel pointer field, and the 6 least-significant bits are always internally set to zero. For the MH360, the most-significant bit must be set to zero, as the addressing range is 2 Kbytes.
Mask(0–7)	Mask bits—These 8 bits identify the valid bits in this time slot for subchanneling support. For 8-bit resolution, all mask bits should be set to 1. Any unmasked bit (1) is processed in the receiver for a valid time slot. Any masked bit (0) is ignored by the receiver for a valid channel and no bit counter is affected.

Table 2-3 describes the fields in the time slot assignment table for transmit.

Table 2-3. Time Slot Assignment Table Entry Fields for Transmit Section

Name	Description
V	Valid bit—The valid bit indicates whether this time slot is valid. 0 Logic 1 is transmitted. If the Tx signal of the TDM interface is programmed to be an open drain output (port B programming), other devices can transmit on nonvalid time slots. 1 Data is transmitted from its associated buffer in combination with the mask bit settings.
W	Wrap bit—The wrap bit identifies the last entry in TSATTx. 0 This is not the last time slot in the frame. 1 The RISC processor wraps around and handles time slot 0 or the first 8 bits of data in the SCC in the next request. The next request is identified by a frame synchronization pulse.
Tx channel pointer	This 6-bit field of the TSATTx entry identifies the data channel routed to this time slot. The actual channel pointer is 12 bits long, and contains the starting address of the channel-specific parameter area (address of TBASE). The 6 most-significant bits are taken from the TSATTx channel pointer field, and the 6 least-significant bits are always internally set to zero. For the MH360 the most-significant bit must be set to zero, as the addressing range is 2 Kbytes.
Mask(0–7)	Mask bits—Identifies the valid bits in this time slot for subchanneling support. For 8-bit resolution, all mask bits should be set to 1. For a valid channel with an unmasked bit (1), the bit position is filled according to the protocol. A valid channel with a masked bit (0) transmits a logic high (1).

If the transmitter and receiver have the same mapping then it is possible to use a common time slot assignment table. This is initialized by setting both Tx_S_PTR and Rx_S_PTR to SCC Base + 20. For 64-channel support it is suggested to use common Rx and Tx parameters. The time slot assignment table will then also be common and have 64 entries starting at SCC Base + 20; see Figure 2-4.



Note: For the 68360, the bit numbering is reversed. See Appendix A for more information.

Figure 2-4. Time Slot Assignment Table for 64-Channel Common Rx and Tx Mapping

2.3 Multiple SCC Assignment Tables

Assume a scenario as depicted in Figure 2-5. A 2.048-Mbps TDM link is fed directly into the TSA. Within the SI RAM, the even channels (byte-wide) are muxed to SCC3 and the odd channels are muxed to SCC2. This arrangement is used to spread the load over two SCCs. This effectively doubles the FIFO depth on the QMC protocol. Time slots are switched to alternate SCCs to avoid data bursts that may stress the FIFOs. Each SCC sees a continuous bitstream without any gaps as described earlier.

Table 2-4. Channel-Specific HDLC Parameters (Continued)

Offset	Name	Width (Bits)	Description
22	**MFLR**	16	Maximum frame length register (host-initialized)—Defines the longest expectable frame for this channel. Its maximum value is 64 Kbytes. The remainder of a frame which is larger than MFLR is discarded and a flag in the last frame's BD is set (LG). An interrupt request (RXF and RXB) might be generated depending on the interrupt mask. The frame length is considered to be everything between flags, including CRC. MFLR is checked every long word, but the content may be on any number of bytes. If MFLR is set to 5 for example, checking is done when 8 bytes have been received. At this point, the SDMA transfers the long word to memory, and all 8 bytes will be in the receive buffer. Also at this point the MFLR violation (>5) is detected and the interrupt may be generated. No more data will be written into this buffer when the MFLR violation is detected.
24	**RSTATE**	32	Rx internal state —Initialize to 0x3900_0000 FC=9, Motorola mode for MH360 or initialize to 0x3100_0000 AT=1, Motorola mode for 860MH. See Section 2.4.1.4, "RSTATE—Rx Internal State (HDLC)," for more information.
28	—	32	Rx internal data pointer—Points to current address of specific channel.
2C	**RBPTR**	16	Rx buffer descriptor pointer (host-initialized to RBASE prior to operation or due to a fatal error)—Contains the offset from MCBASE to the current receive buffer. See Table 2-1. MCBASE + RBPTR gives the address for the BD in use.
2E	—	16	Rx internal byte count—Per Channel: Number of remaining bytes in buffer
30	RPACK	32	(Rx Temp) Packs 4 bytes to 1 long word before writing to buffer.
34	**ZDSTATE**	32	Zero deletion machine state—(Host-initialized to 0x0000_0080 in HDLC mode, 0x1800_0080 in transparent mode, prior to operation and after a fatal Rx error (global overrun, busy) before channel initialization.)—Contains the previous state of zero deletion state machine. The middle 2 bytes, represented by zeros in the initialization value above, hold the received pattern during reception. A window of 16 bits shows the history of what is received on this logical channel. More information is given in the application note section.
38	RCRC	32	Temp receive CRC—Temp value of CRC calculation result
3C	MAX_cnt	16	Max_length counter—Count length remaining
3E	TMP_MB	16	Temp—Holds MIN(MAX_cnt, Rx internal byte count)

2.4.1.1 CHAMR—Channel Mode Register (HDLC)

The channel mode register is a word-length, host-initialized register. Figure 2-7 shows the channel mode register for HDLC operation.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MODE	0	IDLM	ENT	RESERVED			POL	CRC	0	RESERVED		NOF			
Reset: 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Notes: 1. All bits that are defined as reserved should be cleared (0).
2. For the 68360, the bit numbering is reversed. See Appendix A for more information.

Figure 2-7. CHAMR—Channel Mode Register (HDLC)

Table 2-10. Channel-Specific Transparent Parameters (Continued)

Offset	Name	Width	Description
22	**TMRBLR**	16	Transparent maximum receive buffer length (host-initialized entry)—Defines the maximum number of bytes written to a receive buffer before moving to the next buffer for this channel. Note that this value must be a multiple of 4 bytes as the QMC works on long-word alignment.
24	**RSTATE**	32	Rx internal state —Initialize to 0x3900_0000 FC = 9, Motorola mode for MH360, initialize to 0x3100_0000 AT = 1, Motorola mode for 860MH. See Section 2.4.2.5, “RSTATE—Rx Internal State (Transparent Mode),” for more information.
28		32	Rx internal data pointer—Points to current address of specific channel.
2C	**RBPTR**	16	Rx buffer descriptor pointer (host-initialized to RBASE, prior to operation or due to a fatal error)—Contains the offset from MCBASE to the current receive buffer. See Figure 2-2. MCBASE + RBPTR gives the address for the BD in use.
2E		16	Rx internal byte count—Per Channel: Number of remaining bytes in buffer
30	RPACK	32	(Rx temp)—Packs 4 bytes to 1 long word before writing to buffer.
34	**ZDSTATE**	32	Zero deletion machine state—(Host-initialized to 0x0000_0080 in HDLC mode, 0x1800_0080 in transparent mode, prior to operation and after a fatal Rx error (global overrun, busy) before channel initialization.)—Contains the previous state of the zero-deletion state machine. The middle 2 bytes, represented by zeros in the initialization value above, holds the received pattern during reception. A window of 16 bits shows the history of what is received on this logical channel.
38	RES	32	
3C	**TRNSYNC**	16	Transparent synchronization—In transparent mode, this register controls synchronization for single time slots or superchannel applications. See Section 2.4.2.4, “TRNSYNC—Transparent Synchronization.”
3E	RES	16	

2.4.2.1 CHAMR—Channel Mode Register (Transparent Mode)

The channel mode register is a word-length, host-initialized register. Figure 2-11 shows the channel mode register for transparent mode.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MODE	RD	1	ENT	RES'D	SYNC	RES	POL	0	0	RESERVED		0			
Reset: 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Notes: 1. All bits defined as reserved are cleared (0).
2. For the 68360, the bit numbering is reversed. See Appendix A for more information.

Figure 2-11. CHAMR—Channel Mode Register (Transparent Mode)

Table 2-11 describes the channel mode register’s fields for transparent operation. Boldfaced parameters must be initialized by the user.

2.4.2.3 INTMSK—Interrupt Mask (Transparent Mode)

Each event defined in the interrupt circular queue entry maps directly to a bit in INTMSK as shown in Figure 2-13. There is one mask bit for each event—UN (bit 11), BSY (bit 13), TXB (bit 14) and RXB (bit 15). Bits that do not map to an event are reserved. Reserved bits must be set to zero.

- 0 = No interrupt request is generated and no new entry is written in the circular interrupt table.
- 1 = Interrupts are enabled.

This register is initialized by the host before operation.

INTERRUPT TABLE ENTRY:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
V	W	RES	RES	–	CHANNEL NUMBER					RES	UN	RES	BSY	TXB	RXB
RESET: 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

INTMSK:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RESERVED		RESERVED		RESERVED						RES	INTERRUPT MASK BITS				
Reset: 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: For the 68360, the bit numbering is reversed. See Appendix A for more information.

Figure 2-13. INTMSK and Interrupt Table Entry (Transparent Mode)

2.4.2.4 TRNSYNC—Transparent Synchronization

In transparent mode, the TRNSYNC register controls the synchronization for single time slots or superchannel applications.

Note

This register has no meaning if the SYNC bit in the channel mode register (CHAMR) is cleared (0).

When sending a transparent message over several time slots, it is necessary to know in which time slot the first byte of data appears.

The TRNSYNC word-length register is divided into two parts with the high byte controlling the first received time slot and the low byte controlling the transmitter synchronization.

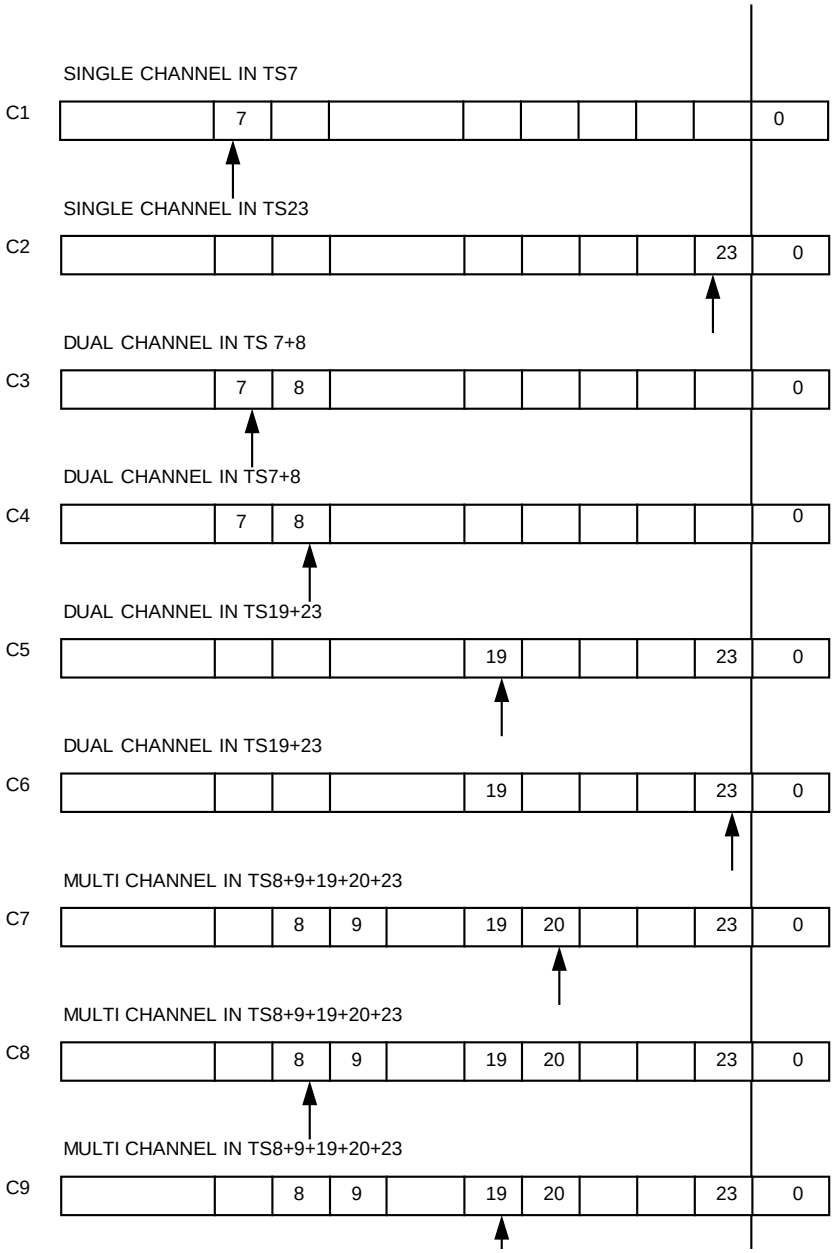


Figure 2-14. Examples of Different T1 Time Slot Allocation

Following a request that is not masked out by the INTMASK or the SCCM (SCC mask) register, an interrupt is generated to the host. The host reads the SCCE to determine the cause of interrupt. A dedicated SCCE bit (GINT) indicates that at least one new entry was added to the queue. After clearing GINT, the host starts processing the queue. The host then clears this entry's valid bit (V). The host follows this procedure until it reaches an entry with V = 0, indicating an invalid entry.

NOTE

It is important that the user clear all interrupt flags in a queue entry even though its valid bit may be cleared since old flags are not necessarily overwritten with each new event.

4.1 Global Error Events

A global error affects the operation of the SCC. A global error can occur for two reasons—serial data rates being too high for the CPM to handle, and CPM bus latency being too long for correct FIFO operation.

There are two global errors— global transmitting underrun (GUN) and global receiver overrun (GOV). GUN indicates that transmission has failed due to lack of data; and GOV indicates that the receiver has failed because the RISC processor did not write previous data to the receive buffer. In both cases, it is unknown which channel(s) are affected.

Nonglobal, individual channel errors are handled differently. See Section 4.3, "Interrupt Table Entry," for underrun and overrun in a specific channel.

The incoming data to the CPM is governed by transfers between the SCC and the SI. Every transfer in either direction causes a request to the CPM state machine. If requests are received too quickly, the CPM crashes due to an overload of serial data. This causes a global error depending on whether it happened in the transmit side or the receive side. This error affects all QMC channels.

The other error condition is bus latency. A receiving channel submits data to the FIFO for transfer to external memory as long as the channel operates normally. If the bus latency for the SDMA channels is too long and the receive FIFO is filled and overwritten, a receiver overflow occurs. The overwriting channels cannot be traced, affecting entire QMC operation.

A similar situation can occur during transmission when the SDMA cannot fill the FIFO from external memory because of bus latency. Again, it cannot be determined which channel is underrun, and the whole QMC operation is affected.

Global errors are unlikely to occur in normal system operation, if correct serial speed is used. The only area of concern is data movement between the FIFO and external memory. To avoid problems, the user must understand the bus arbitration mechanism of the QUICC and meet the latency requirements; see Chapter 8, "Performance," for more information.

Table 5-2. Transmit Buffer Descriptor (TxBD) Field Descriptions (Continued)

Field	Name	Description
6	**CM**	Continuous mode 0 Normal operation. 1 The R bit is not cleared by the CPM after this buffer descriptor is closed, allowing the associated data buffer to be retransmitted automatically when the CPM next accesses this buffer descriptor.
7	—	—
8	**UB**	User bit—The CPM never touches, sets, or clears this user-defined bit. The user determines how this bit is used. For example, it can be used to signal between higher-level protocols whether a buffer has been processed by the CPU.
9–11	—	—
12–15	**PAD**	Padding bits—These four bits indicate the number of PAD characters (0x7E or 0xFF depending on IDLM mode in the CHAMR register) that the transmitter sends after the closing flag. The transmitter issues a TXB interrupt only after sending the programmed value of pads to the Tx FIFO. The user can use the PAD value to guarantee that a TXB interrupt occurs after the closing flag has been sent on the TXD line. PAD = 0 means the TXB interrupt is issued immediately after sending the closing flag to the Tx FIFO. The number of PAD characters depends on the FIFO size and the number of time slots in use. An example explains the calculation: In SCC1 the FIFO is 32 bytes. If 16 time slots are used in the link, the resulting number of PAD characters is 32/16 = 2, to append to this buffer to ensure that the TXB interrupt is not given before the closing flag has been transmitted through the TXD line. The number of PAD characters must not exceed the NOF characters, ensuring that the closing of one buffer (the interrupt generation) occurs before the start of the next frame (clearing of R-bit). After the sequence of a closing flag followed by (PAD + 1) flag characters, a TXB interrupt will be generated; see Figure 5-4.
16–31	**DL**	Data length—The data length is the number of bytes the CPM should transmit from this buffer descriptor's data buffer. It is never modified by the CPM. This field should be greater than zero.
32–63	**TxBP**	Tx buffer pointer—The transmit buffer pointer, which contains the address of the associated data buffer, may be even or odd. The buffer may reside in either internal or external memory. This value is never modified by the CPM.

Figure 5-4 shows a TXB interrupt generated after (PAD + 1) flag characters following the closing flag. Four flags (NOF = 3) precede the next data. To set up this sequence correctly, the PAD value must not exceed NOF.

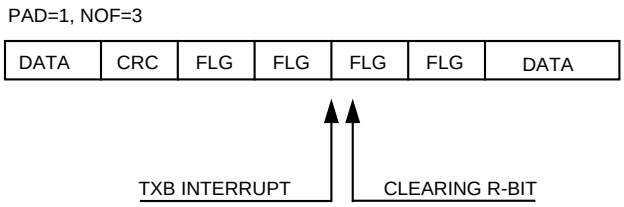
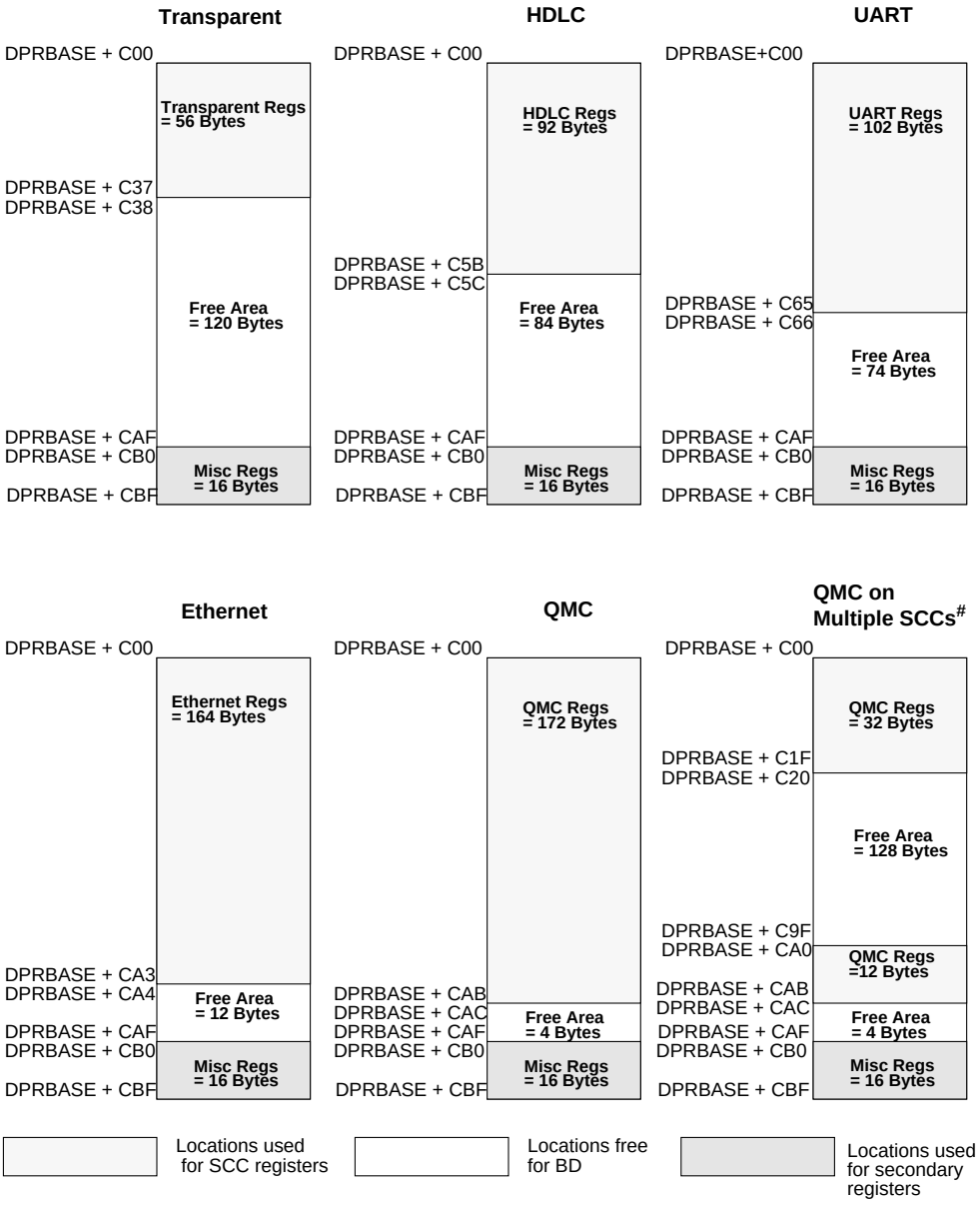
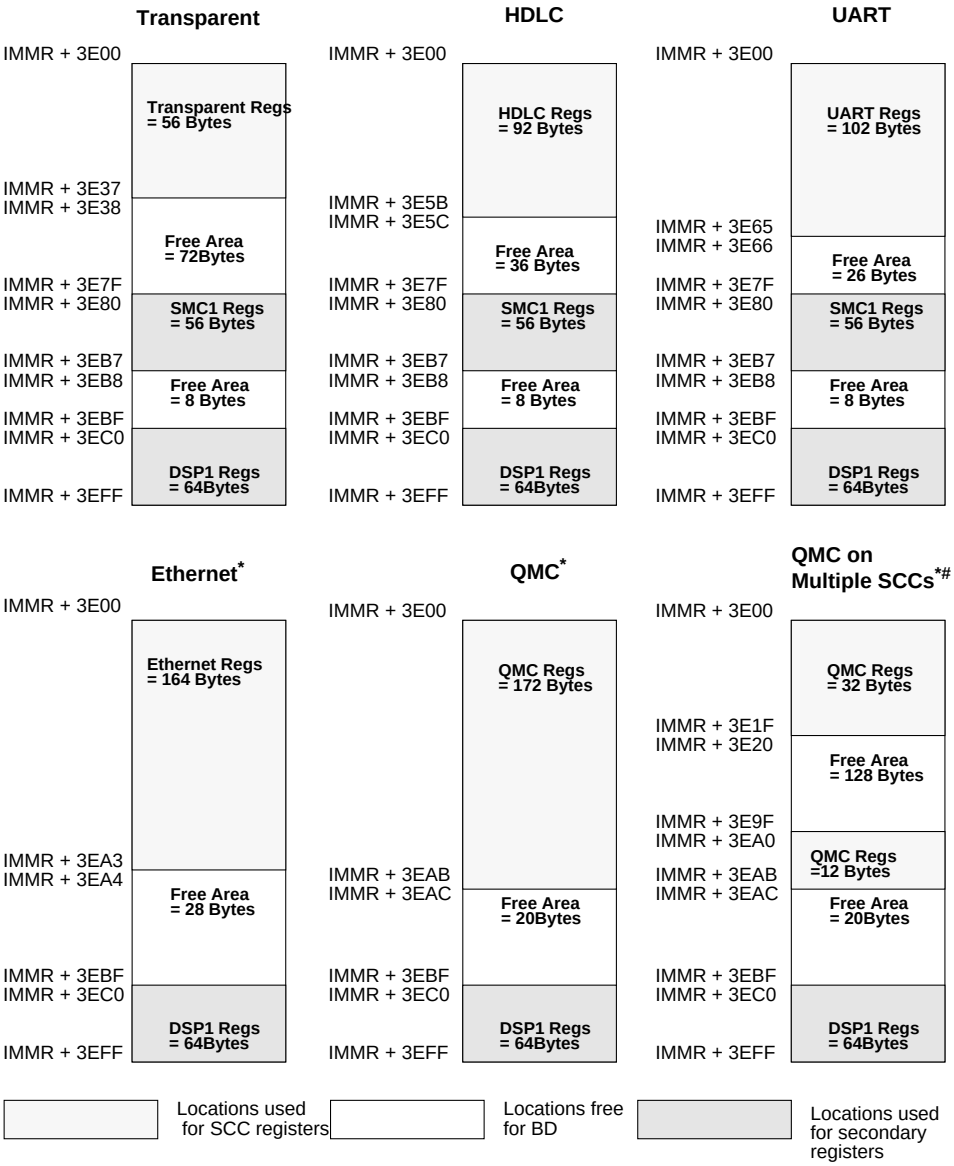


Figure 5-4. Relation between PAD and NOF



 # —TSATRx & TSATTx are mapped to an alternative SCC's parameter RAM.

Figure 5-7. MC68MH360 SCC1 Parameter RAM Usage



#—TSATRx & TSATTx are mapped to an alternative SCC's parameter RAM.
***—SMC1 is not available in these configurations due to memory conflict.**

Figure 5-14. MPC860MH SCC3 Parameter RAM Usage

```
            pdpr->ch[v1].ZDSTATE = 0x80;
            pdpr->ch[v1].INTMSK = 0xA;
            pdpr->ch[v1].MFLR = 60;
            pdpr->ch[v1].TBPTR = pdpr->ch[v1].TBASE;
            pdpr->ch[v1].RBPTR = pdpr->ch[v1].RBASE;
      };
      chbd[0].recvbd0.rxbdptr = (char *)((int)chbd + 0x100);/*   receive   BD0
      pointer=0x100 */
      chbd[1].recvbd0.rxbdptr = (char *)((int)chbd + 0x200);/*   receive   BD1
      pointer=0x200 */
      chbd[2].recvbd0.rxbdptr = (char *)((int)chbd + 0x300);/*   receive   BD2
      pointer=0x300 */
      chbd[3].recvbd0.rxbdptr = (char *)((int)chbd + 0x400);/*   receive   BD3
      pointer=0x400 */
      for (v1 = 0; v1 < 4; v1++)
      {
            chbd[v1].recvbd0.rxbdsac.E = 1;     /* mark receive bufs empty */
            chbd[v1].recvbd0.rxbdsac.W = 1; /*endreceive buffer descriptors */
            chbd[v1].recvbd0.rxbdsac.I = 1;     /* enable intrpts */
/* Continuous mode bits are initialized to 0 from reset */
/* Transmit data length field is initialized to 0 from */
/* reset; the Ready bit is also 0 from reset. */
            chbd[v1].xmitbd0.txbdsac.W = 1;/* end xmit buffer descriptors */
            chbd[v1].xmitbd0.txbdsac.I = 1;     /* enable intrpts */
            chbd[v1].xmitbd0.txbdsac.L = 1;     /* last buffer in frame */
            chbd[v1].xmitbd0.txbdsac.TC= 1;     /* xmit CRC sequence */
            chbd[v1].xmitbd0.txbdcnt = 0;       /* clear data length field */
      };
/* Clear interrupt table */
      intrpt = pdpr->INTBASE;
      for (v1 = 0; v1 < 10; v1++)
      {
            intrpt[v1].V = 0;                   /* clear valid bits */
            intrpt[v1].W = 0;                   /* clear wrap bits */
      };
      intrpt[9].W = 1;
      poem[0] = "Humpty Dumpty sat on a wall\n\r";
      poem[1] = "Humpty Dumpty had a great fall\n\r";
      poem[2] = "All the king's horses and all the king's men\n\r";
```

Chapter 8
Performance

Calculating performance is key to choosing the clock frequency required for a given system. For the 860MH and MH360, the large number of possible channel combinations complicates performance estimation.

This chapter addresses the problem by first providing a performance table for common configurations supported by the 860MH and/or the MH360 in Section 8.1, “Common Channel Combinations.” For configurations not covered in the first section, Section 8.2, “CPM Loading,” covers general guidelines and examples for determining the serial bit rate and CPM loading on a given system. The final section, Section 8.3, “Bus Latency and Peak Load,” addresses system bus utilization and arbitration.

For more definitive answers to performance questions, benchmark the desired configuration on a development board.

8.1 Common Channel Combinations

Table 8-1 provides some common channel combinations configured on the MH devices along with suggested operating frequencies. Note that the MH360 is available only at 25 and 33 MHz,; the 860MH is currently available at 25, 40, and 50 MHz.

Table 8-1. Common QMC Configurations

Protocols Selected	Frequency Supported			
	25 MHz	33 MHz	40 MHz	50 MHz
SCC1: 24-channel QMC. Serial bit rate 1.544 Mbps (T1)	Yes	Yes	Yes	Yes
SCC1: 32-channel QMC. Serial bit rate 2.048 Mbps (E1/CEPT)	Yes	Yes	Yes	Yes
SCC1: 10-Mbps Ethernet; SCC2: 12 x 64-Kbps QMC; SCC3: 12 x 64-Kbps QMC. TDM bit rate = 1.544 Mbps	Yes	Yes	Yes	Yes
SCC1: 10-Mbps Ethernet; SCC2: 16 x 64-Kbps QMC; TDM bit rate = 1.544 Mbps	Yes	Yes	Yes	Yes
SCC1: 32 x 64-Kbps QMC; SCC2: 64 Kbps; SCC3:64 Kbps; SCC4: 64 Kbps; all HDLC.	Yes	Yes	Yes	Yes

Figure A-2 shows the 68360 bit numbering for a time slot assignment table for 64-channel common Rx and Tx mapping.

Figure A-2. Time Slot Assignment Table for 64-Channel Common Rx and Tx Mapping

A.5 SCC Event Register

Figure A-12 shows the 68360 bit numbering for the SCC event register.

7	6	5	4	3	2	1	0
				IQOV	GINT	GUN	GOV

Figure A-12. SCC Event (SCCE) Register

A.6 SCCM Register

Figure A-13 shows the 68360 bit numbering for the SCCM register.

7	6	5	4	3	2	1	0
				IQOV	GINT	GUN	GOV

Figure A-13. SCCM Register

A.7 Receive and Transmit Buffer Descriptors

Figure A-14 and Figure A-15 show the 68360 bit numbering for the receive and transmit buffer descriptors.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET + 0	**E**	—	**W**	**I**	L	F	**CM**	—	UB	—	LG	NO	AB	CR	—	—
OFFSET + 2	DATA LENGTH															
OFFSET + 4	RX DATA BUFFER POINTER															
OFFSET + 6																

Figure A-14. Receive Buffer Descriptor (RxBD)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET + 0	**R**	—	**W**	**I**	**L**	**TC**	**CM**	**—**	**UB**	—	—	—	**PAD**			
OFFSET + 2	DATA LENGTH															
OFFSET + 4	TX DATA BUFFER POINTER															
OFFSET + 6																

Figure A-15. Transmit Buffer Descriptor (TxBD)

Appendix C
Connecting ISDN Multiple S/T or U Interfaces to QUICC32

Using IDL or GCI protocols, the MC145574 (S/T interface) and the MC145572 (U interface) can be gluelessly interfaced to members of the MC68302 family for low-cost, active-ISDN basic rate terminal applications.

For applications needing to support more than one basic rate interface (BRI), such as LAN/WAN bridges, PBX, line cards or multiple-line terminal adaptors, a system solution using multiple MC145574s or MC145572s can be built around a QUICC32 (MC68MH360).

The QUICC32 and the QMC (QUICC's multichannel controller) protocol are useful for such ISDN applications requiring several logical channels on one physical medium.

This appendix shows how multiple MC145574s or MC145572s can be connected to a QUICC32, describing the level-1 connections and explaining the data flow through the devices.

No software issues are addressed in this appendix.

C.1 The QMC Protocol

Based upon the IDL bus, the QMC protocol implemented on the QUICC32 generates a TDM (time-division multiplexing) bus with programmable time slots for each ISDN interface. With 32 time slots, each carrying 8 consecutive bits forming 64-Kbps channels, a 2-Mbps TDM line (roughly equivalent to a CEPT/E1 link) can be created.

Time slot zero (TS0) is dedicated to the first B1 channel, with TS1 assigned to the first B2 channel and TS2 to the first D channel. Even though only 2 bits are used for signaling, the D channel has 8 bits reserved on the TDM link since the QMC microcode must process data on 8-bit boundaries for correct delineation of channels. The unused 6 bits are masked in the QMC time slot assignment table.

Since the TDM line allows a maximum of 32 channels, the above process of routing channels to time slots (that is, the second B1 channel routed to TS3 and so on) can be repeated for up to 10 BRIs.

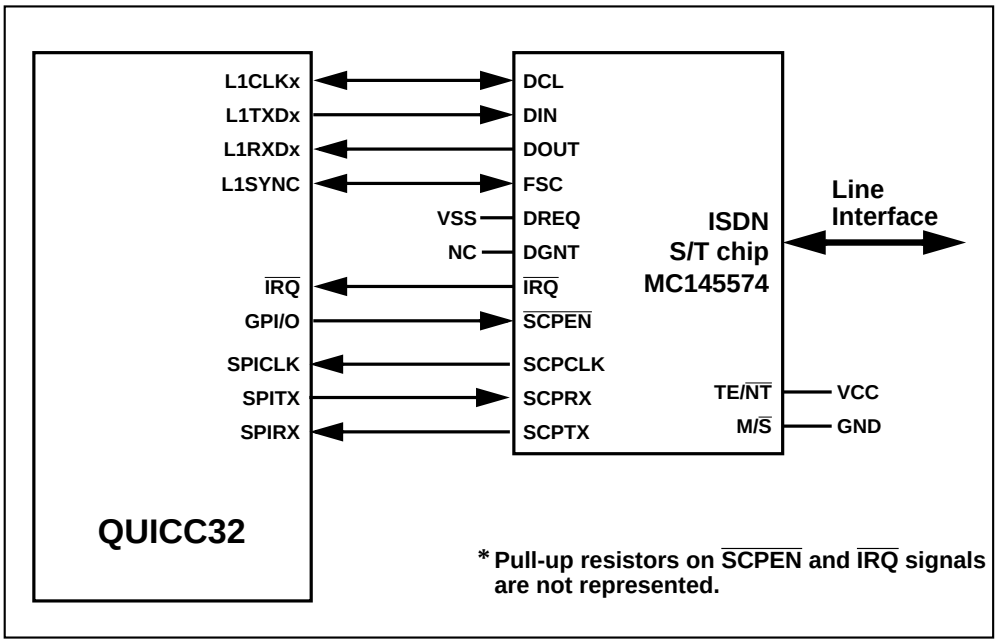


Figure C-2. IDL and SCP Connections between the QUICC32 and the S/T Interface

The QUICC32 is always a slave on the IDL bus, with the data clock (DCL) and frame sync (FSC) signals acting as inputs. As explained in Section C.3, “Data Clock (DCL) and Frame Sync (FSC) Generation,” this specific application requires the S/T interface be configured in slave mode on the IDL bus, with external circuitry providing the DCL and FSC signals to both the QUICC32 and the S/T interface.

The D channel request/grant function is not required for this application since each S/T is assumed to be directly connected to the NT1 (that is, point-to-point configuration with only one TE connected to one NT).

The DGNT signal is left unconnected, and DREQ can be directly connected to VSS. As there is no contention on the D channel, the D channel contention procedure of the MC145574 should be disabled by setting BR7[6].

Figure C-3 shows the connection between the QUICC32 and a U interface.

C.3.1.1 Activation Procedure

If no S/T transceiver is active, no TCLK clock is generated. Once the first transceiver is activated, it will generate a TCLK signal only if DCL and FSC signals are present as well.

Pseudo DCL and FSC signals generated from one of the baud rate generators (BRG) of the QUICC32 can be used to generate the TCLK signal. The BRG can generate a clock based on the QUICC32's system clock. A divider factor should be chosen so that the BRG frequency is close to 2.048 MHz. This clock then feeds into the 256-divider circuitry of Figure C-4 to generate a pseudo DCL and a pseudo FSC.

A multiplexer commanded by the QUICC32 is required to select either the BRG signal or the TCLK signals of the transceivers to be the clock master generating the DCL and FSC signals.

When no transceiver is activated, the QUICC32 selects the BRG to be the clock master, and the S/T interface receives the pseudo DCL and FSC signals. (These two signals are not synchronized to the network but are not used to sample data.)

As the first MC145574 is activated, it will be able to generate the TCLK signal; see Figure C-7. This transceiver will then send an interrupt to the QUICC32 (IRQ3—register NR3[3]—meaning Info 2 has been received) indicating that the activation process has begun. The QUICC32 then uses the multiplexer to select the TCLK signal of that MC145574 to be the clock master.

As shown in Figure C-7 and Figure C-8, the TCLK signal is present before the interruption, with at least 750 µs between the IRQ and the received Info 4. The QUICC32 therefore has 750 µs to react to the IRQ and to select the new clock master.

C.3.2 MC145572 U Interface

The FREQREF signal of the MC145572 provides a clock synchronized to the network timing for the U interface. This frequency reference is a fixed 2.048-MHz clock enabled by setting OR8[4] in the MC145572 register set.

The U interface's FREQREF differs from the TCLK of the S/T interface. When enabled, the FREQREF signal generates the 2.048-MHz clock regardless of the activation status of the U interface (but that clock is synchronized to the network only when the U interface is activated). Also, FREQREF does not require the DCL and FSC signals to enable clock generation.

Like the S/T interface, on the other hand, the FREQREF signal can be used as the DCL for the IDL bus. When divided by 256, FREQREF can also be used to generate the 8-KHz frame sync FSC. The same logic design used for the S/T interface must be added to insure a correct FSC duty cycle; see Figure C-4.

Also like the S/T interface, elastic buffers are included to allow the U interface to operate with any phase relationship between the IDL frame sync and the network.

Figure C-10 shows a block diagram of the connection between four U interfaces and the QUICC32. The diagram would be the same for up to 10 U interfaces.