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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	CPU32+
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	25MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	357-BGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68mh360zp25vl

TABLES

Chapter 1
Overview

This chapter gives an overview of the QMC protocol including some example applications.

1.1 The QMC (QUICC Multichannel Controller)

The QMC protocol emulates up to 64 logical channels within one SCC (serial communication controller) using the same time-division-multiplexed (TDM) physical interface. This multichannel protocol is implemented using the CPM ROM space and additional hardware; it is not a downloadable microcode.

The standard QUICC family members (MC68360[1], MPC860[2], etc.) work in TDM applications but can only support one logical channel per SCC. The parts currently supporting the QMC protocol are a superset to the following devices:

- MC68MH360 is a superset of the MC68EN360[3]
- MPC860MH is a superset of the MPC860EN
- MPC860DH is a superset of the MPC860DE

The QMC parts are pin-compatible with their respective family members. With minor adjustments, they can be used in identical applications such as primary rate ISDN support.

1.2 Introduction

Ideal for E1/T1 applications, the QMC protocol can multiplex any 64-channel combination of subgroups to one TDM interface.

Each of the channels can be separately programmed either to perform HDLC formatting/deformatting or to act as a transparent channel.

Both of the SI serial interfaces (for example, TDM_a or TDM_b) can be dedicated to the QMC protocol. The SI transfers the whole frame to an SCC[4]. Using the CPM RISC, the SCC

[1]MC68360 is trademarked as the QUICC.
[2]MPC860 is trademarked as the PowerQUICC.
[3]On the MC68MH360, protocol support for Centronics and BISYNC have been removed to create space for the QMC microcode.
[4]This is the normal operating mode; however, it is possible to split the TDM stream over several SCCs.

Chapter 2
QMC Memory Organization

This section describes the operation specific to the QMC protocol. When not running the QMC protocol, SCCs operate as described in the MC68360 and MPC860 user's manuals.

Figure 2-1 shows the dual-ported RAM structure for the MC68MH360 and the MPC860MH. The MC68MH360 and the MPC860MH have similar functionality but are organized in a different manner.

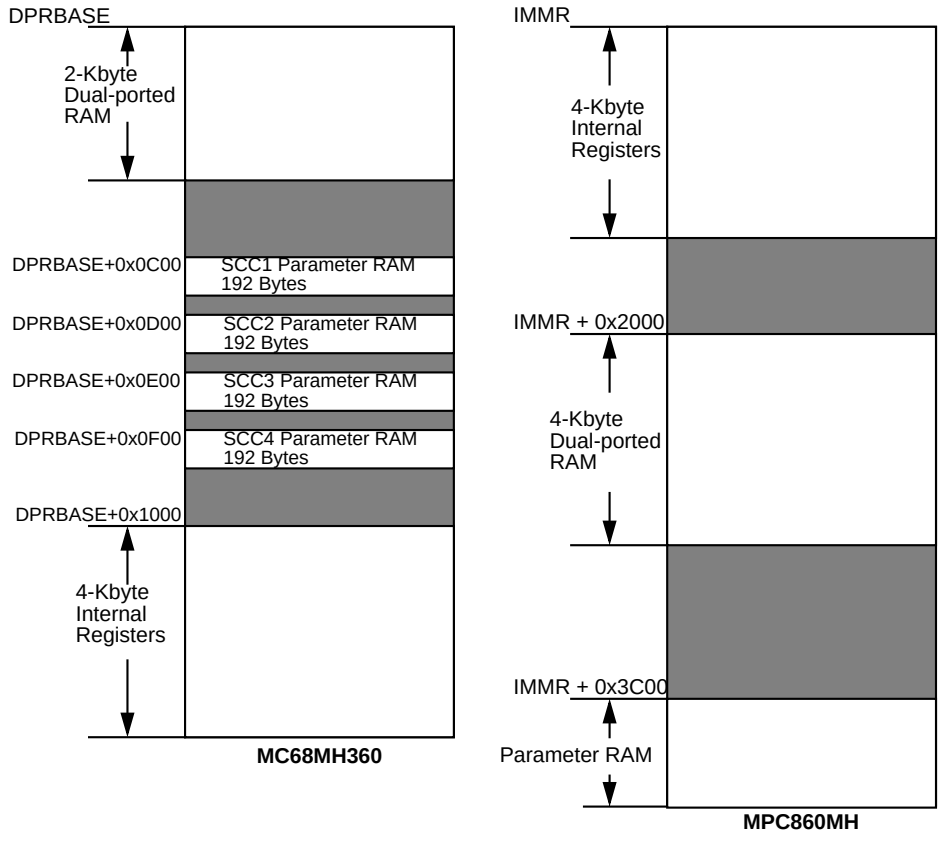


Figure 2-1. MC68MH360 and MPC860MH Internal Memory Structures

2.1.8 Data Buffer Pointer

As with the standard CPM protocols, the data buffer is addressed by a 32-bit pointer within the buffer descriptor. This addresses the data received or transmitted from external memory.

2.1.9 Data Buffer

The data buffers in external memory can hold up to 64 Kbytes of data as determined by the data length in the buffer descriptor.

2.2 Global Multichannel Parameters

The global multichannel parameters reside in the SCC's parameter RAM page and are common to all logical channels.

The largest portion of the global area is the time slot assigner tables for the receiver and transmitter section of the SCC. For 32-channel support, there is one table for Tx and one for Rx within the parameter RAM. If the connection is split over multiple SCCs, this table only needs to be present once for multiple SCCs operating in QMC mode. See Section 2.3, "Multiple SCC Assignment Tables," for more information. For 64-channel support there is only space for one table; therefore common Rx and Tx parameters will need to be used unless one of the TSA tables can be accommodated elsewhere in memory, such as in the parameter RAM area of another SCC.

The dual-ported RAM is used for the channel-specific area for all SCCs. It is important that individual time slots are mapped to only one SCC, and that individual logical channels are separated to avoid contention.

Table 2-1 lists the global parameters. Note that the boldfaced parameters must be initialized by the user. See Chapter 6, "QMC Initialization," for more information.

Table 2-1. Global Multichannel Parameters

Offset to SCC Base	Name	Width (Bits)	Description
00	**MCBASE**	32	Multichannel base pointer—This host-initialized parameter points to the starting address of the 64-Kbyte buffer descriptor table in external memory. The MCBASE is used with the TBASE and RBASE registers in the channel-specific parameters.
04	**QMCSTATE**	16	Multichannel controller state (initialize to 0x8000)—Internal QMC state machine value used by RISC processor for global state definition.

NOTE

The area between SCC base + 20 and SCC base + 9F is normally used for TSA tables. The mapping above is ideal for 32-channel support. The exact mapping of the TSA tables is determined by the programming of Rx_S_PTR and Tx_S_PTR, and is not fixed. For 64-channel support it is suggested to use common Rx and Tx parameters. The TSA table will be common and have 64 entries starting at SCC base + 20; see Figure 2-4. Alternatively, another SCC's parameter RAM may be used, as determined by Rx_S_PTR and Tx_S_PTR; see Figure 2-6 for more information. However implemented, the TSA tables may reside anywhere in internal memory.

Figure 2-3 shows a general time slot assignment table for 32 16-bit time slots. The fields will be used to either transmit or receive channels.

Time Slot 0	V	W	Mask(0:1)	Channel Pointer	Mask(2:7)
Time Slot 1	V	W	Mask(0:1)	Channel Pointer	Mask(2:7)
	V	W	Mask(0:1)	Channel Pointer	Mask(2:7)
					32 x 16
	V	W	Mask(0:1)	Channel Pointer	Mask(2:7)
	V	W	Mask(0:1)	Channel Pointer	Mask(2:7)
Time Slot 30	V	W	Mask(0:1)	Channel Pointer	Mask(2:7)
Time Slot 31	V	W	Mask(0:1)	Channel Pointer	Mask(2:7)

Note: For the 68360, the bit numbering is reversed. See Appendix A for more information.

Figure 2-3. Time Slot Assignment Table

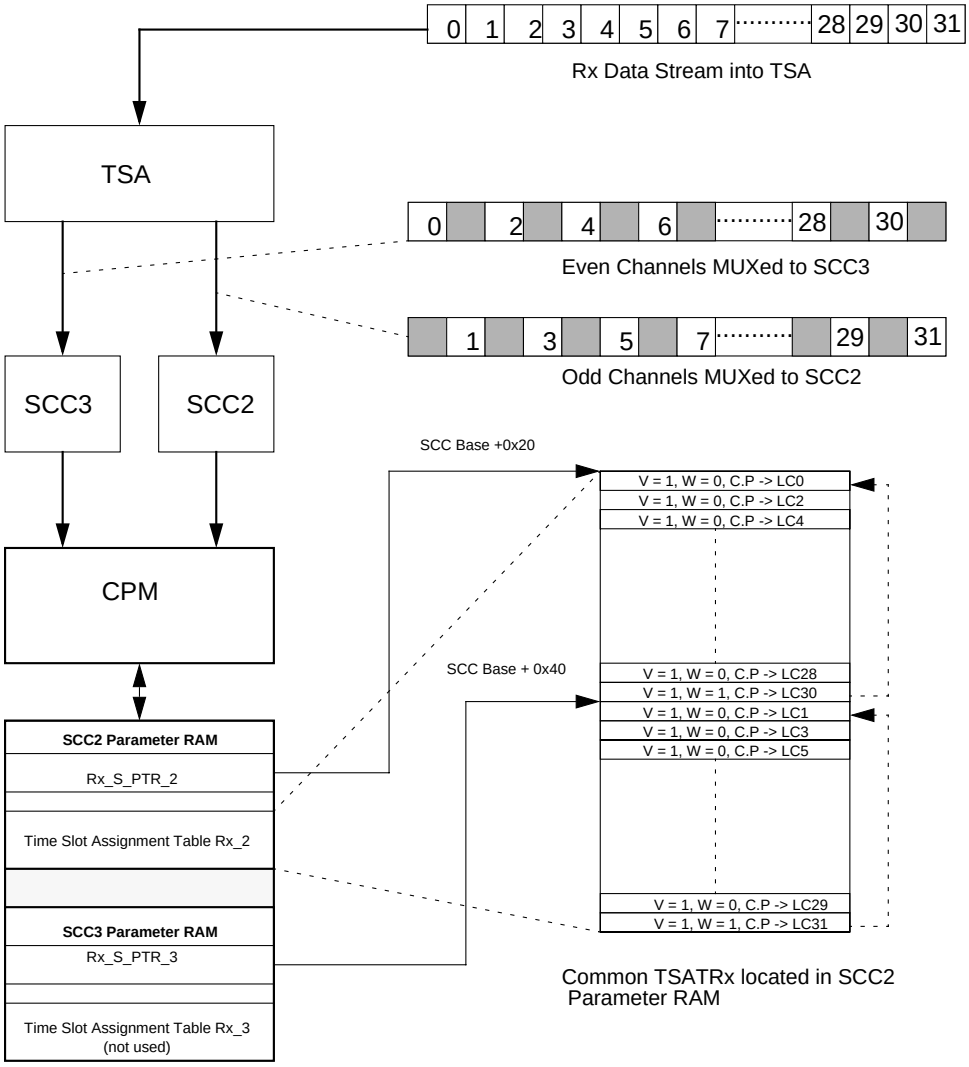


Figure 2-5. Rx Time Slot Assignment Table for 32 Channels over Two SCCs

Note

It is important that multiples of bytes are routed to each SCC to delineate between time slots. Unused bits shall be routed to the SCC and be masked in the time slot assignment table.

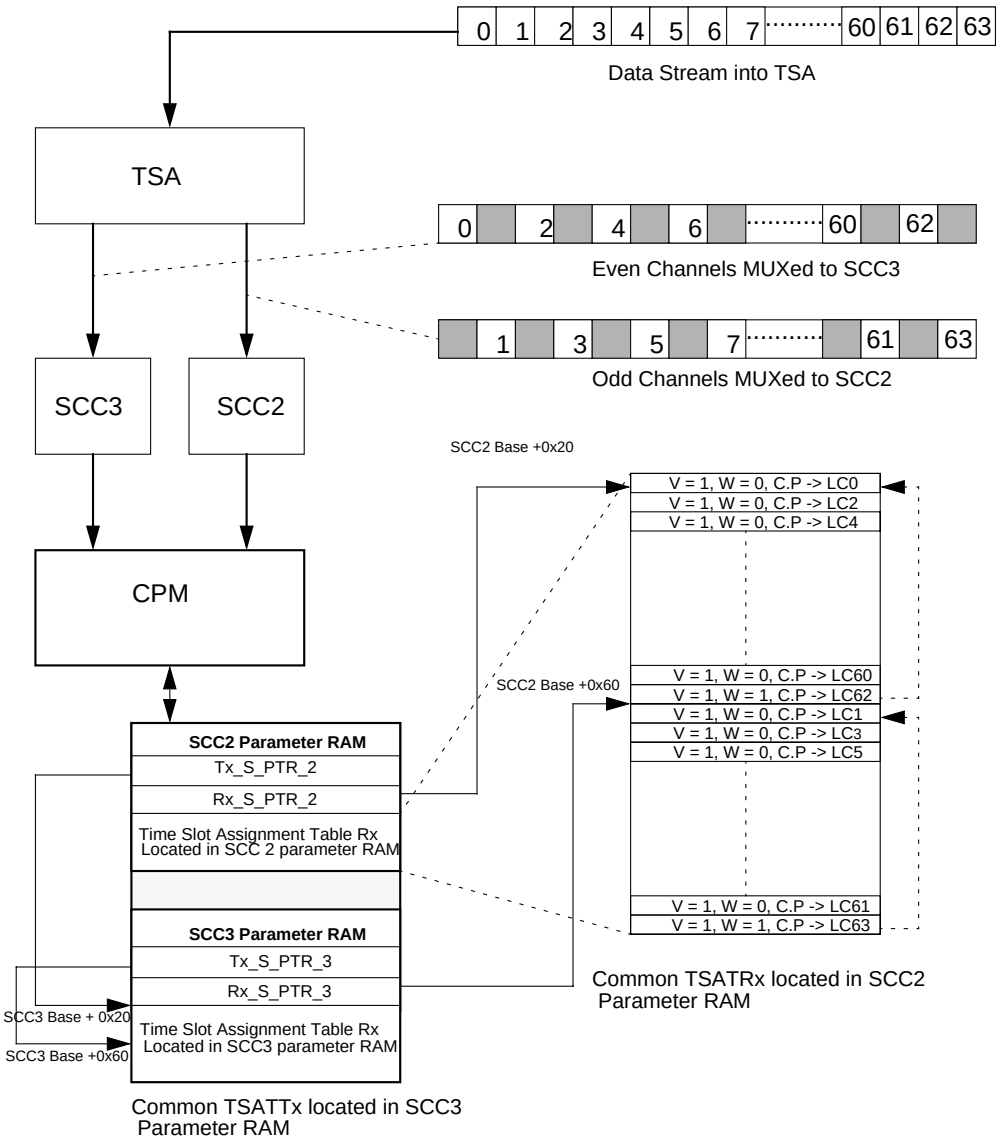


Figure 2-6. Time Slot Assignment Tables for 64 Channels over 2 SCCs

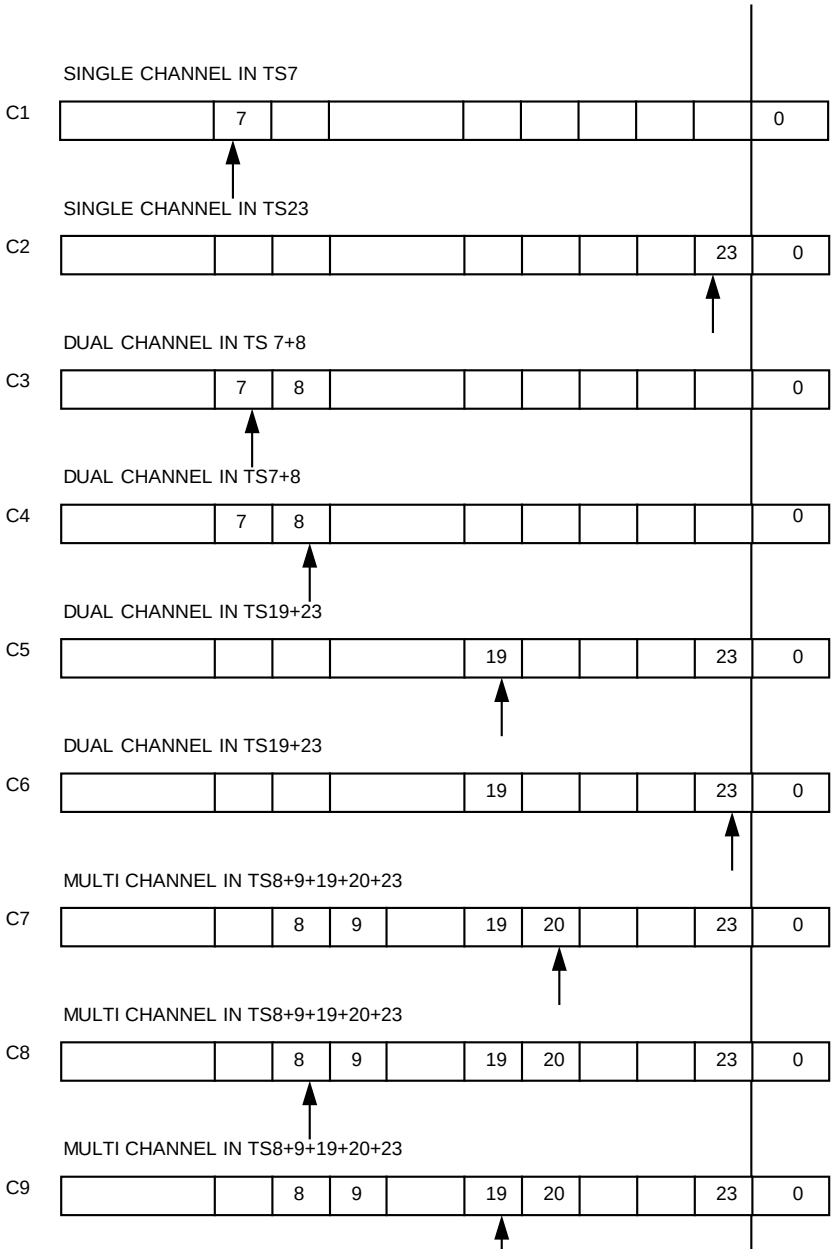
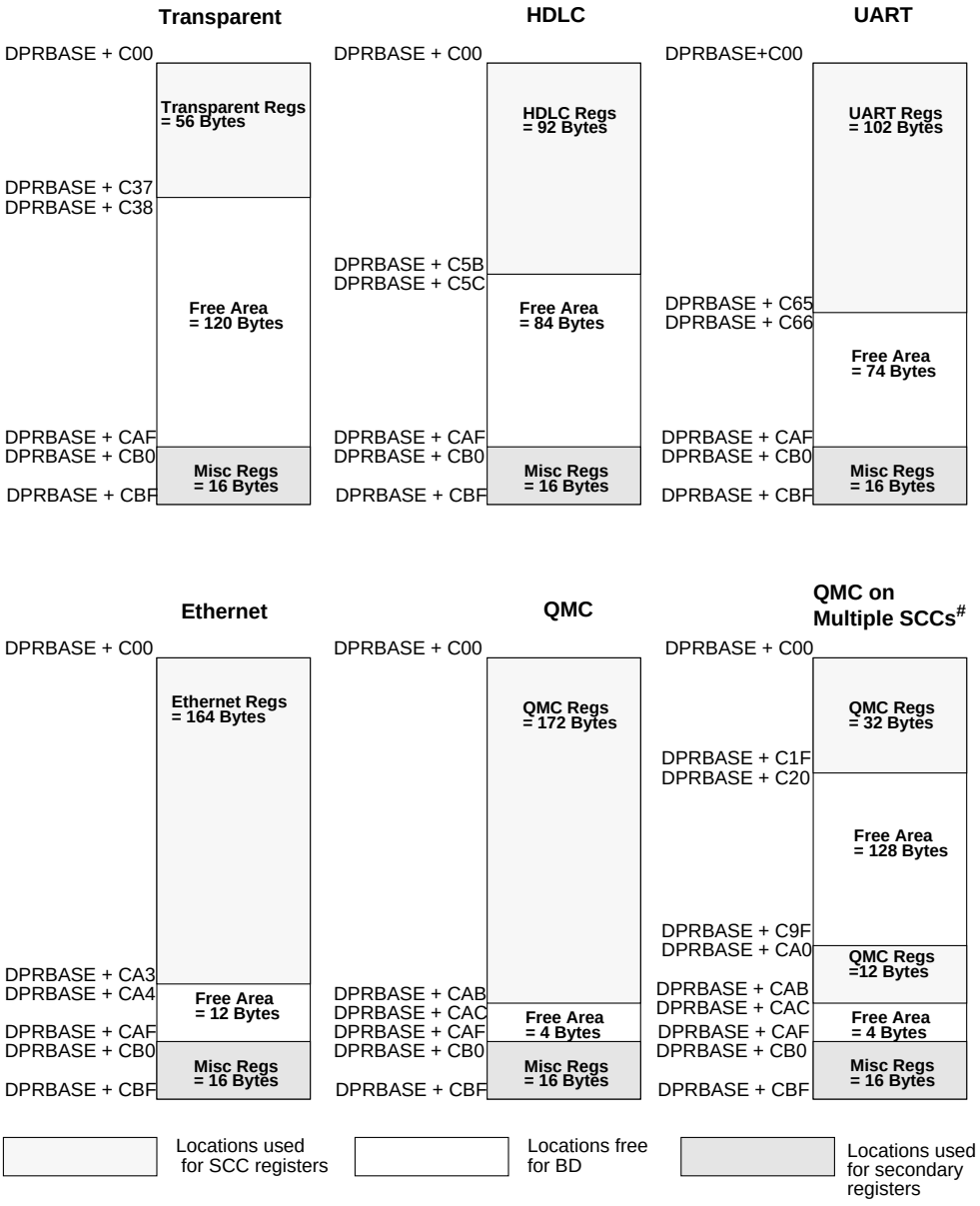


Figure 2-14. Examples of Different T1 Time Slot Allocation

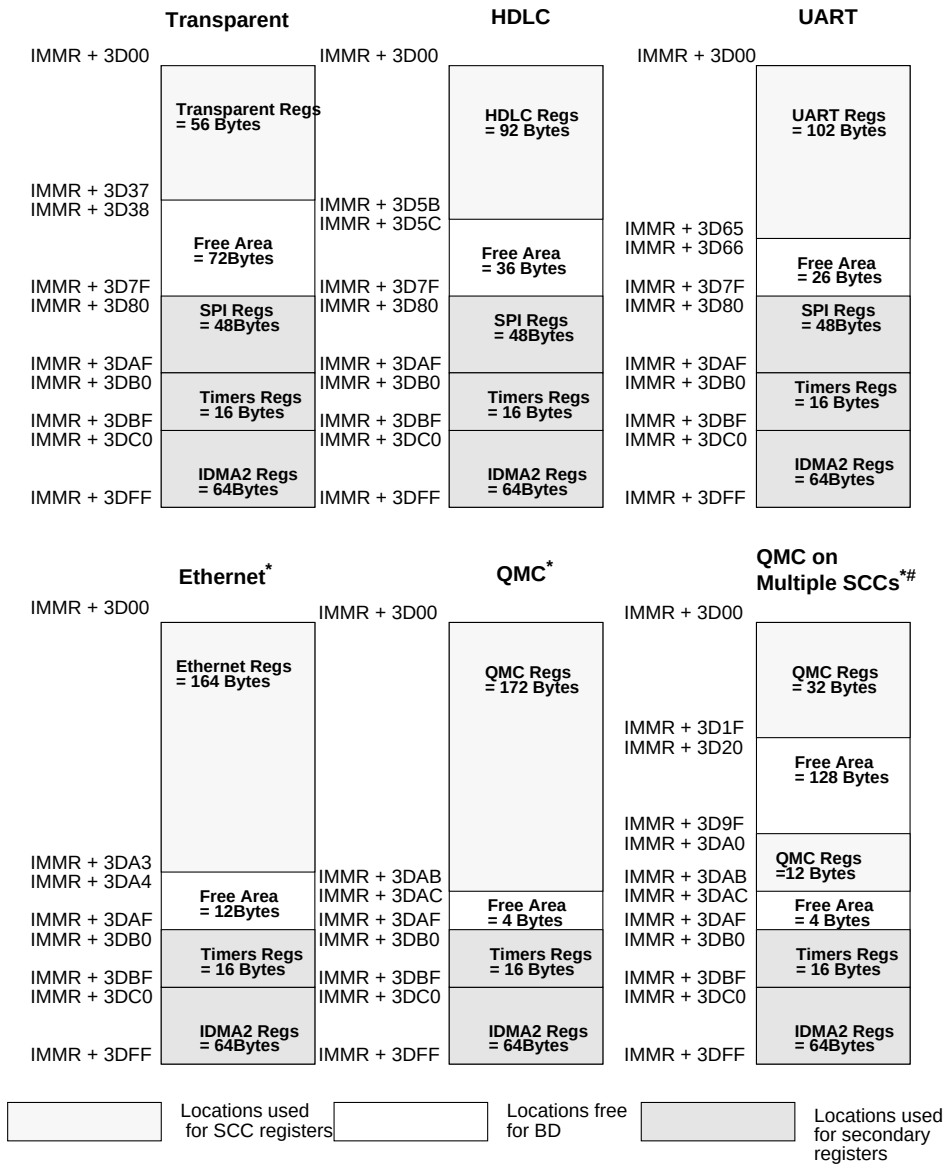
Table 5-1. Receive Buffer Descriptor (RxBD) Field Descriptions (Continued)

Field	Name	Description
1	—	—
2	**W**	Wrap (final buffer descriptor in table) 0 This is not the last buffer descriptor in the RxBD table. 1 This is the last buffer descriptor in the RxBD table. After this buffer is used, the CPM receives incoming data into the first buffer descriptor in the table (the buffer descriptor pointed to by RBASE). The number of RxBDs in this table is programmable and is determined only by the wrap bit and by the space constraints of the dual-ported RAM.
3	**I**	Interrupt 0 The RXB bit will not be set after this buffer has been used, but RXF operation remains unaffected. 1 The RXB bit (and/or the RXF bit in HDLC mode) of the interrupt table entry will be set when this buffer has been used by the HDLC controller. These two bits may cause interrupts (if enabled).
4	L	Last-in-frame (HDLC mode only)—The HDLC controller sets L when this buffer is the last in a frame. This implies the receipt of a closing flag or reception of an error, in which case one or more of the CD, OV, AB, and LG bits are set. The HDLC controller writes the number of frame octets to the data length field. 0 This buffer is not the last in a frame. 1 This buffer is the last in a frame.
5	F	First-in-frame—The controller sets this bit when this buffer is the first in a frame. 0 The buffer is not the first in a frame. 1 The buffer is the first in a frame.
6	**CM**	Continuous Mode 0 Normal operation. 1 The empty bit is not cleared by the CPM after this buffer descriptor is closed, allowing the associated data buffer to be overwritten automatically when the CPM next accesses this buffer descriptor. The empty bit is not cleared if an error occurs during reception. The user must terminate continuous mode by clearing this bit.
7	—	—
8	UB	User bit—The CPM never touches, sets, or clears this user-defined bit. The user determines how this bit is used. For example, it can be used to signal between higher level protocols whether a buffer has been processed by the CPU.
9	—	—
10	LG	Rx frame length violation (HDLC mode only)—A frame length greater than the maximum value was received in this channel. Only the maximum-allowed number of bytes, MFLR rounded to the nearest higher longword alignment, are written to the data buffer. This event is recognized as soon as the MFLR value is exceeded when data is long-word-aligned. When data is not long-word-aligned, this interrupt occurs when the SDMA writes 32 bits to memory. The worst-case latency from MFLR violation until detected is 3-byte timings for this channel. When MFLR violation is detected, the receiver is still receiving even though the data is discarded. The buffer is closed when a flag is detected, and this is considered to be the closing flag for this buffer. At this point, LG = 1 and an interrupt may be generated. The length field for this buffer includes everything between the opening flag and this last identified flag.



 # —TSATRx & TSATTx are mapped to an alternative SCC's parameter RAM.

Figure 5-7. MC68MH360 SCC1 Parameter RAM Usage



#—TSATRx & TSATTx are mapped to an alternative SCC's parameter RAM.
***—SPI is not available in these configurations due to memory conflict.**

Figure 5-13. MPC860MH SCC2 Parameter RAM Usage

Chapter 9
Multi-Subchannel (MSC) Microcode

The RISC processor in the PowerQUICC has an option to execute microcode from the internal dual-ported RAM. Motorola uses this feature to enhance existing protocols or implement additional protocols. Customers can purchase RAM microcodes in an object-code format and download it to the PowerQUICC dual-ported RAM during system initialization.

The RAM microcode is provided by Motorola as a set of S records that can be downloaded directly to an application development system or stored in a system EPROM; for more information on S records, see Appendix C of the *M68000 Family Programmer's Reference Manual*. After system reset, the binary of the microcode should be copied to the dual-ported RAM. The QUICC registers, including the RISC controller configuration register (RCCR), should be initialized as specified in the microcode RAM documentation. Before the RISC is used in the system, the user should issue a reset command to the communications processor command register (CR). The microcode RAM functions are available in addition to all protocols available in the standard QUICC microcode ROM.

9.1 MSC Microcode Features

The multi-subchannel (MSC) microcode is a downloadable microcode for the MPC860MH and has the following key features:

- General
  - Multiple subchannels within a single 8-bit time slot
  - Bit resolution for subchannels
  - Up to 32 independent communications channels for both Rx and Tx
  - Supports either transparent or HDLC protocols per subchannel
- Performance
  - 32 channels + 10-Mbps ethernet support at 40-MHz system clock

Figure A-2 shows the 68360 bit numbering for a time slot assignment table for 64-channel common Rx and Tx mapping.

Figure A-2. Time Slot Assignment Table for 64-Channel Common Rx and Tx Mapping

- A hybrid approach runs a single line of up to 64 multiplexed time slots to two separate SCCs, each with its own set of parameters. Normally this would route 32 time slots to each SCC. This would have the benefit of doubling your effective FIFO depth, allowing greater system design flexibility.

Q: My understanding is that the MH360 could not support the SS-7 microcode. Is this also true of the 860MH?

A: The 860MH will not support SS-7 over the multiplexed (QMC) channels. If SS-7 is to be run, it must be run over its own dedicated SCC. However, by using the time slot assigner, the traffic from this SCC could be routed over the same E1 or T1 as the other multiplexed HDLC channels.

For example, one channel of an E1 could be routed to an SCC running SS-7, and the other 31 channels to an SCC running QMC. Thus, the number of SS-7 channels allowed is limited to the number of SCCs (that is, at most 4).

Q: What is the CPM's maximum CPU bus utilization when running two 2-Mbps QMC channels?

A: For 64 channels (two E1 lines), two 2-Mbps full duplex means 8 Mbps of aggregate traffic. Factoring in a large margin for buffer descriptor accesses bumps this 8 Mbps up to 10 Mbps. The 10 Mbps of traffic translates to 0.3 megatransfers of 32 bits each requiring only 1.5 MHz out of a 50-MHz bus (assuming a 5 wait-state memory). A similar calculation for Ethernet would account for higher data traffic and fewer descriptor accesses.

Q: Is the 860MH pin compatible with the 860DH?

A: Yes, it is pin compatible.

Q: Are BISYNC and Centronics still removed from the 860MH as they are with the MH360?

A: No, Centronics and Bisync are both supported on the 860MH.

Q: How is time slot 0 identified on an SCC? Is an external sync required?

A: The TSA identifies time slot 0. A sync pulse must be provided to the TSA at the beginning of a frame.

Q: What does the larger dual-ported RAM on the 860MH provide?

A: The larger dual-ported RAM means that up to 64 QMC channels may be supported. It also provides more buffer descriptor area needed for the higher serial performance at higher speeds.

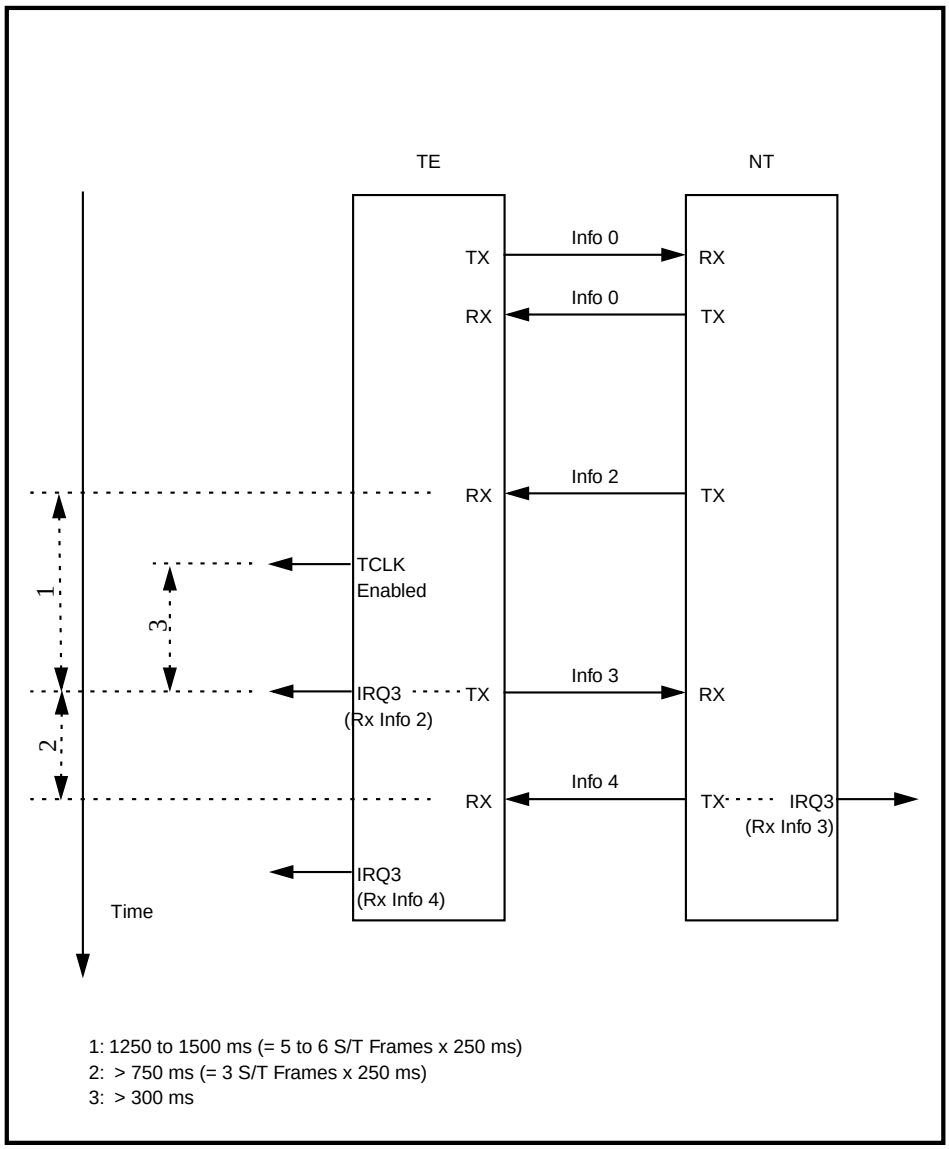


Figure C-7. Timing Diagram for an Activation Initiated by the NT

C.3.3.2 U-Interface Configuration

Do the following for U-interface configuration:

- IDL2 with time slot assigner (TSA enabled in reg. OR6[5–7]; TSA selection in reg. OR0 to OR5)
- Slave mode (DCL & FSC are input) - (pin M/$\overline{S}$ to GND)
- FREQREF enabled at 2.048 MHz (reg. OR8[4] = 1)

C.3.3.3 QUICC32 Configuration

Do the following for QUICC32 configuration:

- SCC3 using the QMC protocol for handling the different channels of the multiplexed IDL2 bus. (D channels are HDLC encoded/decoded and B-channels can be configured for transparent or HDLC framing)
- SCC1 can be configured for Ethernet, HDLC, transparent, or UART.
- SCC2 and SCC4 can be configured for HDLC, transparent, or UART.
- The SPI is connected to the SCP port of each S/T or U interface for handling configuration and control information.
- For the U interface, the SPI/SCP connection can be replaced by a connection of the 8-bit parallel port of the U transceiver to the processor bus of the QUICC.
- One I/O signal can be dedicated for handling the $\overline{SCPEN}$ signal of each S/T or U interface.
- One interrupt signal can be dedicated for handling the $\overline{IRQ}$ signal of each S/T or U interface.