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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	33MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	WDT
Number of I/O	54
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91m42800a-33ai

interrupt request to the ARM7TDMI. It integrates an 8-level priority controller, and, using the Auto-vectoring feature, reduces the interrupt latency time.

The Parallel Input/Output Controllers (PIOA, PIOB) controls up to 54 I/O lines. It enables the user to select specific pins for on-chip peripheral input/output functions, and general-purpose input/output signal pins. The PIO controllers can be programmed to detect an interrupt on a signal change from each line.

There are three embedded system timers. The Real-time Timer (RTT) counts elapsed seconds and can generate periodic or programmed interrupts. The Period Interval Timer (PIT) can be used as a user-programmable time-base, and can generate periodic ticks. The Watchdog (WD) can be used to prevent system lock-up if the software becomes trapped in a deadlock.

The Special Function (SF) module integrates the Chip ID and the Reset Status registers.

5.2.2 User Peripherals

Two USARTs, independently configurable, enable communication at a high baud rate in synchronous or asynchronous mode. The format includes start, stop and parity bits and up to 9 data bits. Each USART also features a Time-out and a Time-guard register, facilitating the use of the two dedicated Peripheral Data Controller (PDC) channels.

The two 3-channel, 16-bit Timer/Counters (TC) are highly-programmable and support capture or waveform modes. Each TC channel can be programmed to measure or generate different kinds of waves, and can detect and control two input/output signals. Each TC also has three external clock signals.

Two independently configurable SPIs provide communication with external devices in master or slave mode. Each has four external chip selects which can be connected to up to 15 devices. The data length is programmable, from 8- to 16-bit.

Figure 11-20. Early Read Protocol with t_{DF}

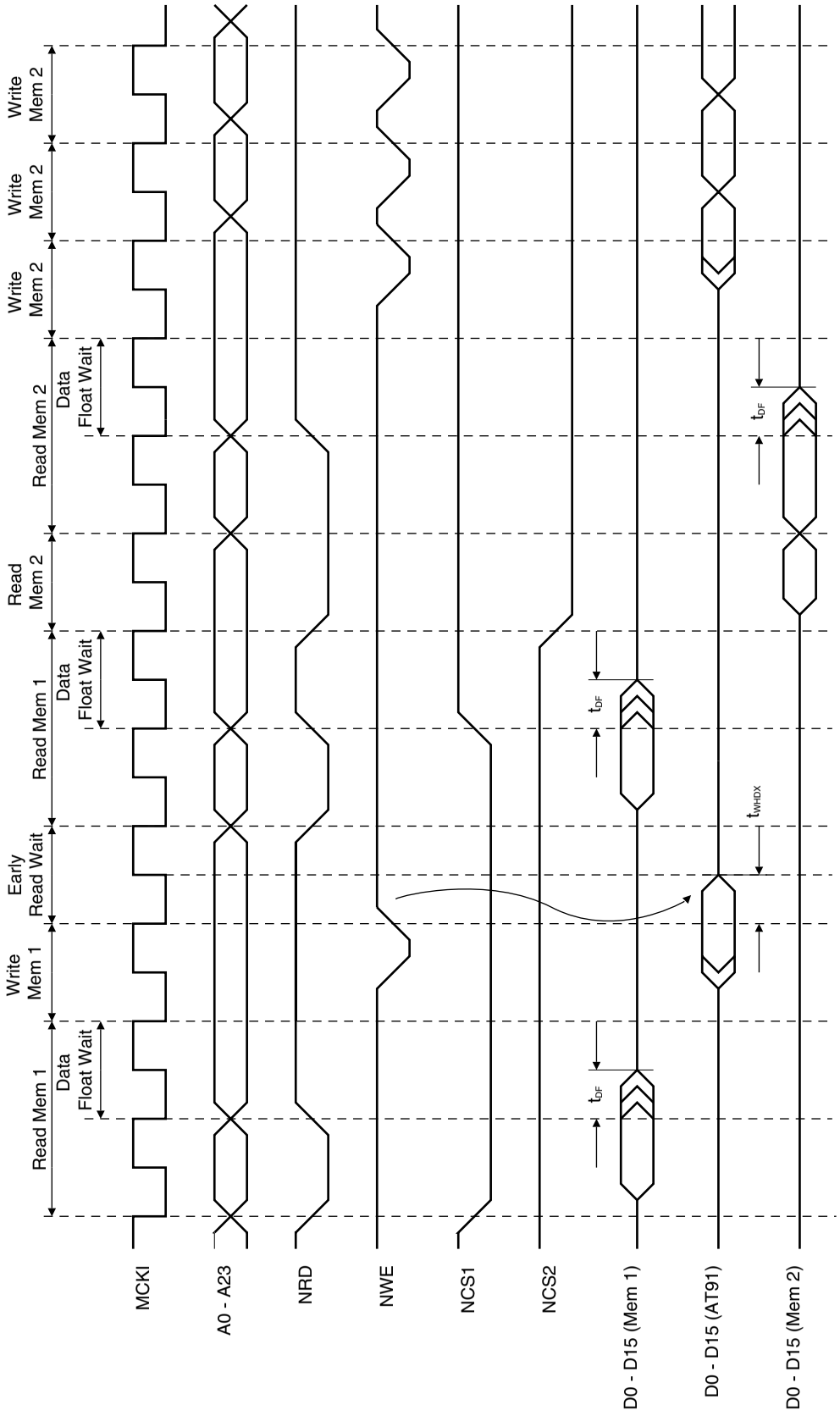
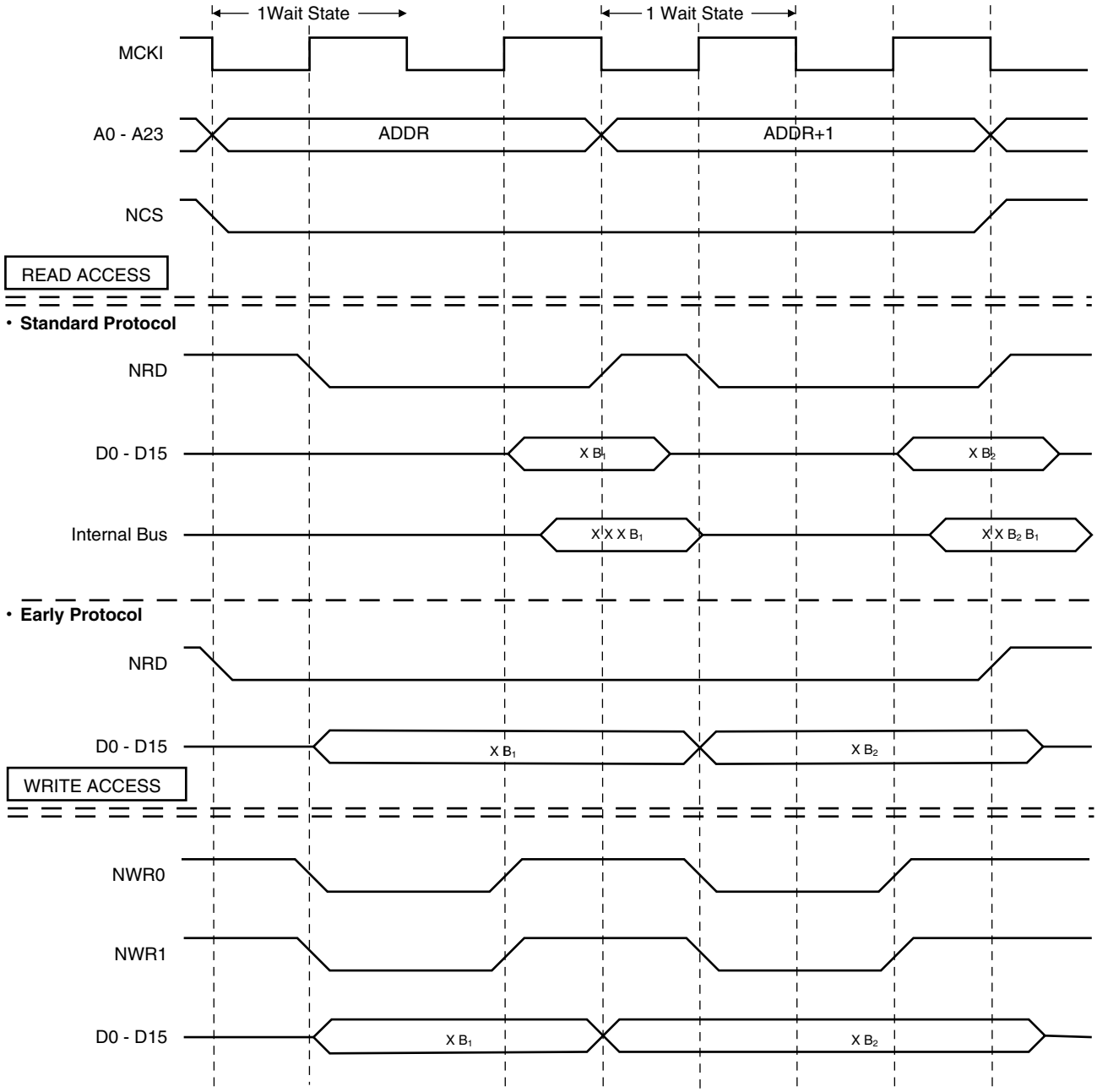


Figure 11-25. 1 Wait State, 8-bit Bus Width, Half-word Transfer



11.18 Abort Address Status Register

Register Name: EBI_AASR
Access Type: Read-only
Offset: 0x34
Reset Value: 0x0

31	30	29	28	27	26	25	24
ABTADD							
23	22	21	20	19	18	17	16
ABTADD							
15	14	13	12	11	10	9	8
ABTADD							
7	6	5	4	3	2	1	0
ABTADD							

- **ABTADD: Abort Address**

This field contains the address required by the last aborted access.

12.8 PMC System Clock Disable Register

Register Name: PMC_SCDR
Access Type: Write-only
Offset: 0x04

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	CPU

- **CPU: System Clock Disable**

0 = No effect.

1 = Disables the System Clock.

12.9 PMC System Clock Status Register

Register Name: PMC_SCSR
Access Type: Read-only
Offset: 0x08
Reset Value: 0x01

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	CPU

- **CPU: System Clock Status**

0 = System Clock is disabled.

1 = System Clock is enabled.

- **CSS: Clock Source Selection**

0 = The clock source is the Slow Clock.

1 = The clock source is the output of the PLL.

- **MUL: Phase Lock Loop Factor**

0 = The PLL is disabled, reducing at the minimum its power consumption.

1 up to 2047 = The PLL output is at frequency (MUL+1) x Slow Clock frequency when the LOCK bit is set.

- **PLLCOUNT: PLL Lock Counter**

Specifies the number of 32,768 Hz clock cycles for the PLL lock timer to count before the PLL is locked, after the PLL is started.

13.4 System Timer User Interface

System Timer Base Address: 0xFFFF8000

Table 5. System Timer Registers

Offset	Register Name	Register Mnemonic	Access	Reset Value
0x00	Control Register	ST_CR	W	–
0x04	Period Interval Mode Register	ST_PIMR	R/W	0x00000000(1)
0x08	Watchdog Mode Register	ST_WDMR	R/W	0x00020000(1)
0x0C	Real-time Mode Register	ST_RTMR	R/W	0x00008000
0x10	Status Register	ST_SR	R	–
0x14	Interrupt Enable Register	ST_IER	W	–
0x18	Interrupt Disable Register	ST_IDR	W	–
0x1C	Interrupt Mask Register	ST_IMR	R	0x0
0x20	Real-time Alarm Register	ST_RTAR	R/W	0x0
0x24	Current Real-time Register	ST_CRTR	R	0x0

Note: 1. Corresponds to maximum value of the counter.

13.5 System Timer Control Register

Register Name: ST_CR
Access Type: Write-only
Offset: 0x00

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	WDRST

- **WDRST: Watchdog Timer Restart**

0 = No effect.

1 = Reload the start-up value in the Watchdog Timer.

15. PIO: Parallel I/O Controller

The AT91M42800A has 54 programmable I/O lines. I/O lines are multiplexed with an external signal of a peripheral to optimize the use of available package pins (see Tables Table 15-1 on page 100 and Table 15-2 on page 101). These lines are controlled by two separate and identical PIO Controllers called PIOA and PIOB. Each PIO controller also provides an internal interrupt signal to the Advanced Interrupt Controller.

Note: After a hardware reset, the PIO clock is disabled by default (see Section 12. "PMC: Power Management Controller" on page 55). The user must configure the Power Management Controller before any access to the User Interface of the PIO.

15.1 Multiplexed I/O Lines

When a peripheral signal is not used in an application, the corresponding pin can be used as a parallel I/O. Each parallel I/O line is bi-directional, whether the peripheral defines the signal as input or output. Figure 15-1 shows the multiplexing of the peripheral signals with Parallel I/O signals.

A pin is controlled by the registers PIO_PER (PIO Enable) and PIO_PDR (PIO Disable). The register PIO_PSR (PIO Status) indicates whether the pin is controlled by the corresponding peripheral or by the PIO Controller.

When the PIO is selected, the peripheral input line is connected to zero.

15.2 Output Selection

The user can enable each individual I/O signal as an output with the registers PIO_OER (Output Enable) and PIO_ODR (Output Disable). The output status of the I/O signals can be read in the register PIO_OSR (Output Status). The direction defined has effect only if the pin is configured to be controlled by the PIO Controller.

15.3 I/O Levels

Each pin can be configured to be driven high or low. The level is defined in four different ways, according to the following conditions.

- If a pin is controlled by the PIO Controller and is defined as an output (see Section 15.2 "Output Selection" on page 97 above), the level is programmed using the registers PIO_SODR (Set Output Data) and PIO_CODR (Clear Output Data). In this case, the programmed value can be read in PIO_ODSR (Output Data Status).
- If a pin is controlled by the PIO Controller and is not defined as an output, the level is determined by the external circuit.
- If a pin is not controlled by the PIO Controller, the state of the pin is defined by the peripheral (see peripheral datasheets).

In all cases, the level on the pin can be read in the register PIO_PDSR (Pin Data Status).

15.4 Filters

Optional input glitch filtering is available on each pin and is controlled by the registers PIO_IFER (Input Filter Enable) and PIO_IFDR (Input Filter Disable). The input glitch filtering can be selected whether the pin is used for its peripheral function or as a parallel I/O line. The register PIO_IFSR (Input Filter Status) indicates whether or not the filter is activated for each pin.

15.5 Interrupts

Each parallel I/O can be programmed to generate an interrupt when a level change occurs. This is controlled by the PIO_IER (Interrupt Enable) and PIO_IDR (Interrupt Disable) registers which enable/disable the I/O interrupt by setting/clearing the corresponding bit in the PIO_IMR. When a change in level occurs, the corresponding bit in the PIO_ISR (Interrupt Status) is set whether the pin is used as a PIO or a peripheral and whether it is defined as input or output. If the corresponding interrupt in PIO_IMR (Interrupt Mask) is enabled, the PIO interrupt is asserted.

When PIO_ISR is read, the register is automatically cleared.

15.6 User Interface

Each individual I/O is associated with a bit position in the Parallel I/O user interface registers. Each of these registers are 32 bits wide. If a parallel I/O line is not defined, writing to the corresponding bits has no effect. Undefined bits read zero.

15.7 Multi-driver (Open Drain)

Each I/O can be programmed for multi-driver option. This means that the I/O is configured as open drain (can only drive a low level) in order to support external drivers on the same pin. An external pull-up is necessary to guarantee a logic level of one when the pin is not being driven.

Registers PIO_MDER (Multi-Driver Enable) and PIO_MDDR (Multi-Driver Disable) control this option. Multi-driver can be selected whether the I/O pin is controlled by the PIO Controller or the peripheral. PIO_MDSR (Multi-Driver Status) indicates which pins are configured to support external drivers.

15.18 PIO Set Output Data Register

Register Name: PIO_SODR
Access Type: Write-only
Offset: 0x30

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

This register is used to set PIO output data. It affects the pin only if the corresponding PIO output line is enabled and if the pin is controlled by the PIO. Otherwise, the information is stored.

0 = No effect.

1 = PIO output data on the corresponding pin is set.

15.19 PIO Clear Output Data Register

Register Name: PIO_CODR
Access Type: Write-only
Offset: 0x34

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

This register is used to clear PIO output data. It affects the pin only if the corresponding PIO output line is enabled and if the pin is controlled by the PIO. Otherwise, the information is stored.

0 = No effect.

1 = PIO output data on the corresponding pin is cleared.

18.6 TC Block Control Register

Register Name: TC_BCR

Access Type: Write-only

Offset: 0xC0

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	SYNC

- **SYNC: Synchro Command (Code Label** TC_SYNC)

0 = No effect.

1 = Asserts the SYNC signal which generates a software trigger simultaneously for each of the channels.

22. Soldering Profile

22.1 LQFP Soldering Profile (Green)

Table 22-1 gives the recommended soldering profile from J-STD-020C.

Table 22-1. Soldering Profile Green Compliant Package

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3° C/sec. max.
Preheat Temperature 175°C ±25°C	180 sec. max.
Temperature Maintained Above 217°C	60 sec. to 150 sec.
Time within 5° C of Actual Peak Temperature	20 sec. to 40 sec.
Peak Temperature Range	260° C
Ramp-down Rate	6° C/sec. max.
Time 25° C to Peak Temperature	8 min. max.

Note: The package is certified to be backward compatible with Pb/Sn soldering profile.

A maximum of three reflow passes is allowed per component.

22.2 BGA Soldering Profile (RoHS-compliant)

Table 22-2 gives the recommended soldering profile from J-STD-20C.

Table 22-2. Soldering Profile RoHS Compliant Package

Profile Feature	Convection or IR/Convection
Average Ramp-up Rate (183° C to Peak)	3° C/sec. max.
Preheat Temperature 125° C ±25° C	180 sec. max
Temperature Maintained Above 183° C	60 sec. to 150 sec.
Time within 5° C of Actual Peak Temperature	20 sec. to 40 sec.
Peak Temperature Range	260° C
Ramp-down Rate	6° C/sec.
Time 25° C to Peak Temperature	8 min. max

Note: It is recomended to apply a soldering temperature higher than 250°C.

A maximum of three reflow passes is allowed per component.