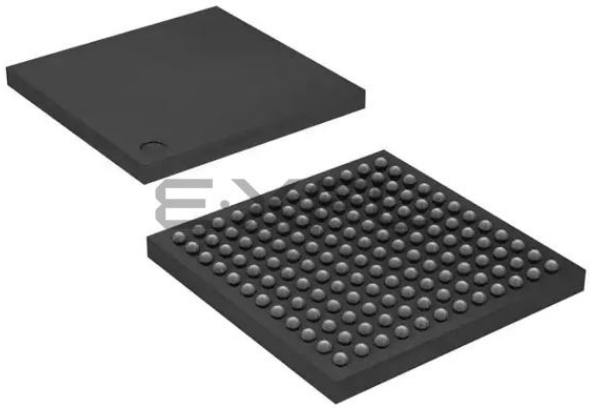

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	33MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	WDT
Number of I/O	54
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-BGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91m42800a-33ci-t

6. Associated Documentation

Table 6-1. Associated Documentation

Information	Document Title
Internal architecture of processor ARM/Thumb instruction sets Embedded in-circuit-emulator	ARM7TDMI (Thumb) Datasheet
External memory interface mapping Peripheral operations Peripheral user interfaces	AT91M42800A Datasheet (this document)
DC characteristics Power consumption Thermal and reliability chonsiderations AC characteristics	AT91M42800A Electrical Characteristics Datasheet
Product overview Ordering information Packaging information Soldering profile	AT91M42800A Summary Datasheet

7. Product Overview

7.1 Power Supply

The AT91M42800A has three kinds of power supply pins:

- VDDCORE pins that power the chip core
- VDDIO pins that power the I/O lines
- VDDPLL pins that power the oscillator and PLL cells

VDDCORE and VDDIO pins allow core power consumption to be reduced by supplying it with a lower voltage than the I/O lines. The VDDCORE pins must never be powered at a voltage greater than the supply voltage applied to the VDDIO.

The VDDPLL pin is used to supply the oscillator and both PLLs. The voltage applied on these pins is typically 3.3V, and it must not be lower than VDDCORE.

Typical supported voltage combinations are shown in the following table:

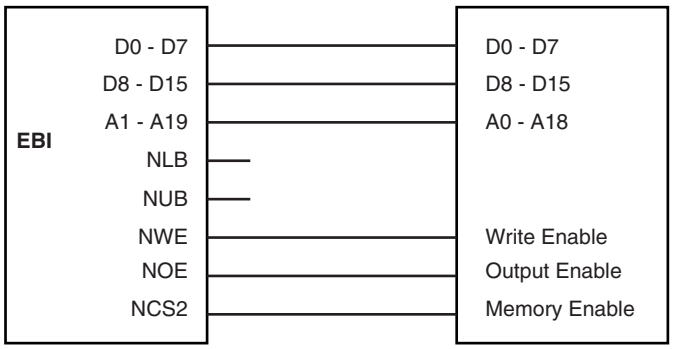
Table 1.

Pins	Nominal Supply Voltages	
VDDCORE	3.3V	3.0V or 3.3V
VDDIO	5.0V	3.0V or 3.3V
VDDPLL	3.3V	3.0V or 3.3V

7.2 Input/Output Considerations

After the reset, the peripheral I/Os are initialized as inputs to provide the user with maximum flexibility. It is recommended that in any application phase, the inputs to the AT91M42800A microcontroller be held at valid logic levels to minimize the power consumption.

Figure 11-8. Connection for a 16-bit Data Bus without Byte Write Capability



11.8 Boot on NCS0

Depending on the device and the BMS pin level during the reset, the user can select either an 8-bit or 16-bit external memory device connected on NCS0 as the Boot memory. In this case, EBI_CSR0 (Chip Select Register 0) is reset at the following configuration for chip select 0:

- 8 wait states (WSE = 0 - wait states disabled)
- 8-bit or 16-bit data bus width, depending on BMS

Byte access type and number of data float time are set to Byte Write Access and 0, respectively.

Before the remap command, the user can modify the chip select 0 configuration, programming the EBI_CSR0 with the exact Boot memory characteristics. The base address becomes effective after the remap command.

Warning: In the internal oscillator bypass mode described in ”Operating Modes” on page 12, the user must take the external oscillator frequency into account according to the minimum access time on the boot memory device.

As illustration, the following table gives examples of oscillator frequency limits according to the time access without using NWAIT pin at the boot.

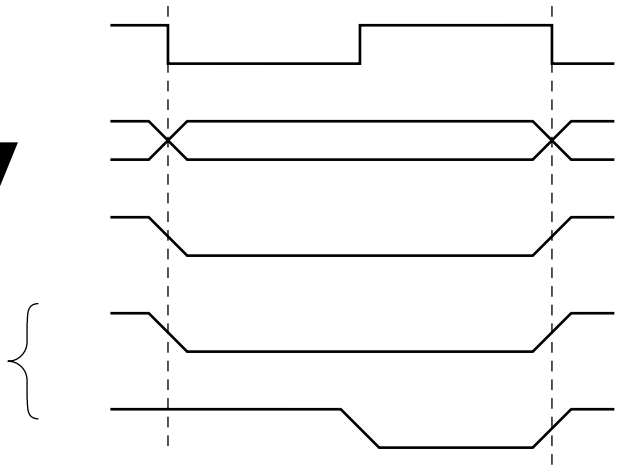
Chip Select Assertion to Output Data Valid Maximum Delay in Read Cycle (t_{CE} in ns)	External Oscillator Frequency Limit (MHz)
110	7
90	9
70	11
55	14
25	24

Note: Values take only t_{CE} into account.

11.9 Read Protocols

The EBI provides two alternative protocols for external memory read access: standard and early read. The difference between the two protocols lies in the timing of the NRD (read cycle) waveform.

Figure 11-10. Early Read Protocol

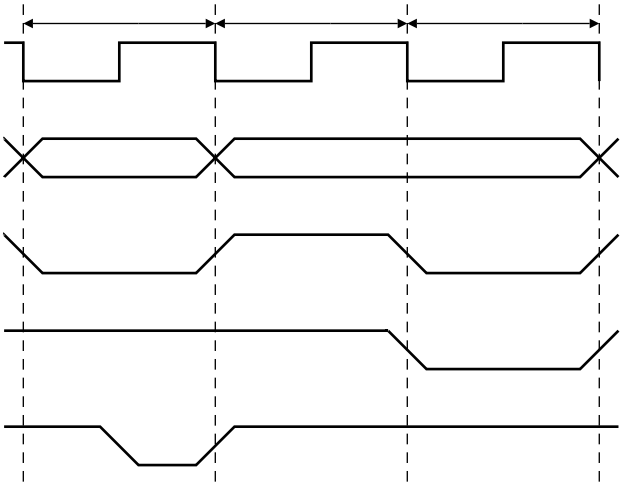


read protocol, an early read wait state is automatically inserted when an external write s followed by a read cycle to allow time for the write cycle to end before the subsequent cycle begins (see Figure 11-11). This wait state is generated in addition to any other pro-nmed wait states (i.e., data float wait).

o wait state is added when a read cycle is followed by a write cycle, between consecutive ccesses of the same type or between external and internal memory accesses.

Early read wait states affect the external bus only. They do not affect internal bus timing.

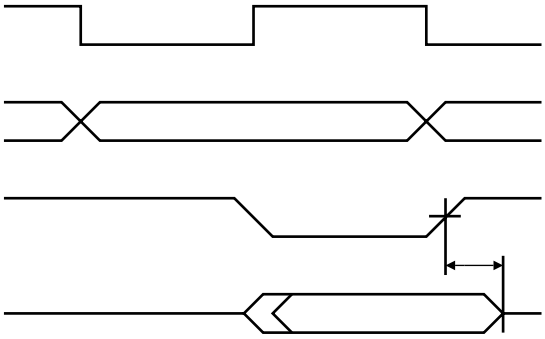
Figure 11-11. Early Read Wait State



es in both protocols, output data becomes valid after the falling edge of the remains valid after the rising edge of NWE, as illustrated in Figure 11-12. The aveform (on the NWE pin) is used to control the output data timing to guaran-n.

It is therefore necessary to avoid excessive loading of the NWE pins, which could delay the write signal too long and cause a contention with a subsequent read cycle in standard protocol.

Figure 11-12. Data Hold Time



ad protocol the data can remain valid longer than in standard read protocol due to onal wait cycle which follows a write access.

EBI can automatically insert wait states. The different types of wait states are listed below:

- Standard wait states
- Data float wait states
- External wait states
- Chip select change wait states
- Early Read wait states (as described in ”Read Protocols” on page 29)

it States

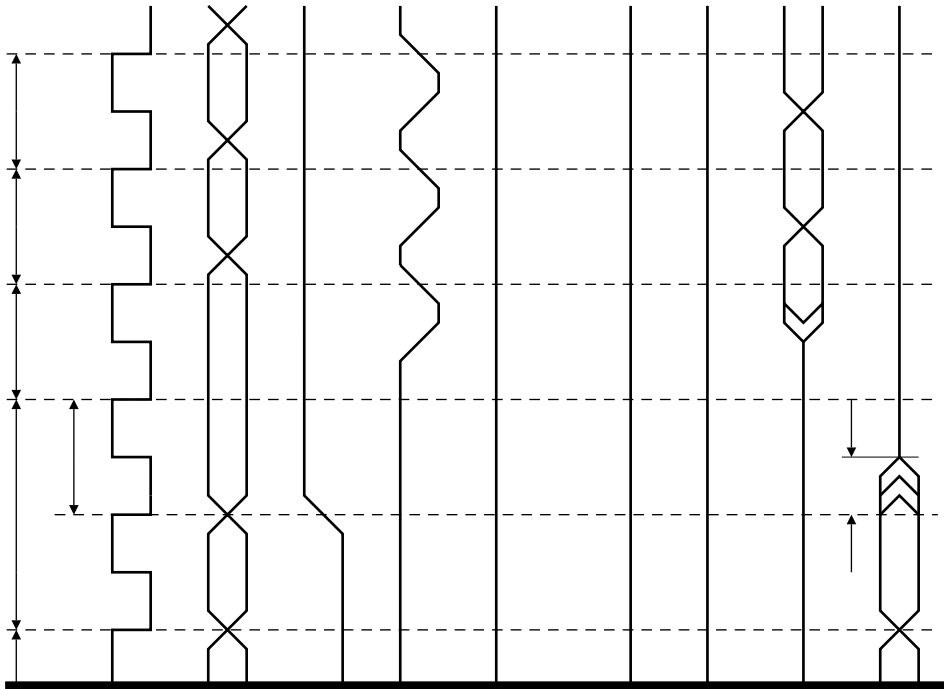
Each chip select can be programmed to insert one or more wait states during an access on the corresponding device. This is done by setting the WSE field in the corresponding EBI_CSR. The number of cycles to insert is programmed in the NWS field in the same register.

Below is the correspondence between the number of standard wait states programmed and the number of cycles during which the NWE pulse is held low:

0 wait states	1/2 cycle
1 wait state	1 cycle

For each additional wait state programmed, an additional cycle is added.

Figure 11-20. Early Read Protocol with t_{DF}



- CSS: Clock Source Selection

0 = The clock source is the Slow Clock.

1 = The clock source is the output of the PLL.

- MUL: Phase Lock Loop Factor