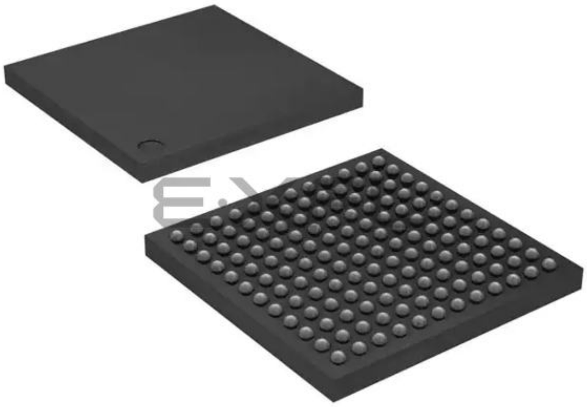
Microchip Technology - AT91M42800A-33CJ Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	33MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	WDT
Number of I/O	54
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-BGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91m42800a-33cj

interrupt request to the ARM7TDMI. It integrates an 8-level priority controller, and, using the Auto-vectoring feature, reduces the interrupt latency time.

The Parallel Input/Output Controllers (PIOA, PIOB) controls up to 54 I/O lines. It enables the user to select specific pins for on-chip peripheral input/output functions, and general-purpose input/output signal pins. The PIO controllers can be programmed to detect an interrupt on a signal change from each line.

There are three embedded system timers. The Real-time Timer (RTT) counts elapsed seconds and can generate periodic or programmed interrupts. The Period Interval Timer (PIT) can be used as a user-programmable time-base, and can generate periodic ticks. The Watchdog (WD) can be used to prevent system lock-up if the software becomes trapped in a deadlock.

The Special Function (SF) module integrates the Chip ID and the Reset Status registers.

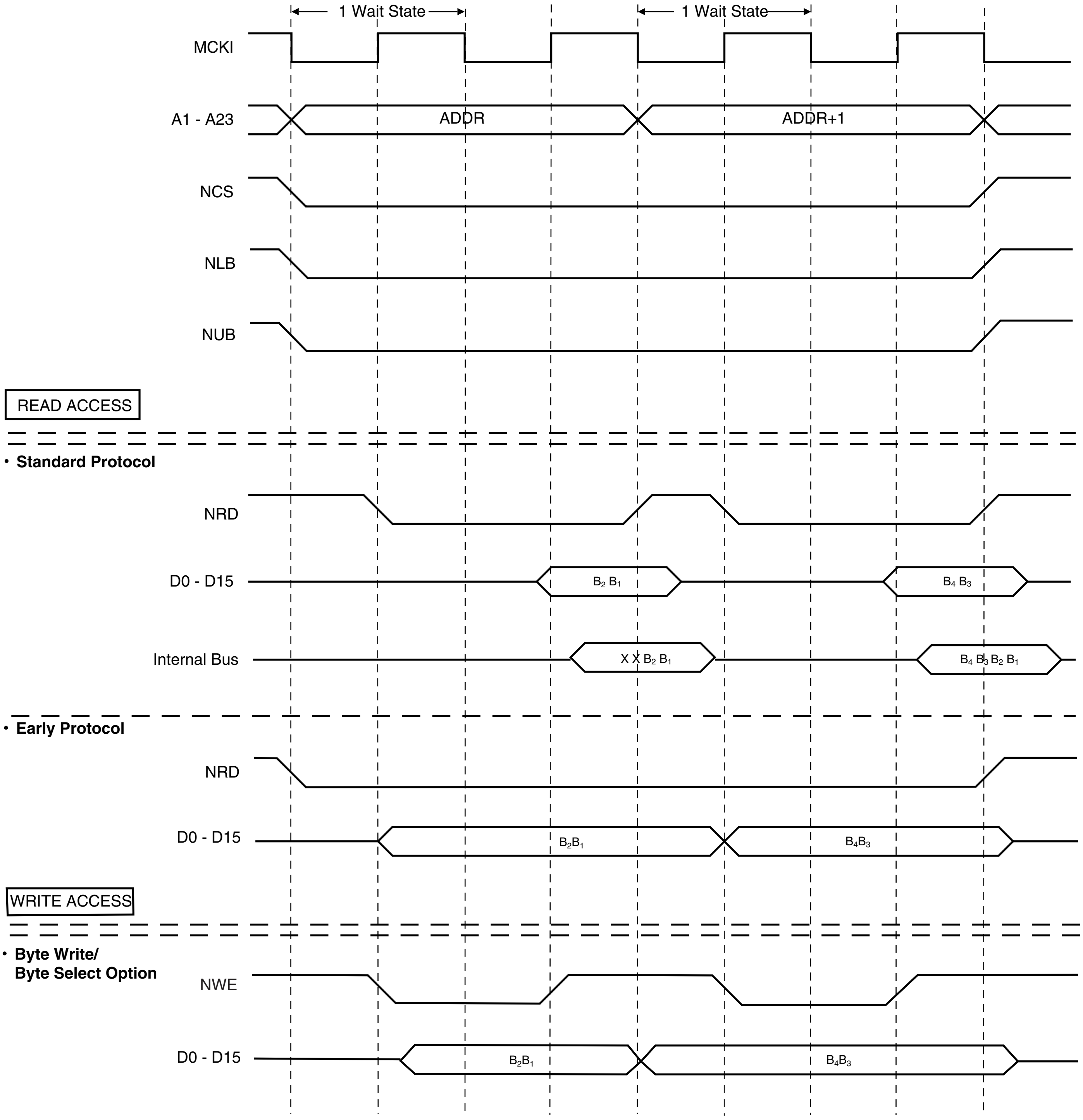
5.2.2 User Peripherals

Two USARTs, independently configurable, enable communication at a high baud rate in synchronous or asynchronous mode. The format includes start, stop and parity bits and up to 9 data bits. Each USART also features a Time-out and a Time-guard register, facilitating the use of the two dedicated Peripheral Data Controller (PDC) channels.

The two 3-channel, 16-bit Timer/Counters (TC) are highly-programmable and support capture or waveform modes. Each TC channel can be programmed to measure or generate different kinds of waves, and can detect and control two input/output signals. Each TC also has three external clock signals.

Two independently configurable SPIs provide communication with external devices in master or slave mode. Each has four external chip selects which can be connected to up to 15 devices. The data length is programmable, from 8- to 16-bit.

Figure 11-22. 1 Wait State, 16-bit Bus Width, Word Transfer



12.10 PMC Peripheral Clock Enable Register

Register Name: PMC_PCER
Access Type: Write-only
Offset: 0x10

31	30	29	28	27	26	25	24
–	–	–	–	—	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	PIOB	PIOA	–	TC5	TC4	TC3	TC2

7	6	5	4	3	2	1	0
TC1	TC0	SPIB	SPIA	US1	US0	–	–

- **Peripheral Clock Enable**

0 = No effect.

1 = Enables the peripheral clock.

12.11 PMC Peripheral Clock Disable Register

Register Name: PMC_PCDR
Access Type: Write-only
Offset: 0x14

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	PIOB	PIOA	–	TC5	TC4	TC3	TC2

7	6	5	4	3	2	1	0
TC1	TC0	SPIB	SPIA	US1	US0	–	–

- **Peripheral Clock Disable**

0 = No effect.

1 = Disables the peripheral clock.

13.11 System Timer Interrupt Disable Register

Register Name: ST_IDR

Access Type: Write-only

Offset: 0x18

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
–	–	–	–	–	–	–	–
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
–	–	–	–	–	–	–	–
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
–	–	–	–	ALMS	RTTINC	WDOVF	PITS

- **PITS: Period Interval Timer Status Interrupt Disable**

0 = No effect.

1 = Disables the Period Interval Timer Status Interrupt.

- **WDOVF: Watchdog Overflow Interrupt Disable**

0 = No effect.

1 = Disables the Watchdog Overflow Interrupt.

- **RTTINC: Real-time Timer Increment Interrupt Disable**

0 = No effect.

1 = Disables the Real-time Timer Increment Interrupt.

- **ALMS: Alarm Status Interrupt Disable**

0 = No effect.

1 = Disables the Alarm Status Interrupt.

14.11 AIC Source Mode Register

Register Name: AIC_SMR0..AIC_SMR31
Access Type: Read/Write
Reset Value: 0

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	SRCTYPE		–	–	PRIOR		

- **PRIOR: Priority Level (Code Label `AIC_PRIOR`)**

Program the priority level for all sources except source 0 (FIQ).

The priority level can be between 0 (lowest) and 7 (highest).

The priority level is not used for the FIQ, in the SMR0.

- **SRCTYPE: Interrupt Source Type (Code Label `AIC_SRCTYPE`)**

Program the input to be positive or negative edge-triggered or positive or negative level sensitive.

The active level or edge is not programmable for the internal sources.

SRCTYPE		External Sources	Code Label
0	0	Low-level Sensitive	AIC_SRCTYPE_EXT_LOW_LEVEL
0	1	Negative Edge triggered	AIC_SRCTYPE_EXT_NEGATIVE_EDGE
1	0	High-level Sensitive	AIC_SRCTYPE_EXT_HIGH_LEVEL
1	1	Positive Edge triggered	AIC_SRCTYPE_EXT_POSITIVE_EDGE

SRCTYPE		Internal Sources	Code Label
X	0	Level Sensitive	AIC_SRCTYPE_INT_LEVEL_SENSITIVE
X	1	Edge triggered	AIC_SRCTYPE_INT_EDGE_TRIGGERED

15.5 Interrupts

Each parallel I/O can be programmed to generate an interrupt when a level change occurs. This is controlled by the PIO_IER (Interrupt Enable) and PIO_IDR (Interrupt Disable) registers which enable/disable the I/O interrupt by setting/clearing the corresponding bit in the PIO_IMR. When a change in level occurs, the corresponding bit in the PIO_ISR (Interrupt Status) is set whether the pin is used as a PIO or a peripheral and whether it is defined as input or output. If the corresponding interrupt in PIO_IMR (Interrupt Mask) is enabled, the PIO interrupt is asserted.

When PIO_ISR is read, the register is automatically cleared.

15.6 User Interface

Each individual I/O is associated with a bit position in the Parallel I/O user interface registers. Each of these registers are 32 bits wide. If a parallel I/O line is not defined, writing to the corresponding bits has no effect. Undefined bits read zero.

15.7 Multi-driver (Open Drain)

Each I/O can be programmed for multi-driver option. This means that the I/O is configured as open drain (can only drive a low level) in order to support external drivers on the same pin. An external pull-up is necessary to guarantee a logic level of one when the pin is not being driven.

Registers PIO_MDER (Multi-Driver Enable) and PIO_MDDR (Multi-Driver Disable) control this option. Multi-driver can be selected whether the I/O pin is controlled by the PIO Controller or the peripheral. PIO_MDSR (Multi-Driver Status) indicates which pins are configured to support external drivers.

15.14 PIO Output Status Register

Register Name: PIO_OSR
Access Type: Read-only
Offset: 0x18
Reset Value: 0

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24

23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16

15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8

7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

This register shows the PIO pin control (output enable) status which is programmed in PIO_OER and PIO ODR. The defined value is effective only if the pin is controlled by the PIO. The register reads as follows:

0 = The corresponding PIO is input on this line.

1 = The corresponding PIO is output on this line.

15.18 PIO Set Output Data Register

Register Name: PIO_SODR
Access Type: Write-only
Offset: 0x30

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

This register is used to set PIO output data. It affects the pin only if the corresponding PIO output line is enabled and if the pin is controlled by the PIO. Otherwise, the information is stored.

0 = No effect.

1 = PIO output data on the corresponding pin is set.

15.19 PIO Clear Output Data Register

Register Name: PIO_CODR
Access Type: Write-only
Offset: 0x34

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

This register is used to clear PIO output data. It affects the pin only if the corresponding PIO output line is enabled and if the pin is controlled by the PIO. Otherwise, the information is stored.

0 = No effect.

1 = PIO output data on the corresponding pin is cleared.

Calculation of time-out duration:

Duration = Value x 4 x Bit Period

17.4 Transmitter

The transmitter has the same behavior in both synchronous and asynchronous operating modes. Start bit, data bits, parity bit and stop bits are serially shifted, lowest significant bit first, on the falling edge of the serial clock. See example in Figure 17-6.

The number of data bits is selected in the CHRL field in US_MR.

The parity bit is set according to the PAR field in US_MR.

The number of stop bits is selected in the NBSTOP field in US_MR.

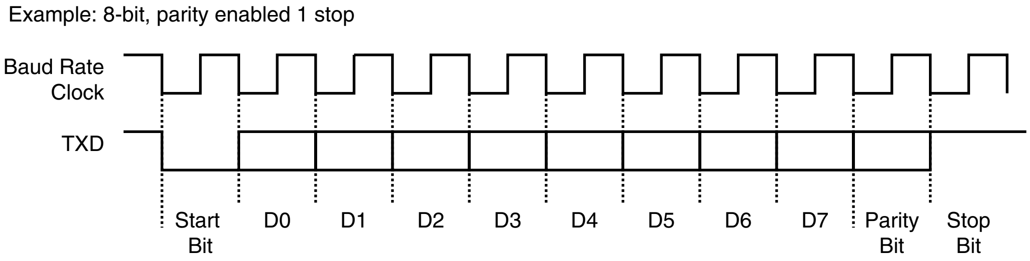
When a character is written to US_THR (Transmit Holding), it is transferred to the Shift Register as soon as it is empty. When the transfer occurs, the TXRDY bit in US_CSR is set until a new character is written to US_THR. If Transmit Shift Register and US_THR are both empty, the TXEMPTY bit in US_CSR is set.

17.4.1 Time-guard

The Time-guard function allows the transmitter to insert an idle state on the TXD line between two characters. The duration of the idle state is programmed in US_TTGR (Transmitter Time-guard). When this register is set to zero, no time-guard is generated. Otherwise, the transmitter holds a high level on TXD after each transmitted byte during the number of bit periods programmed in US_TTGR.

$$\text{Idle state duration between two characters} = \text{Time-guard Value} \times \text{Bit Period}$$

Figure 17-6. Synchronous and Asynchronous Modes: Character Transmission



17.5 Multi-drop Mode

When the field PAR in US_MR equals 11X (binary value), the USART is configured to run in Multi-drop mode. In this case, the parity error bit PARE in US_CSR is set when data is detected with a parity bit set to identify an address byte. PARE is cleared with the Reset Status Bits Command (RSTSTA) in US_CR. If the parity bit is detected low, identifying a data byte, PARE is not set.

The transmitter sends an address byte (parity bit set) when a Send Address Command (SENDA) is written to US_CR. In this case, the next byte written to US_THR will be transmitted as an address. After this any byte transmitted will have the parity bit cleared.

17.12 USART Mode Register

Name: US_MR

18.6 TC Block Control Register

Register Name: TC_BCR

Access Type: Write-only

Offset: 0xC0

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
–	–	–	–	–	–	–	–
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
–	–	–	–	–	–	–	–
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
–	–	–	–	–	–	–	SYNC

- **SYNC: Synchro Command (Code Label `TC_SYNC`)**

0 = No effect.

1 = Asserts the SYNC signal which generates a software trigger simultaneously for each of the channels.

18.7 TC Block Mode Register

Register Name: TC_BMR

Access Type: Read/Write

Offset: 0xC4

Reset Value: 0x0

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	TC2XC2S		TC1XC1S		TC0XC0S	

- **TC0XC0S: External Clock Signal 0 Selection**

TC0XC0S		Signal Connected to XC0	Code Label: `TC_TC0XC0S`
0	0	TCLK0	`TC_TCLK0XC0`
0	1	None	`TC_NONEXC0`
1	0	TIOA1	`TC_TIOA1XC0`
1	1	TIOA2	`TC_TIOA2XC0`

- **TC1XC1S: External Clock Signal 1 Selection**

TC1XC1S		Signal Connected to XC1	Code Label: `TC_TC1XC1S`
0	0	TCLK1	`TC_TCLK1XC1`
0	1	None	`TC_NONEXC1`
1	0	TIOA0	`TC_TIOA0XC1`
1	1	TIOA2	`TC_TIOA2XC1`

- **TC2XC2S: External Clock Signal 2 Selection**

TC2XC2S		Signal Connected to XC2	Code Label: `TC_TC2XC2S`
0	0	TCLK2	`TC_TCLK2XC2`
0	1	None	`TC_NONEXC2`
1	0	TIOA0	`TC_TIOA0XC2`
1	1	TIOA1	`TC_TIOA1XC2`

18.8 TC Channel Control Register

Register Name: TC_CCR

Access Type: Write-only

Offset: 0x00

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	–	–	SWTRG	CLKDIS	CLKEN

- **CLKEN: Counter Clock Enable Command (Code Label `TC_CLKEN`)**

0 = No effect.

1 = Enables the clock if CLKDIS is not 1.

- **CLKDIS: Counter Clock Disable Command (Code Label `TC_CLKDIS`)**

0 = No effect.

1 = Disables the clock.

- **SWTRG: Software Trigger Command (Code Label `TC_SWTRG`)**

0 = No effect.

1 = A software trigger is performed: the counter is reset and clock is started.

18.12 TC Register A

Register Name: TC_RA

Access Type: Read-only if WAVE = 0, Read/Write if WAVE = 1

Offset: 0x14

Reset Value: 0x0

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

<table><tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th></tr><tr><td colspan="8">RA</td></tr></table>

<table><tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr><tr><td colspan="8">RA</td></tr></table>

- **RA: Register A (Code Label `TC_RA`)**

RA contains the Register A value in real time.

18.13 TC Register B

Register Name: TC_RB

Access Type: Read-only if WAVE = 0, Read/Write if WAVE = 1

Offset: 0x18

Reset Value: 0x0

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

<table><tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th></tr><tr><td colspan="8">RB</td></tr></table>

<table><tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr><tr><td colspan="8">RB</td></tr></table>

- **RB: Register B (Code Label `TC_RB`)**

RB contains the Register B value in real time.

19.16 SPI Receive Pointer Register

Name: SP_RPR

Access Type: Read/Write

Offset: 0x20

Reset Value: 0x0

31	30	29	28	27	26	25	24
RXPTR							
23	22	21	20	19	18	17	16
RXPTR							
15	14	13	12	11	10	9	8
RXPTR							
7	6	5	4	3	2	1	0
RXPTR							

- **RXPTR: Receive Pointer**

RXPTR must be loaded with the address of the receive buffer.

19.17 SPI Receive Counter Register

Name: SP_RCR

Access Type: Read/Write

Offset: 0x24

Reset Value: 0x0

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
RXCTR							
7	6	5	4	3	2	1	0
RXCTR							

- **RXCTR: Receive Counter**

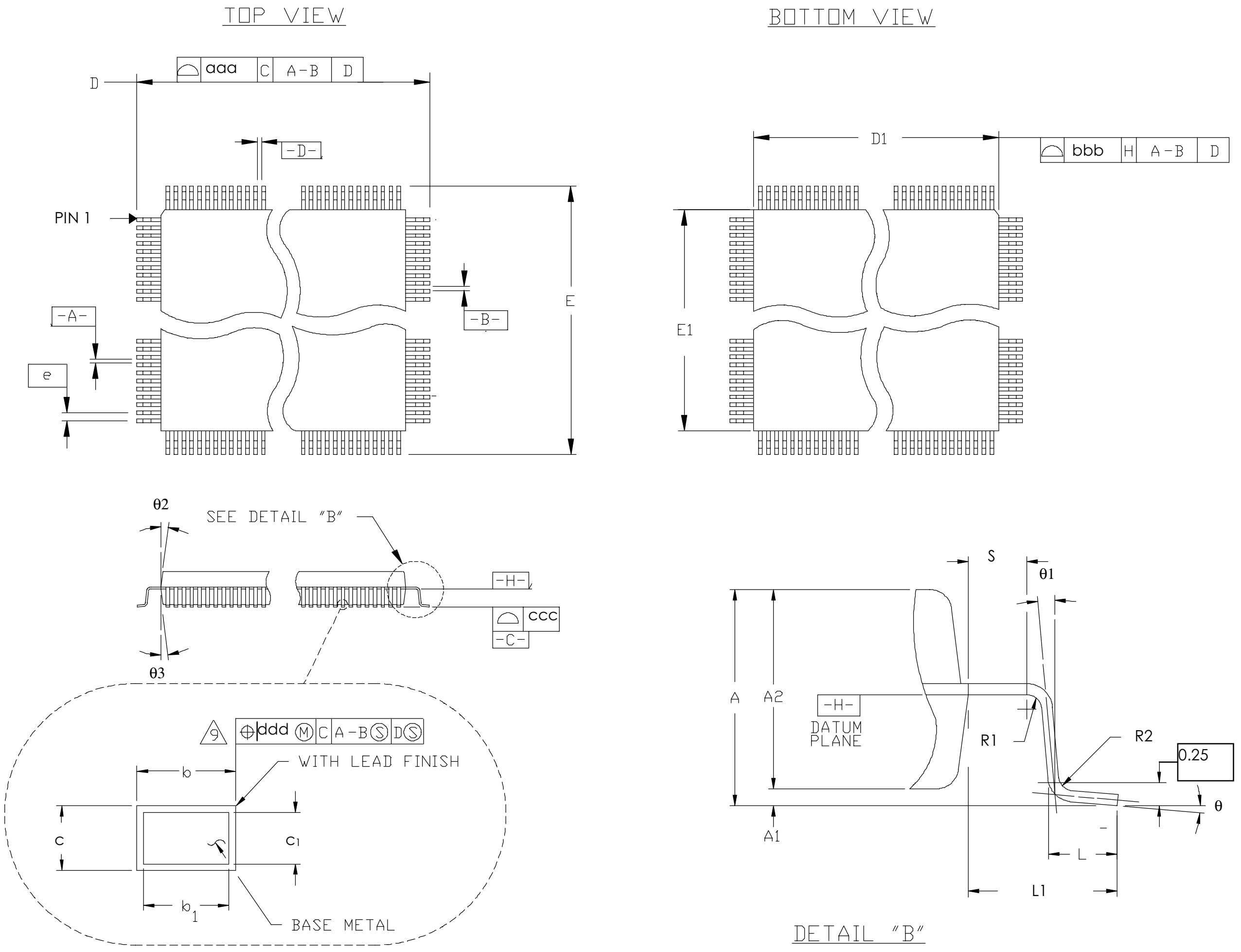
RXCTR must be loaded with the size of the receive buffer.

0: Stop Peripheral Data Transfer dedicated to the receiver.

1-65535: Start Peripheral Data transfer if RDRF is active.

21. Packaging Information

Figure 21-1. 144-lead LQFP Package Drawing



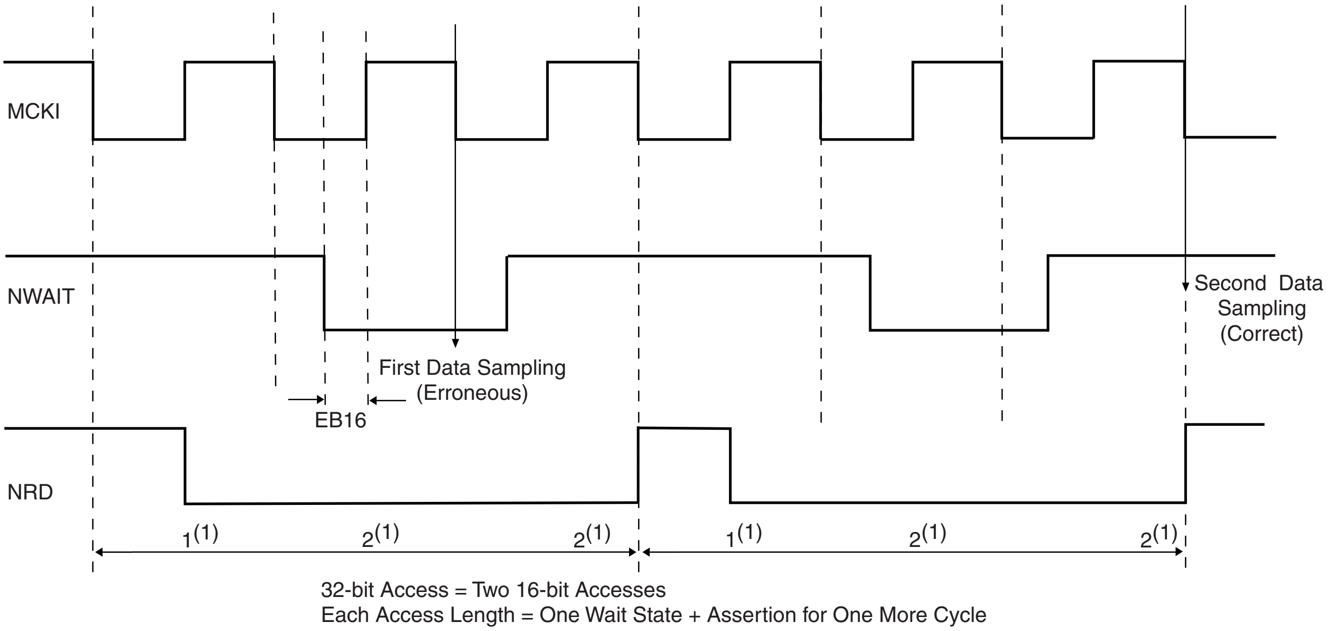
23. Ordering Information

Table 23-1. Ordering Information

Ordering Code	Package	Package Type	Operating Temperature Range
AT91M42800A-33CJ	BGA 144	RoHS-compliant	Industrial (-40° C to 85° C)
AT91M42800A-33AU	LQFP 144	Green	

If the first two conditions are not met during a 32-bit read access, the first 16-bit data is read at the end of the standard 16-bit read access. In the following example, the number of standard waits is one. NWAIT assertions do affect both NRD pulse lengths, but first data sampling is not delayed. The second data sampling is correct.

Figure 24-3. Number of Standard Wait States is One


MCKI
NWAIT
NRD
First Data Sampling (Erroneous)
EB16
Second Data Sampling (Correct)
1(1)
2(1)
2(1)
1(1)
2(1)
2(1)
32-bit Access = Two 16-bit Accesses
Each Access Length = One Wait State + Assertion for One More Cycle

Note: 1. These numbers refer to the standard access cycles.

If the first two conditions are not met during write accesses, the NWE signal is not affected by the NWAIT assertion. The following example illustrates the number of standard wait states. NWAIT is not asserted during the first cycle, but is asserted at the second and last cycle of the standard access. The access is correctly delayed as the NCS line rises accordingly to the NWAIT assertion. However, the NWE signal waveform is unchanged, and rises too early.

Problem Fix/Workaround

The user must use the Time Guard programmed at the value 12.

24.6 SCK is Ignored at 32 kHz

If the origin of the Master Clock is the Slow Clock, the USART Channels cannot be synchronized with a clock that comes from the SCK pin.

Problem Fix/Workaround

No problem fix/workaround to propose.

24.7 SCK Maximum Frequency Relative to MCK in Synchronous Mode

In USART Synchronous Mode, the external clock frequency (SCK) must be at least 10 times lower than the Master Clock.

Problem Fix/Workaround

No problem fix/workaround to propose.

24.8 PIO Input Filters are not Bit-to-bit Selectable

The PIO input filters are enabled and disabled only for all of the PIO input pins and not individually. To activate them, the user must write 0x0001 in the PIO IFER and 0x0001 in the PIO IFDR to deactivate them.

Problem Fix/Workaround

No problem fix/workaround to propose.

24.9 PIO Multi-drive Capability not Usable

The PIO multi-drive capability does not work in PIO mode or in peripheral mode.

Problem Fix/Workaround

No practical workaround proposed.