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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	2304
Total RAM Bits	18432
Number of I/O	289
Number of Gates	50000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C
Package / Case	352-LBGA
Supplier Device Package	352-SBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at40k40lv-3bgc

Description

The AT40K is a family of fully PCI-compliant, SRAM-based FPGAs with distributed 10ns programmable synchronous/asynchronous, dual port/single port SRAM, 8 global clocks, Cache Logic ability (partially or fully reconfigurable without loss of data), automatic component generators, and range in size from 5,000 to 50,000 usable gates. I/O counts range from 128 to 384 in industry standard packages ranging from 84-pin PLCC to 475-pin BGA, and support 3.3V and 5V designs.

The AT40K is designed to quickly implement high performance, large gate count designs through the use of synthesis and schematic-based tools used on a PC, Sun and HP platform. Atmel's design tools provide seamless integration with industry standard tools from Cadence (Concept/Verilog), Everest, Exemplar, Mentor, OrCAD, Synario, Veribest, and Viewlogic.

The AT40K can be used as a Coprocessor for high speed (DSP/Processor-based) designs by implementing a variety of compute-intensive, arithmetic functions. These include adaptive finite impulse response (FIR) filters, fast Fourier transforms (FFT), convolvers, interpolators and discrete-cosine transforms (DCT) that are required for video compression and decompression, encryption, convolution and other multimedia applications.

Fast, Flexible and Efficient SRAM

The AT40K FPGA offers a patented distributed 10ns SRAM capability where the RAM can be used without losing logic resources. Multiple independent, synchronous or asynchronous, dual port or single port RAM functions (FIFO, scratch pad, etc.) can be created using Atmel's macro generator tool.

Fast, Efficient Array & Vector Multipliers

The AT40K's patented 8-sided core cell with direct horizontal, vertical and diagonal cell-to-cell connections implements ultra fast array multipliers without using any busing resources. The AT40K's Cache Logic capability enables a large number of design coefficients and variables to be implemented in a very small amount of silicon, enabling vast improvement in system speed at much lower cost than conventional FPGAs.

Cache Logic Design

The AT40K is the only FPGA family capable of implementing Cache Logic (Dynamic full/partial logic reconfiguration, without loss of data, on-the-fly) for building adaptive logic and systems. As new logic functions are required, they can be loaded into the logic cache without losing the data already there or disrupting the operation of the rest of the chip; replacing or complementing the active logic. The AT40K can act as a reconfigurable coprocessor.

Automatic Component Generators

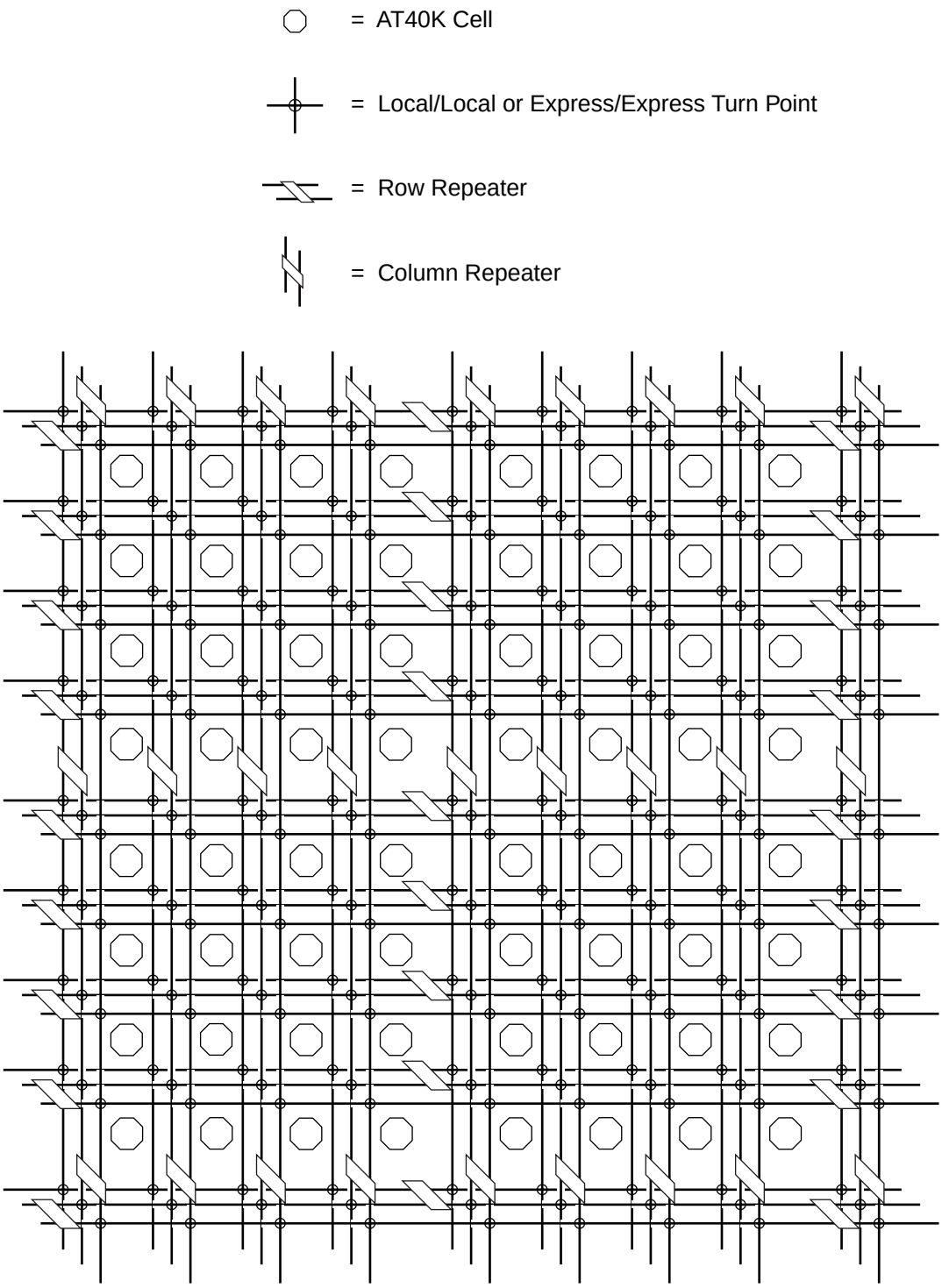
The AT40K is the only FPGA family capable of implementing user-defined, automatically generated, macros in multiple designs; speed and functionality are unaffected by the macro orientation or density of the target device. This enables the fastest, most predictable and efficient FPGA design approach and minimizes design risk by reusing already proven functions. The Automatic Component Generators work seamlessly with industry standard schematic and synthesis tools to create the fastest, most efficient designs available.

The patent-pending AT40K Series architecture employs a symmetrical grid of small yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices range in size from 5,000 to 50,000 usable gates in the initial family, and 256 to 2,304 registers. Pin locations are consistent throughout the AT40K Series for easy design migration in the same package footprint. AT40K Series FPGAs utilize a reliable 0.6 micron single-poly, triple-metal CMOS process and are 100% factory-tested. Atmel's PC- and workstation-based Integrated Development System is used to create AT40K Series designs. Multiple design entry methods are supported.

The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, efficient and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances

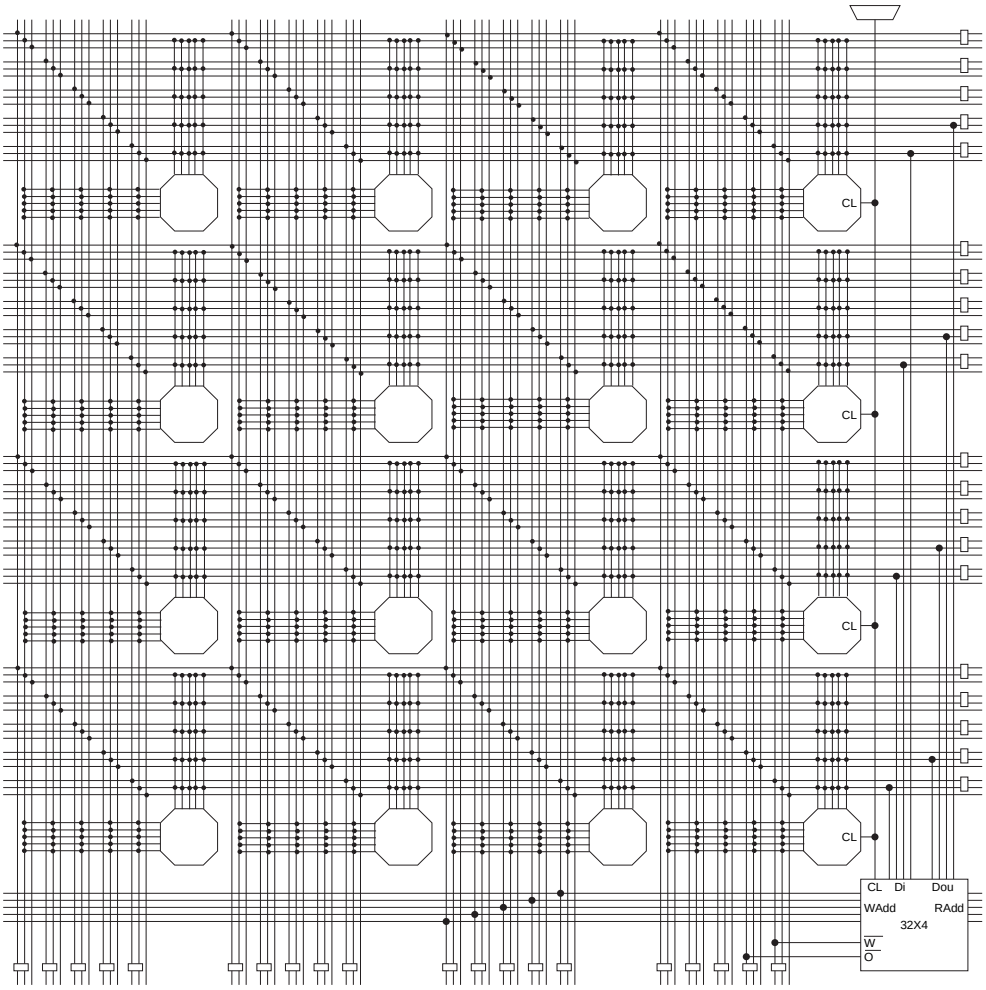
Figure 3. Busing Plane (one of five)



RAM

32 x 4 Dual-Ported RAM blocks are dispersed throughout the array as shown in Figure 7. A four-bit Input Data Bus connects to four horizontal local buses distributed over four sector rows (plane 1). A four-bit Output Data Bus connects to four horizontal local buses distributed over four sector rows (plane 2). A five-bit Input-Address Bus connects to five vertical express buses in same column. A five-bit Output-Address Bus connects to five vertical express buses in same column. WAddr (Write Address) and RAddr (Read Address) alternate positions in horizontally aligned RAM blocks. For the left-most RAM blocks, RAddr is on the left and WAddr is on the right. For the right-most RAM blocks, WAddr is on the left and RAddr is tied off. For single-ported RAM, WAddr is the READ/WRITE address port and Din is the (bi-directional) data port. Right-most RAM blocks can be used only for single-ported memories. /WE & /OE connect to the vertical express buses in the same column. WAddr, RAddr, /WE and /OE connect to express buses that are full length at array edge.

Figure 7. RAM Connections (One Ram Block)

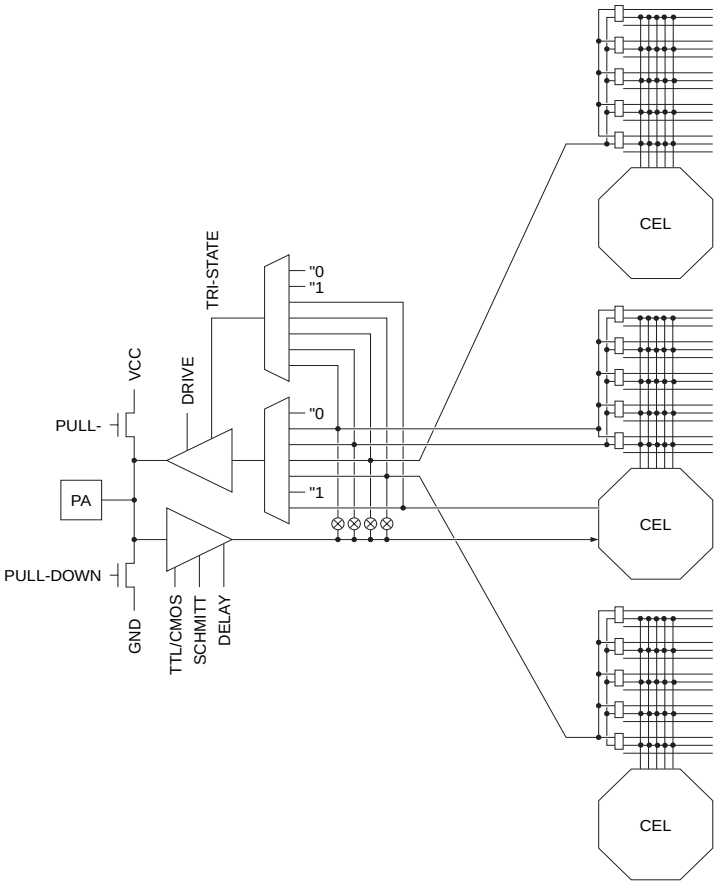


Clocking and Set/Reset

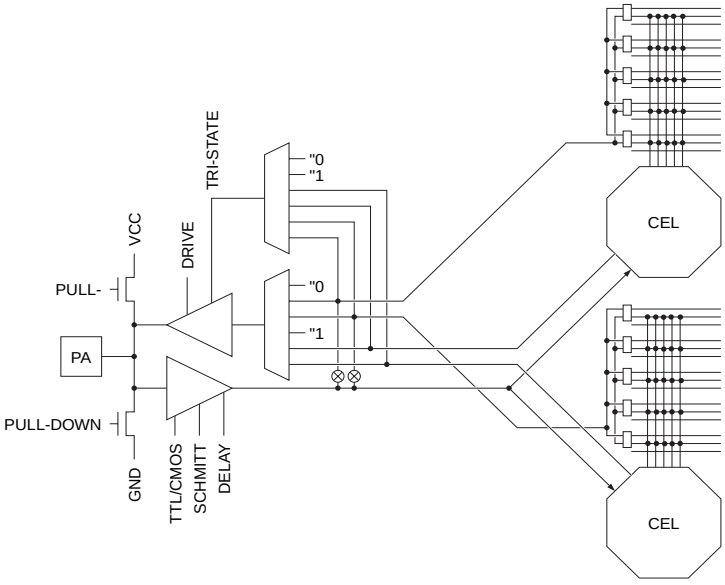
Each of 8 dedicated Global Clock buses is connected to a dual-use Global Clock pad (GCK1 - GCK8). An internal signal can be placed on a Global Clock bus by routing that signal to a Global Clock pad. Each column of the array has a Column Clock selected from one of the 8 Global Clock buses. The extreme-left Column Clock mux has two additional inputs from dual-use pins FCK1 & FCK2 to provide fast clocking to left-side I/O. The extreme-right Column Clock mux has two additional inputs from dual-use pins FCK3 & FCK4 to provide fast clocking to right-side I/O. Each sector column of 4 cells can be clocked from a (Plane 4) express bus or from the Column Clock. Clocking to the 4 cells can be disabled. The Plane 4 express bus used for clocking is half length at the array edge. The clock provided to each sector column of 4 cells can be either inverted or not inverted. The register in each cell is triggered on a rising clock edge. On power up, constant “0” is provided to each registers clock pins.

A dedicated Global Set/Reset bus can be driven by any USER I/O pad, except those used for clocking, Global or Fast. An internal signal can be placed on the Global Set/Reset bus by routing that signal to the pad programmed as the Global Set/Reset input. Global Set/Reset is distributed to each column of the array. Each sector column of 4 cells can be Set/Reset by a (Plane 5) express bus or by the Global Set/Reset. The Plane 5 express bus used for Set/Reset is half length at array edge. The Set/Reset provided to each sector column of 4 cells can be either inverted or not inverted. The function of the Set/Reset input of a register (either Set or Reset) is determined by a configuration bit in each cell. The Set/Reset input of a register is Active Low (logic 0). Setting or resetting of a register is asynchronous. On power up, a logic 1 (a high) is provided by each register, i.e., all registers are set at power up.

Figure 12. West I/O (Mirrored for East I /O)

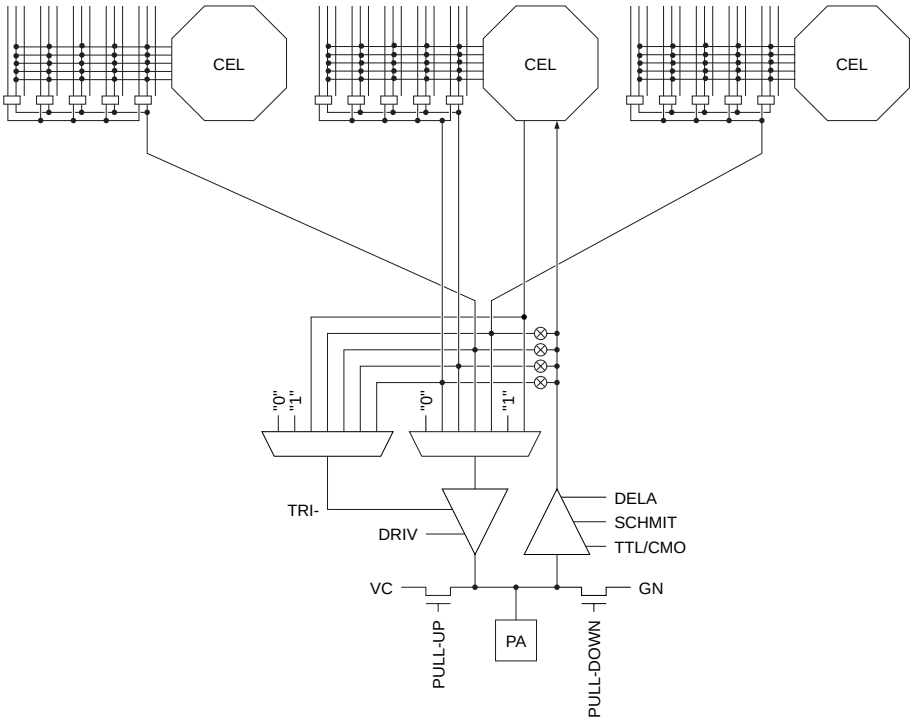


(a) Primary

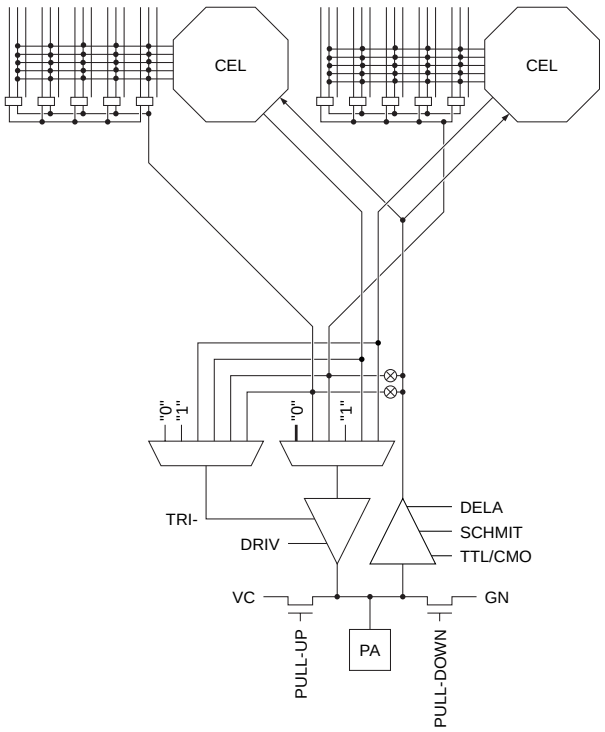


(a) Secondary

Figure 13. South I/O (Mirrored for North I/O)

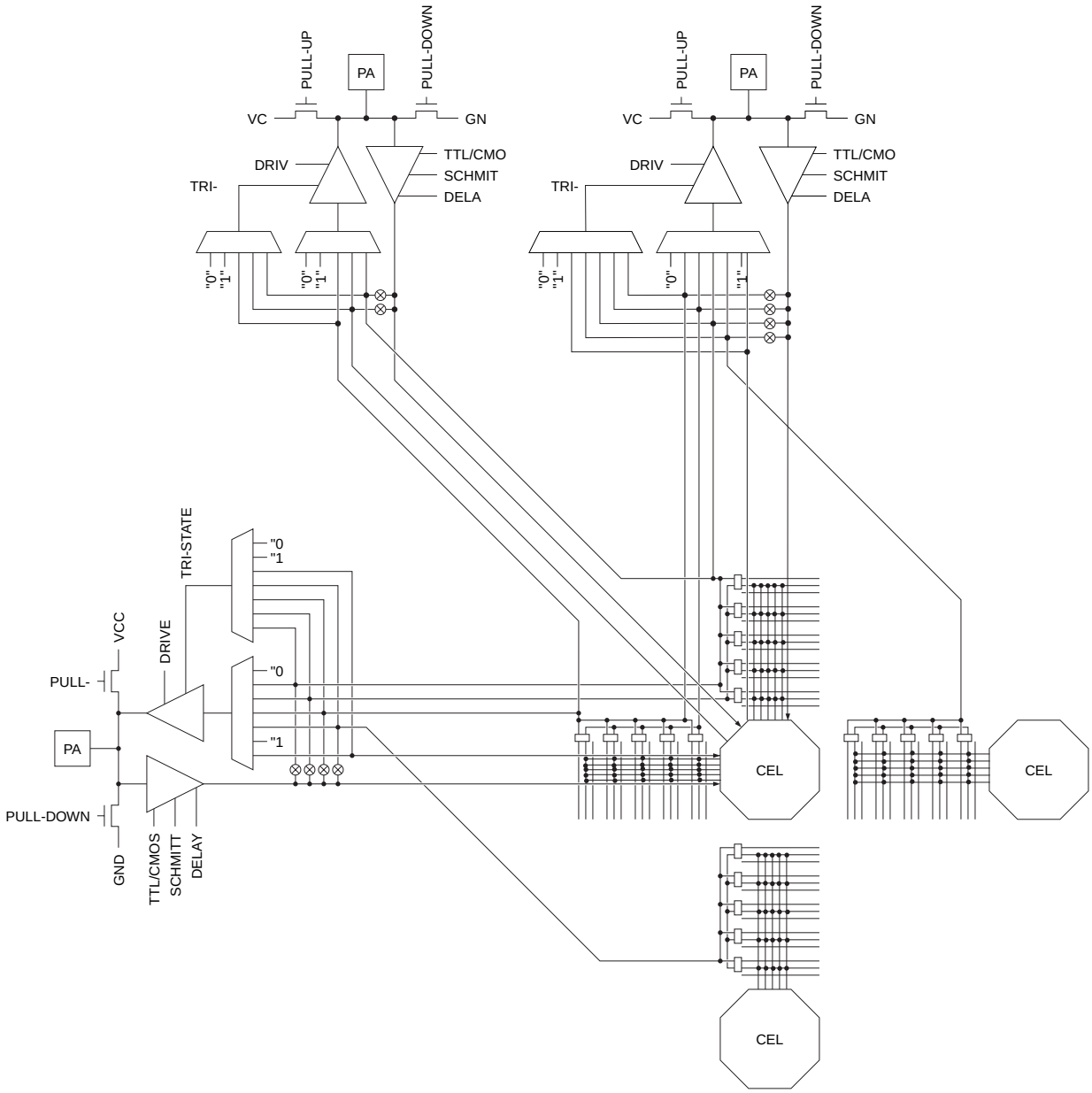


(a) Primary



(a) Secondary

Figure 14. North/West Corner, (similar for NE/SE/SW corners)



AC Timing Characteristics - 5V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Max delays are the average of t_{PDLH} and t_{PDHL}.

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_C.
All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{CC}.

Cell Function	Parameter	Path	-2	Units	Notes
Repeaters					
Repeater	t_{PD}(max)	L->E	1.3	ns	1 unit load
Repeater	t_{PD}(max)	E->E	1.3	ns	1 unit load
Repeater	t_{PD}(max)	L->L	1.3	ns	1 unit load
Repeater	t_{PD}(max)	E->L	1.3	ns	1 unit load
Repeater	t_{PD}(max)	E->IO	0.8	ns	1 unit load
Repeater	t_{PD}(max)	L->IO	0.8	ns	1 unit load

All input IO characteristics measured from a V_{IH} of 50% at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{CC}.
All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{CC}.

Cell Function	Parameter	Path	-2	Units	Notes
IO					
Input	t_{PD}(max)	pad -> x/y	1.2	ns	no extra delay
Input	t_{PD}(max)	pad -> x/y	3.6	ns	1 extra delay
Input	t_{PD}(max)	pad -> x/y	7.3	ns	2 extra delays
Input	t_{PD}(max)	pad -> x/y	10.8	ns	3 extra delays
Output, slow	t_{PD}(max)	x/y/E/L -> pad	5.9	ns	50pf load
Output, medium	t_{PD}(max)	x/y/E/L -> pad	4.8	ns	50pf load
Output, fast	t_{PD}(max)	x/y/E/L -> pad	3.9	ns	50pf load
Output, slow	t_{PZX}(max)	oe -> pad	6.2	ns	50pf load
Output, low	t_{PXZ}(max)	oe -> pad	1.3	ns	50pf load
Output, medium	t_{PZX}(max)	oe -> pad	4.8	ns	50pf load
Output, medium	t_{PXZ}(max)	oe -> pad	1.9	ns	50pf load
Output, fast	t_{PZX}(max)	oe -> pad	3.7	ns	50pf load
Output, fast	t_{PXZ}(max)	oe -> pad	1.6	ns	50pf load

Absolute Maximum Ratings - 3.3V Commercial/Industrial*

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Supply Voltage	With respect to GND	-0.5	7.0	V
V_I	DC Input Voltage(1)	With respect ot GND	-0.5	7.0	V
V_O	DC Output Voltaage	With respect ot GND	-0.5	7.0	V
T_{STG}	Storage Temperature		-65°C	+150°C	
T_J	Junction Temperature			+150°C	
T_L	Lead Temperature (Soldering, 10 sec.)			+250°C	
ESD		R_{ZAP} = 1.5K, C_{ZAP} = 100 pF		2000	V

Note: 1. Minimum voltage of -0.5V DC which may undershoot to -2.0V for pulses of less than 20 ns.

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range - 3.3V Operation

		AT40K05LV-4/3/2 AT40K10LV-4/3/2 AT40K20LV-4/3/2 AT40K40LV-4/3/2 Commercial	**AT40K05LV-4/3/2 AT40K10LV-4/3/2 AT40K20LV-4/3/2 AT40K40LV-4/3/2 Industrial**
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply		3.3V ± 0.3V	3.3V ± 0.3V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% V_{CC}

AC Timing Characteristics - 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C
Max delays are the average of t_{PDLH} and t_{PDHL}.

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-3	Units	Notes
Repeaters					
Repeater	t_{PD}(max)	L -> E	2.2	ns	1 unit load
Repeater	t_{PD}(max)	E -> E	2.2	ns	1 unit load
Repeater	t_{PD}(max)	L -> L	2.2	ns	1 unit load
Repeater	t_{PD}(max)	E -> L	2.2	ns	1 unit load
Repeater	t_{PD}(max)	E -> IO	1.4	ns	1 unit load
Repeater	t_{PD}(max)	L -> IO	1.4	ns	1 unit load

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-3	Units	Notes
IO					
Input	t_{PD}(max)	pad -> x/y	1.9	ns	no extra delay
Input	t_{PD}(max)	pad -> x/y	5.8	ns	1 extra delay
Input	t_{PD}(max)	pad -> x/y	11.5	ns	2 extra delays
Input	t_{PD}(max)	pad -> x/y	17.4	ns	3 extra delays
Output, slow	t_{PD}(max)	x/y/E/L -> pad	9.1	ns	50pf load
Output, medium	t_{PD}(max)	x/y/E/L -> pad	7.6	ns	50pf load
Output, fast	t_{PD}(max)	x/y/E/L -> pad	6.2	ns	50pf load
Output, slow	t_{PZX}(max)	oe -> pad	9.5	ns	50pf load
Output, slow	t_{PXZ}(max)	oe -> pad	2.1	ns	50pf load
Output, medium	t_{PZX}(max)	oe -> pad	7.4	ns	50pf load
Output, medium	t_{PXZ}(max)	oe -> pad	2.7	ns	50pf load
Output, fast	t_{PZX}(max)	oe -> pad	5.9	ns	50pf load
Output, fast	t_{PXZ}(max)	oe -> pad	2.4	ns	50pf load

AT40K05	AT40K10	AT40K20	AT40K40	Left Side (Top to Bottom)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
	I/O18	I/O22	I/O30							F1	21	279	J25	L30
			GND											GND*
			I/O31											M30
			I/O32											M28
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
			I/O33										J26	M29
			I/O34										L23	M31
		I/O23	I/O35									278	L24	N31
		I/O24	I/O36									277	K25	N28
		GND	GND								22		GND(1)	GND(1)
			VCC										VCC(1)	VCC(1)
			I/O37											N29
			I/O38											N30
		I/O25	I/O39									276	L25	P30
		I/O26	I/O40									275	L26	P28
	I/O19	I/O27	I/O41						19	G4	23	274	M23	P29
	I/O20	I/O28	I/O42						20	G3	24	273	M24	R31
			GND											GND(1)
I/O13	I/O21	I/O29	I/O43				13	15	21	G2	25	272	M25	R30
I/O14	I/O22	I/O30	I/O44		11	8	14	16	22	G1	26	271	M26	R28
			I/O45											
			I/O46											
I/O15 (A22)	I/O23 (A22)	I/O31 (A22)	I/O47 (A22)	19	12	9	15	17	23	G5	27	270	N24	R29
I/O16 (A23)	I/O24 (A23)	I/O32 (A23)	I/O48 (A23)	20	13	10	16	18	24	H3	28	269	N25	T31
GND	GND	GND	GND	21	14	11	17	19	25	GND(1)	29	268	GND(1)	GND(1)
VCC	VCC	VCC	VCC	22	15	12	18	20	26	VCC(1)	30	267	VCC(1)	VCC(1)
I/O17	I/O25	I/O33	I/O49	23	16	13	19	21	27	H4	31	266	N26	T30
I/O18	I/O26	I/O34	I/O50	24	17	14	20	22	28	H5	32	265	P25	T29
			I/O51											
			I/O52											
I/O19	I/O27	I/O35	I/O53		18	15	21	23	29	J2	33	264	P23	U31
I/O20	I/O28	I/O36	I/O54				22	24	30	J1	34	263	P24	U30
			GND											GND(1)
	I/O29	I/O37	I/O55						31	J3	35	262	R26	U28
	I/O30	I/O38	I/O56						32	J4	36	261	R25	U29
		I/O39	I/O57									260	R24	V30
		I/O40	I/O58									259	R23	V29
			I/O59											V28
			I/O60											W31
			VCC										VCC(1)	VCC(1)
		GND	GND								37		GND(1)	GND(1)
		I/O41	I/O61									258	T26	W30
		I/O42	I/O62									257	T25	W29

Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

AT40K05	AT40K10	AT40K20	AT40K40	Bottom Side (Left to Right)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
			I/O186										AC6	AL4
			GND											GND(1)
			I/O187											AH6
			I/O188											AJ5
I/O61	I/O93	I/O125	I/O189				67	75	97	P13	115	158	AD5	AK4
I/O62	I/O94	I/O126	I/O190				68	76	98	K10	116	157	AE3	AH5
I/O63 (D8)	I/O95 (D8)	I/O127 (D8)	I/O191 (D8)	50	50	47	69	77	99	R14	117	156	AD4	AK3
I/O64, GCK4	I/O96, GCK4	I/O128, GCK4	I/O192 ,GCK4	51	51	48	70	78	100	N13	118	155	AC5	AJ4
GND	GND	GND	GND	52	52	49	71	79	101	GND(1)	119	154	GND(1)	GND(1)
/CON	/CON	/CON	/CON	53	53	50	72	80	103	P14	120	153	AD3	AH4

AT40K05	AT40K10	AT40K20	AT40K40	Right Side (Bottom to Top)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
VCC	VCC	VCC	VCC	54	54	51	73	81	106	VCC(1)	121	152	VCC(1)	VCC(1)
/RESET	/RESET	/RESET	/RESET	55	55	52	74	82	108	M12	122	151	AC4	AH3
I/O65 (D7)	I/O97 (D7)	I/O129 (D7)	I/O193 (D7)	56	56	53	75	83	109	P15	123	150	AD2	AJ2
I/O66, GCK5	I/O98, GCK5	I/O130, GCK5	I/O194, GCK5	57	57	54	76	84	110	N14	124	149	AC3	AG4
I/O67	I/O99	I/O131	I/O195				77	85	111	L11	125	148	AB4	AG3
I/O68	I/O100	I/O132	I/O196				78	86	112	M13	126	147	AD1	AH2
			I/O197										AB3	AH1
			I/O198										AC2	AF4
			GND											GND(1)
	I/O101	I/O133	I/O199							N15	127	146	AA4	AF3
	I/O102	I/O134	I/O200							M14	128	145	AA3	AG2
			I/O201											AG1
			I/O202											AE4
		I/O135	I/O203									144	AB2	AE3
		I/O136	I/O204									143	AC1	AF2
		VCC	VCC										VCC(1)	VCC(1)
		GND	GND										GND(1)	GND(1)
I/O69 (D6)	I/O103 (D6)	I/O137 (D6)	I/O205 (D6)	58	58	55	79	87	113	J10	129	142	Y3	AF1
I/O70	I/O104	I/O138	I/O206		59	56	80	88	114	L12	130	141	AA2	AD4
I/O71	I/O105	I/O139	I/O207					89	115	M15	131	140	AA1	AD3
I/O72	I/O106	I/O140	I/O208					90	116	L13	132	139	W4	AE2
			I/O209											AD2
			I/O210											AC4
														VCC(1)
			GND											GND(1)

Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

AT40K05	AT40K10	AT40K20	AT40K40	Right Side (Bottom to Top)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
			I/O211											
			I/O212											
	I/O107	I/O141	I/O213						117	L14	133	138	W3	AC3
	I/O108	I/O142	I/O214						118	K11	134	137	Y2	AD1
		I/O143	I/O215									136	Y1	AC2
		I/O144	I/O216									135	V4	AB4
GND	GND	GND	GND				81	91	119	GND(1)	135	134	GND(1)	GND(1)
	I/O109	I/O145	I/O217							L15	136	133	V3	AB3
	I/O110	I/O146	I/O218							K12	137	132	W2	AB2
I/O73, FCK3	I/O111, FCK3	I/O147, FCK3	I/O219, FCK3				82	92	120	K13	138	131	U4	AB1
I/O74	I/O112	I/O148	I/O220				83	93	121	K14	139	130	U3	AA3
	VCC	VCC	VCC							VCC(1)	140	129	VCC(1)	VCC(1)
I/O75 (D5)	I/O113 (D5)	I/O149 (D5)	I/O221 (D5)	59	60	57	84	94	122	K15	141	127	V2	AA2
I/O76 (CS0)	I/O114 (CS0)	I/O150 (CS0)	I/O222 (CS0)	60	61	58	85	95	123	J12	142	126	V1	Y2
			GND											GND(1)
			I/O223										T4	Y4
			I/O224										T3	Y3
			I/O225											Y1
			I/O226											W1
		I/O151	I/O227									125	U2	W4
		I/O152	I/O228									124	T2	W3
		GND	GND								143		GND(1)	GND(1)
			VCC										VCC(1)	VCC(1)
			I/O229											W2
			I/O230											V2
		I/O153	I/O231									123	T1	V4
		I/O154	I/O232									122	R4	V3
	I/O115	I/O155	I/O233						124	J13	144	121	R3	U1
	I/O116	I/O156	I/O234						125	J14	145	120	R2	U2
			GND											GND(1)
I/O77	I/O117	I/O157	I/O235		62	59	86	96	126	J15	146	119	R1	U4
I/O78	I/O118	I/O158	I/O236		63	60	87	97	127	J11	147	118	P3	U3
			I/O237											
			I/O238											
I/O79(D4)	I/O119(D4)	I/O159(D4)	I/O239(D4)	61	64	61	88	98	128	H13	148	117	P2	T1
I/O80	I/O120	I/O160	I/O240	62	65	62	89	99	129	H14	149	116	P1	T2
VCC	VCC	VCC	VCC	63	66	63	90	100	130	VCC(1)	150	115	VCC(1)	VCC(1)
GND	GND	GND	GND	64	67	64	91	101	131	GND(1)	151	114	GND(1)	GND(1)
I/O81 (D3)	I/O121 (D3)	I/O161 (D3)	I/O241 (D3)	65	68	65	92	102	132	H12	152	113	N2	T3
I/O82 (/CHECK)	I/O122 (/CHECK)	I/O162 (/CHECK)	I/O242 (/CHECK)	66	69	66	93	103	133	H11	153	112	N4	R1
			I/O243											

Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

AT40K05	AT40K10	AT40K20	AT40K40	Right Side (Bottom to Top)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
			I/O244											
I/O83	I/O123	I/O163	I/O245		70	67	94	104	134	G14	154	111	N3	R2
I/O84	I/O124	I/O164	I/O246				95	105	135	G15	155	110	M1	R4
			GND											GND(1)
	I/O125	I/O165	I/O247						136	G13	156	109	M2	R3
	I/O126	I/O166	I/O248						137	G12	157	108	M3	P2
		I/O167	I/O249									107	M4	P3
		I/O168	I/O250									106	L1	P4
			I/O251											N1
			I/O252											N2
			VCC										VCC(1)	VCC(1)
		GND	GND								158		GND(1)	GND(1)
		I/O169	I/O253									105	L2	N3
		I/O170	I/O254									104	L3	N4
			I/O255										K2	M1
			I/O256										L4	M2
			I/O257											M3
			I/O258											M4
			GND											GND(1)
I/O85 (D2)	I/O127 (D2)	I/O171 (D2)	I/O259 (D2)	67	71	68	96	106	138	G11	159	103	J1	L2
I/O86	I/O128	I/O172	I/O260	68	72	69	97	107	139	F15	160	102	K3	L3
	VCC	VCC	VCC							VCC(1)	161	101	VCC(1)	VCC(1)
I/O87	I/O129	I/O173	I/O261				98	108	140	F14	162	99	J2	K1
I/O88, FCK4	I/O130, FCK4	I/O174, FCK4	I/O262, FCK4				99	109	141	F13	163	98	J3	K2
	I/O131	I/O175	I/O263							G10	164	97	K4	K3
	I/O132	I/O176	I/O264							E15	165	96	G1	K4
GND	GND	GND	GND				100	110	142	GND(1)	166	95	GND(1)	GND(1)
		I/O177	I/O265									94	H2	J2
		I/O178	I/O266									93	H3	J3
	I/O133	I/O179	I/O267							E14	167	92	J4	J4
	I/O134	I/O180	I/O268							F12	168	91	F1	H1
			I/O269											
			I/O270											
			GND											GND(1)
	I/O135	I/O181	I/O271						143	E13	169	90	G2	H2
	I/O136	I/O182	I/O272						144	D15	170	89	G3	H3
I/O89	I/O137	I/O183	I/O273					111	145	F11	171	88	F2	H4

Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

AT40K05	AT40K10	AT40K20	AT40K40	Top Side (Right to Left)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
		GND	GND										GND(1)	GND(1)
	I/O151	I/O201	I/O301	75	79	76	109	121	159	F9	189	66	C7	D8
	I/O152	I/O202	I/O302							D11	190	65	B6	C7
I/O103	I/O153	I/O203	I/O303				117	129	167	A12	191	64	A6	B7
I/O104	I/O154	I/O204	I/O304	75(2)	79(2)	76(2)	109(2)	130	168	C11	192	63	D8	D9
			I/O305										C8	B8
			I/O306											A8
														VCC(1)
			GND											GND(1)
			I/O307											
			I/O308											
	I/O155	I/O205	I/O309						169	B11	193	62	B7	D10
	I/O156	I/O206	I/O310						170	E10	194	61	A7	C9
		I/O207	I/O311								195	60	D9	B9
		I/O208	I/O312									59	C9	C10
GND	GND	GND	GND				118	131	171	GND(1)	196	58	GND(1)	GND(1)v
I/O105	I/O157	I/O209	I/O313				119	132	172	A11	197	57	B8	B10
I/O106	I/O158	I/O210	I/O314				120	133	173	D10	198	56	D10	A10
	I/O159	I/O211	I/O315							C10	199	55	C10	C11
	I/O160	I/O212	I/O316							B10	200	54	B9	D12
	VCC	VCC	VCC							VCC*	201	52	VCC(1)	VCC(1)
		I/O213	I/O317									51	A9	B11
		I/O214	I/O318									50	D11	C12
			GND											GND(1)
			I/O319											D13
			I/O320											B12
			I/O321										C11	C13
			I/O322										B10	A12
		I/O215	I/O323									49	B11	D14
		I/O216	I/O324									48	A11	B13
		GND	GND										GND(1)	GND(1)
			VCC										VCC(1)	VCC(1)
I/O107 (A4)	I/O161 (A4)	I/O217 (A4)	I/O325 (A4)	81	85	82	121	134	174	A10	202	47	D12	C14
I/O108 (A5)	I/O162 (A5)	I/O218 (A5)	I/O326 (A5)	82	86	83	122	135	175	D9	203	46	C12	A13
	I/O163	I/O219	I/O327						176	C9	205	45	B12	B14
	I/O164	I/O220	I/O328					136	177	B9	206	44	A12	D15
I/O109	I/O165	I/O221	I/O329		87	84	123	137	178	A9	207	43	C13	C15
I/O110	I/O166	I/O222	I/O330		88	85	124	138	179	E9	208	42	B13	B15

Notes: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

2. This applies to the AT40K05 only.

AT40K05	AT40K10	AT40K20	AT40K40	Top Side (Right to Left)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
			GND											GND(1)
			I/O331											
			I/O332											
			I/O333											A15
			I/O334											C16
I/O111 (A6)	I/O167 (A6)	I/O223 (A6)	I/O335 (A6)	83	89	86	125	139	180	C8	209	41	A13	B16
I/O112 (A7)	I/O168 (A7)	I/O224 (A7)	I/O336 (A7)	84	90	87	126	140	181	B8	210	40	B14	A16
GND	GND	GND	GND	1	91	88	127	141	182	GND(1)	211	39	GND(1)	GND(1)
VCC	VCC	VCC	VCC	2	92	89	128	142	183	VCC(1)	212	38	VCC(1)	VCC(1)
I/O113 (A8)	I/O169 (A8)	I/O225 (A8)	I/O337 (A8)	3	93	90	129	143	184	E8	213	37	D14	D17
I/O114 (A9)	I/O170 (A9)	I/O226 (A9)	I/O338 (A9)	4	94	91	130	144	185	B7	214	36	C14	A17
			I/O339											C17
			I/O340											B17
			I/O341											
			I/O342											
			GND											GND(1)
I/O115	I/O171	I/O227	I/O343		95	92	131	145	186	A7	215	35	A15	C18
I/O116	I/O172	I/O228	I/O344		96	93	132	146	187	C7	216	34	B15	D18
	I/O173	I/O229	I/O345						188	D7	217	33	C15	B18
	I/O174	I/O230	I/O346						189	E7	218	32	D15	A19
I/O117 (A10)	I/O175 (A10)	I/O231 (A10)	I/O347 (A10)	5	97	94	133	147	190	A6	220	31	A16	B19
I/O118 (A11)	I/O176 (A11)	I/O232 (A11)	I/O348 (A11)	6	98	95	134	148	191	B6	221	30	B16	C19
			VCC										VCC(1)	VCC(1)
		GND	GND										GND(1)	GND(1)
		I/O233	I/O349									29	C16	D19
		I/O234	I/O350									28	B17	A20
			I/O351										D16	B20
			I/O352										A18	C20
			I/O353											B21
			I/O354											D20
			GND											GND(1)
		I/O235	I/O355									27	C17	C21
		I/O236	I/O356									26	B18	A22
	VCC	VCC	VCC							VCC(1)	222	25	VCC(1)	VCC(1)
	I/O177	I/O237	I/O357							C6	223	23	C18	B22
	I/O178	I/O238	I/O358							F7	224	22	D17	C22
I/O119	I/O179	I/O239	I/O359				135	149	192	A5	225	21	A20	B23
I/O120	I/O180	I/O240	I/O360				136	150	193	B5	226	20	B19	A24

Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

AT40K20 Ordering Information

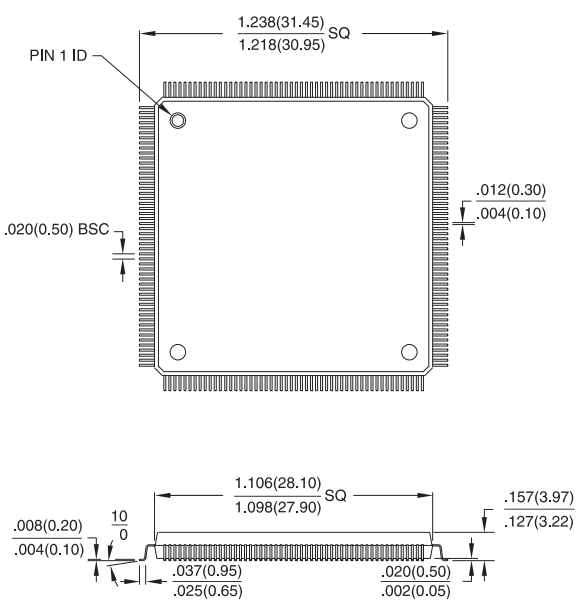
Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
20,000-30,000	2	AT40K20-2AJC	84J	5V Commercial
		AT40K20-2AQC	100Q	(0°C to 70°C)
		AT40K20-2BQC	144Q	
		AT40K20-2CQC	160Q	
		AT40K20-2DQC	208Q	
		AT40K20-2EQC	240Q	
		AT40K20-2FQC	304Q	
		AT40K20-2BGC	352G	
		AT40K20-2AGC	225G	
20,000-30,000	2	AT40K20-2AJI	84J	5V Industrial
		AT40K20-2BQI	144Q	(-40°C to 85°C)
		AT40K20-2CQI	160Q	
		AT40K20-2DQI	208Q	
		AT40K20-2EQI	240Q	
		AT40K20-2FQI	304Q	
		AT40K20-2BGI	352G	
		AT40K20-2AGI	225G	

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
20,000-30,000	3	AT40K20LV-2AJC	84J	3.3V Commercial
		AT40K20LV-2AQC	100Q	(0°C to 20°C)
		AT40K20LV-2BQC	144Q	
		AT40K20LV-2CQC	160Q	
		AT40K20LV-2DQC	208Q	
		AT40K20LV-2EQC	240Q	
		AT40K20LV-2FQC	304Q	
		AT40K20LV-2BGC	352G	
		AT40K20LV-2AGC	225G	

Package Type	
84J	84-lead, Plastic J-Leaded Chip Carrier (PLCC)
100Q	100-lead, Very Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (VQFP)
144Q	144-lead, Thin (1.4 mm) Plastic Gull Wing Quad Flat Package (TQFP)
160Q	160-lead, Plastic Gull Wing Quad Flat Package (PQFP)
208Q	208-lead, Plastic Gull Wing Quad Flat Package (PQFP)
225G	225-lead, Ball Grid Array Package (BGA)
240Q	240-lead, Plastic Gull Wing Quad Flat Package (PQFP)
304Q	304-lead, Plastic Gull Wing Quad Flat Package (PQFP)
352G	352-ball, Ball Grid Array Package (BGA)
432G	432-ball, Ball Grid Array Package (BGA)

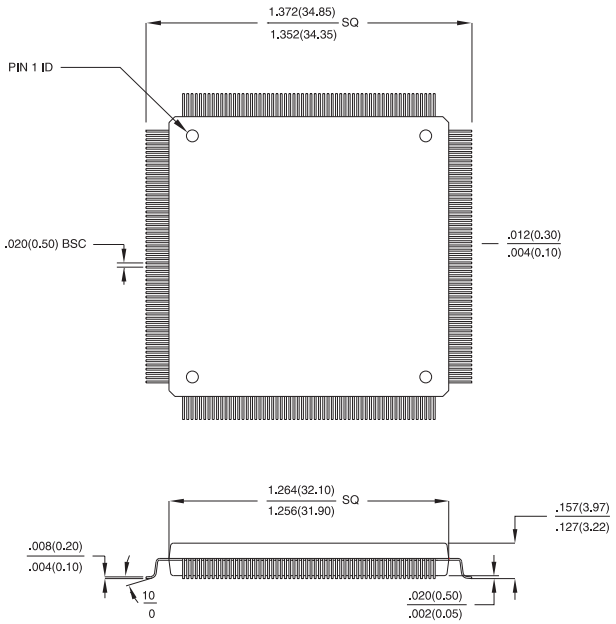
Packaging Information

208Q, 208-lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in (Millimeters) and Inches



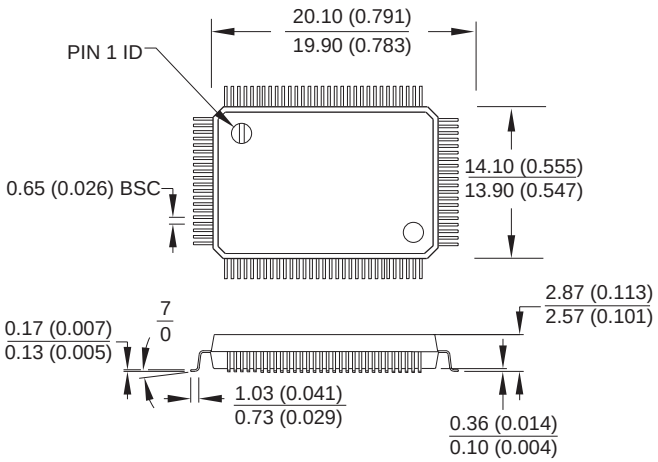
*Controlling dimension: millimeters

240Q, 240-lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in (Millimeters) and Inches



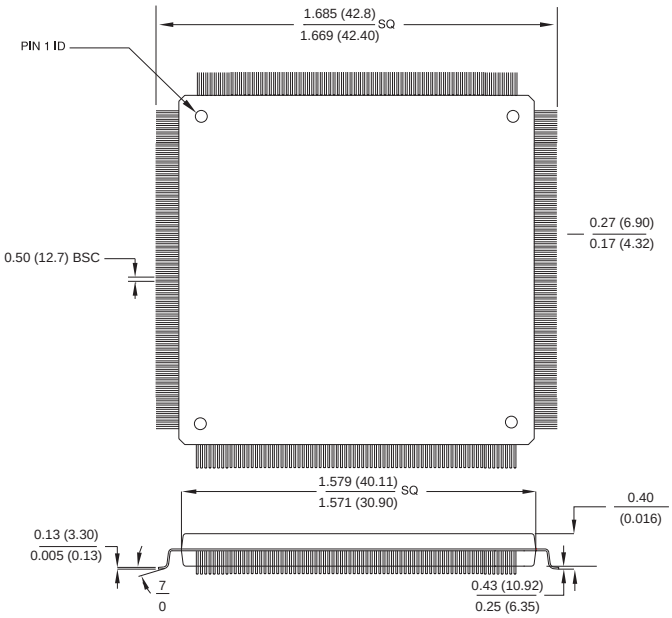
*Controlling dimension: millimeters

100RQ, 100-lead, Rectangular Plastic Gull Wing Quad Flat Pack (RQFP)
Dimensions in Millimeters and (Inches)*



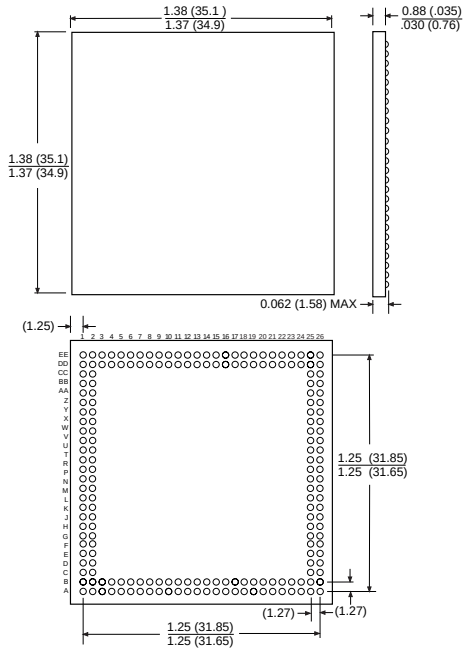
*Controlling dimension: millimeters

304Q, 304-lead, Plastic Gull Wing Quad Flat Pack (PQFP)
Dimensions in (Millimeters) and Inches

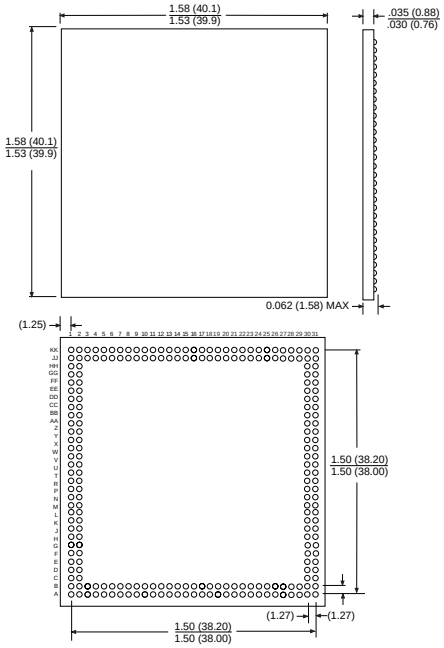


Packaging Information

352B, 352-ball Ball Grid Array (BGA)
Dimensions in (Millimeters) and Inches



432B, 432-ball Ball Grid Array (BGA)
Dimensions in (Millimeters) and Inches



Thermal Coefficient Table

Package Style	Lead Count	Theta J-A 0 LFPM	Theta J-A 225 LFPM	Theta J-A 500 LPFM	Theta J-C
PQFP	144	33	27	23	8.5
PQFP	160	30	24	20	7
PQFP	208	32	28	24	10
PQFP	240	27	No Data	No Data	
PQFP	304	19	No Data	No Data	
TQFP	100	47	39	33	22
RQFP	100	3			
PLCC	84	37	30	25	12
BGA	225	26	No Data	No Data	
BGA	352				
BGA	432				