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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

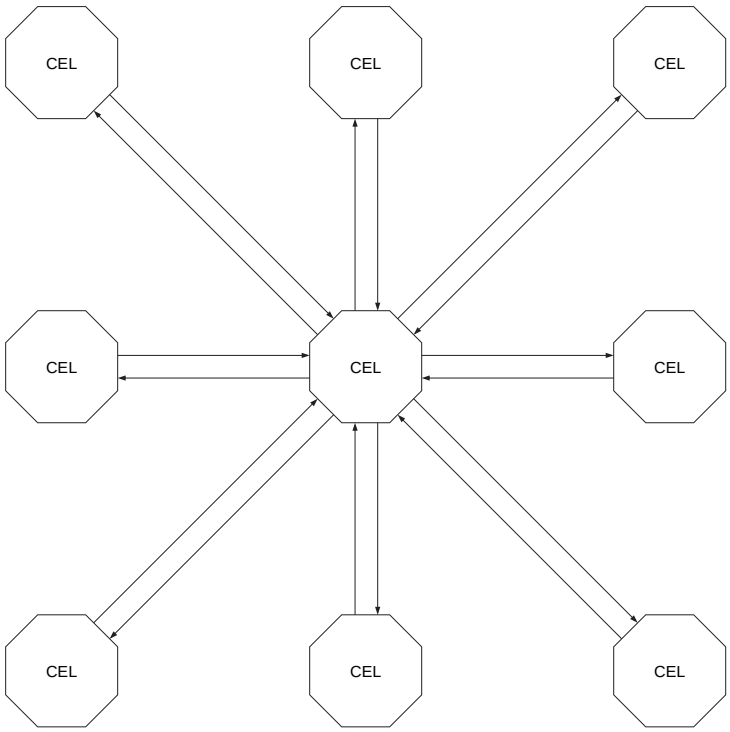
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	2304
Total RAM Bits	18432
Number of I/O	193
Number of Gates	50000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at40k40lv-3eqc

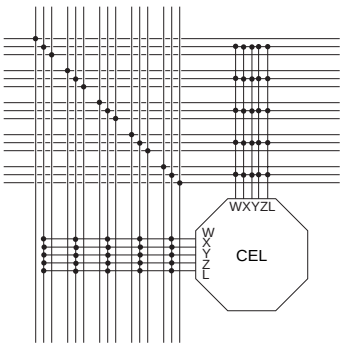
Cell Connections

Figure 4(a) depicts direct connections between a cell and its eight nearest neighbors. Figure 4(b) shows the connections between a cell five horizontal local buses (one per busing plane) and five vertical local buses (one per busing plane).

Figure 4. Cell Connections



(a) Cell to Cell Connections

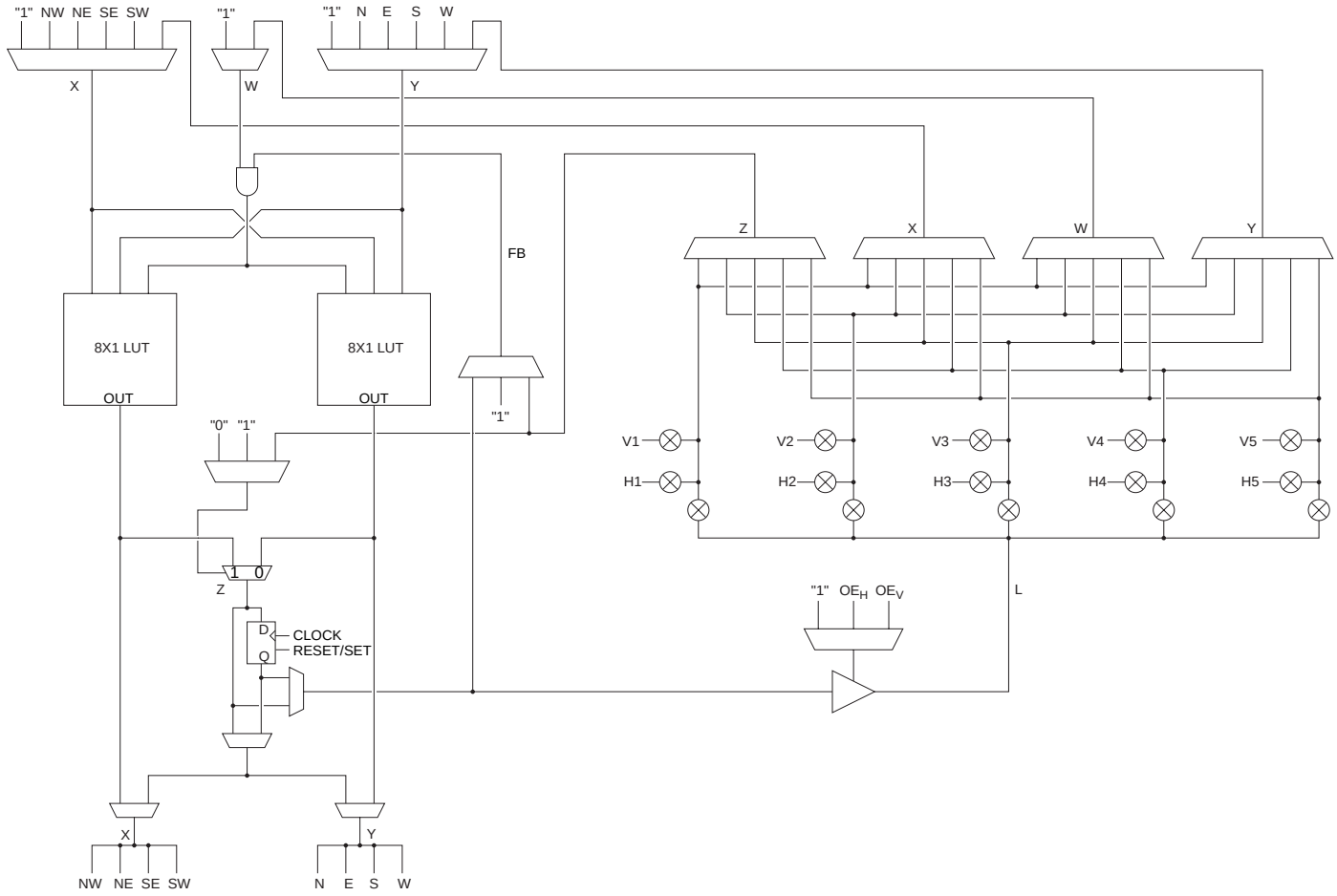


(b) Cell to Bus Connections

The Cell

Figure 5 depicts the AT40K cell. Configuration bits for separate muxes and pass gates are independent. All permutations of programmable muxes and pass gates are legal. Vn is connected to the vertical local bus in plane n. Hn is connected to the horizontal local bus in plane n. A local/local turn in plane n is achieved by turning on the two pass gates connected to Vn and Hn. Up to five simultaneous local/local turns are possible.

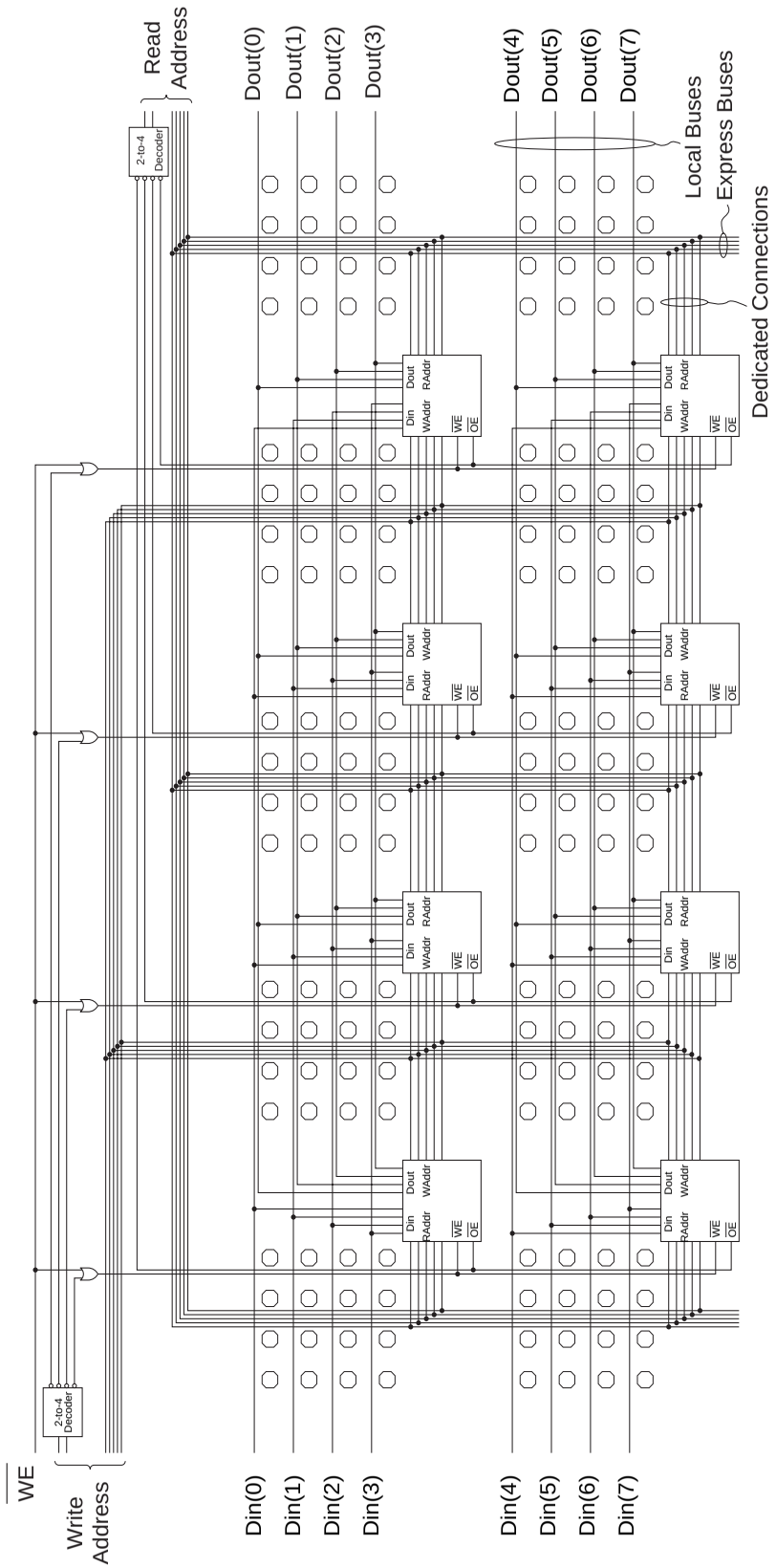
Figure 5. The Cell



X = Diagonal Direct Connect or Bus
Y = Orthogonal Direct Connect or Bus
W = Bus Connection
Z = Bus Connection
FB = Internal Feedback

The core cell can be configured in several “modes”. The core cell flexibility makes the AT40K architecture well suited to most digital design application areas (see Figure 6).

Figure 9. RAM Example: 128 x 8 Dual-Ported RAM (asynchronous)

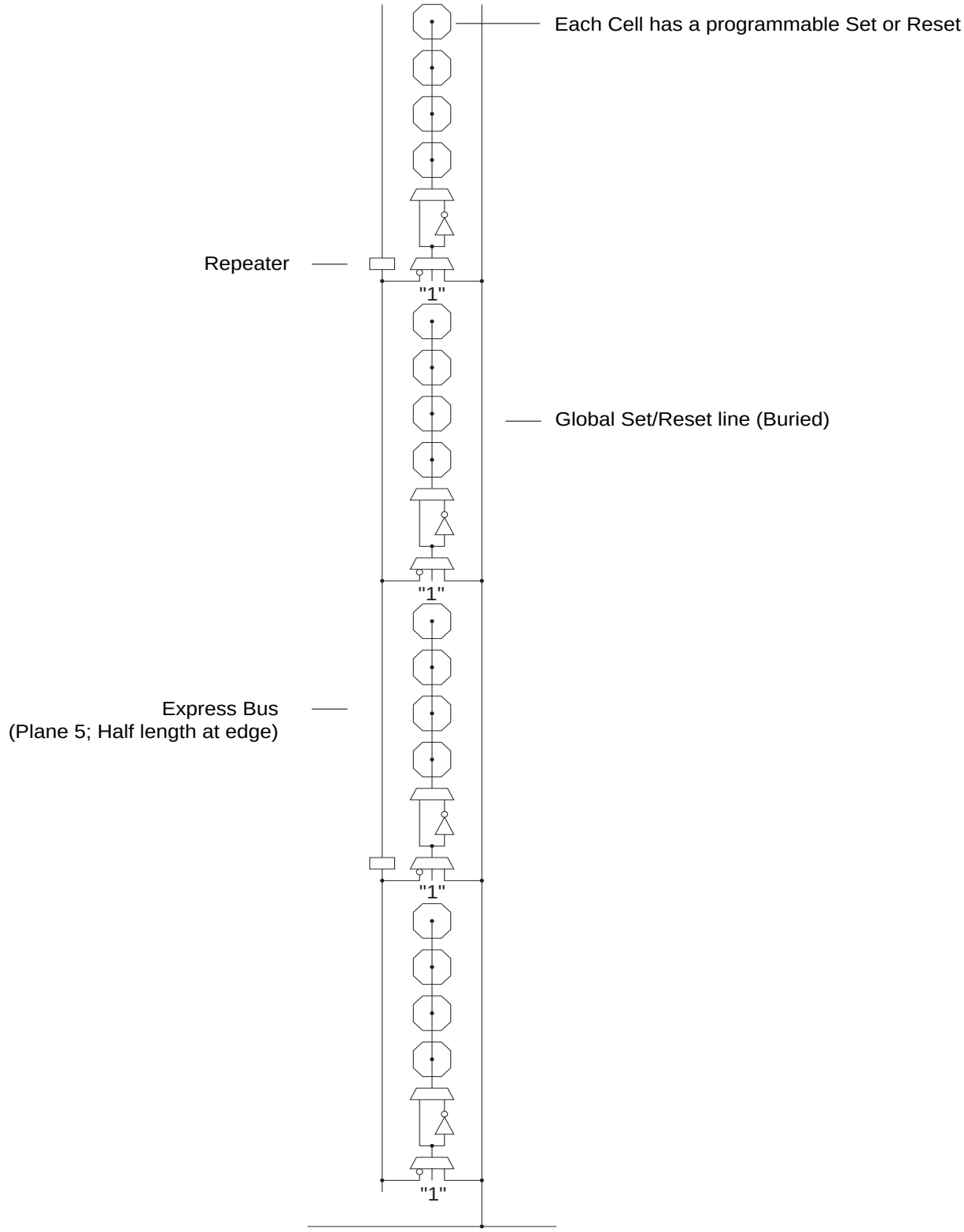


Clocking and Set/Reset

Each of 8 dedicated Global Clock buses is connected to a dual-use Global Clock pad (GCK1 - GCK8). An internal signal can be placed on a Global Clock bus by routing that signal to a Global Clock pad. Each column of the array has a Column Clock selected from one of the 8 Global Clock buses. The extreme-left Column Clock mux has two additional inputs from dual-use pins FCK1 & FCK2 to provide fast clocking to left-side I/O. The extreme-right Column Clock mux has two additional inputs from dual-use pins FCK3 & FCK4 to provide fast clocking to right-side I/O. Each sector column of 4 cells can be clocked from a (Plane 4) express bus or from the Column Clock. Clocking to the 4 cells can be disabled. The Plane 4 express bus used for clocking is half length at the array edge. The clock provided to each sector column of 4 cells can be either inverted or not inverted. The register in each cell is triggered on a rising clock edge. On power up, constant “0” is provided to each registers clock pins.

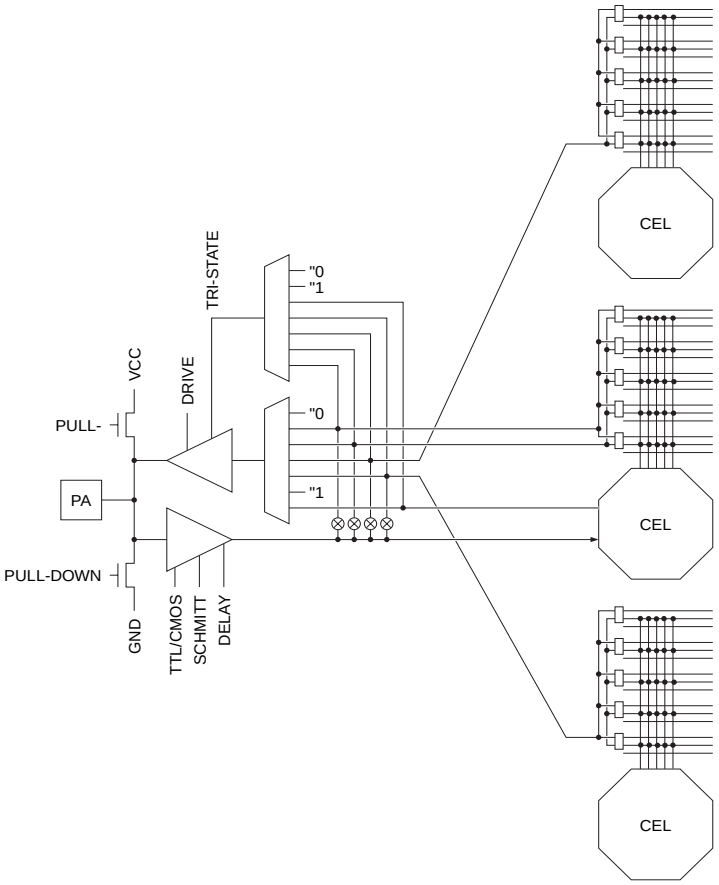
A dedicated Global Set/Reset bus can be driven by any USER I/O pad, except those used for clocking, Global or Fast. An internal signal can be placed on the Global Set/Reset bus by routing that signal to the pad programmed as the Global Set/Reset input. Global Set/Reset is distributed to each column of the array. Each sector column of 4 cells can be Set/Reset by a (Plane 5) express bus or by the Global Set/Reset. The Plane 5 express bus used for Set/Reset is half length at array edge. The Set/Reset provided to each sector column of 4 cells can be either inverted or not inverted. The function of the Set/Reset input of a register (either Set or Reset) is determined by a configuration bit in each cell. The Set/Reset input of a register is Active Low (logic 0). Setting or resetting of a register is asynchronous. On power up, a logic 1 (a high) is provided by each register, i.e., all registers are set at power up.

Figure 11. Set/Reset (for one column of cells)

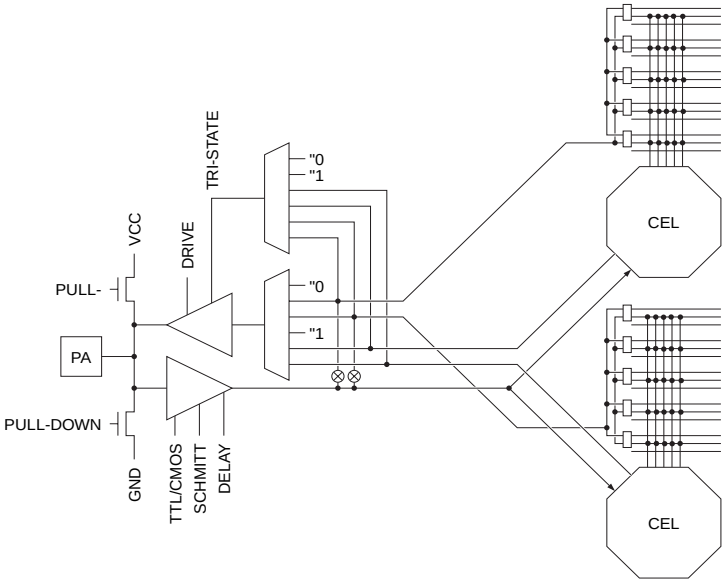


Any User I/O can drive Global Set/Reset line

Figure 12. West I/O (Mirrored for East I /O)

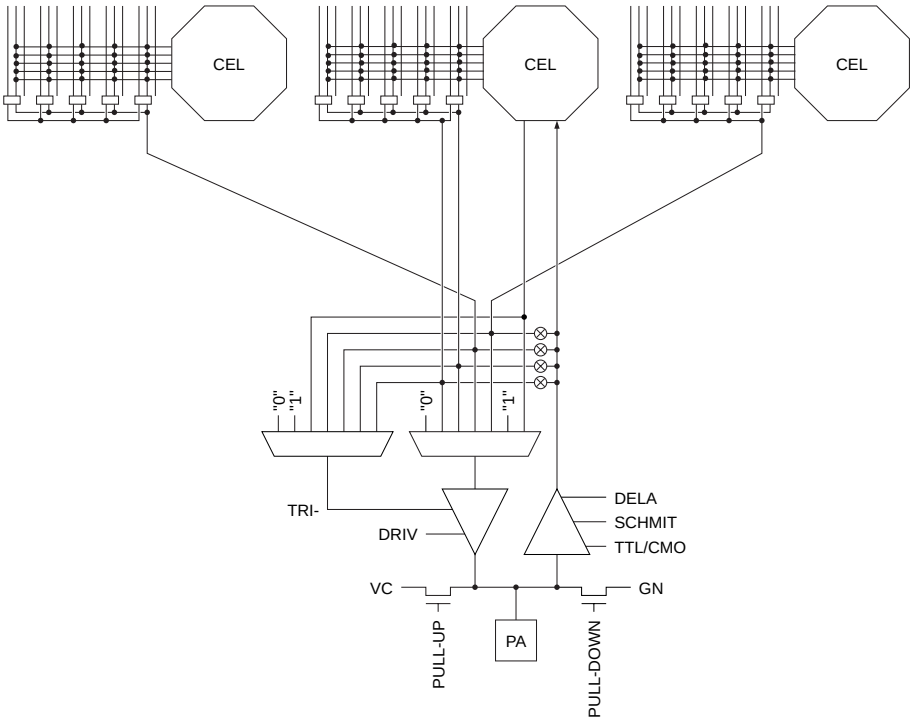


(a) Primary

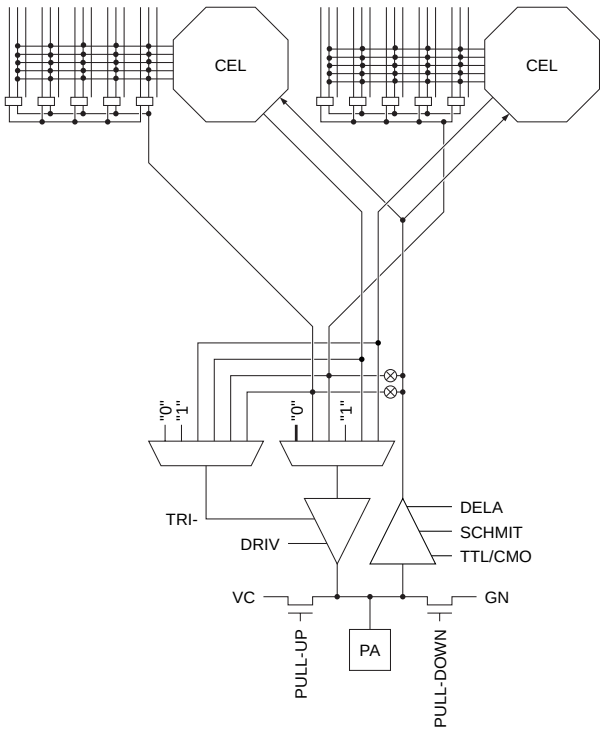


(a) Secondary

Figure 13. South I/O (Mirrored for North I/O)

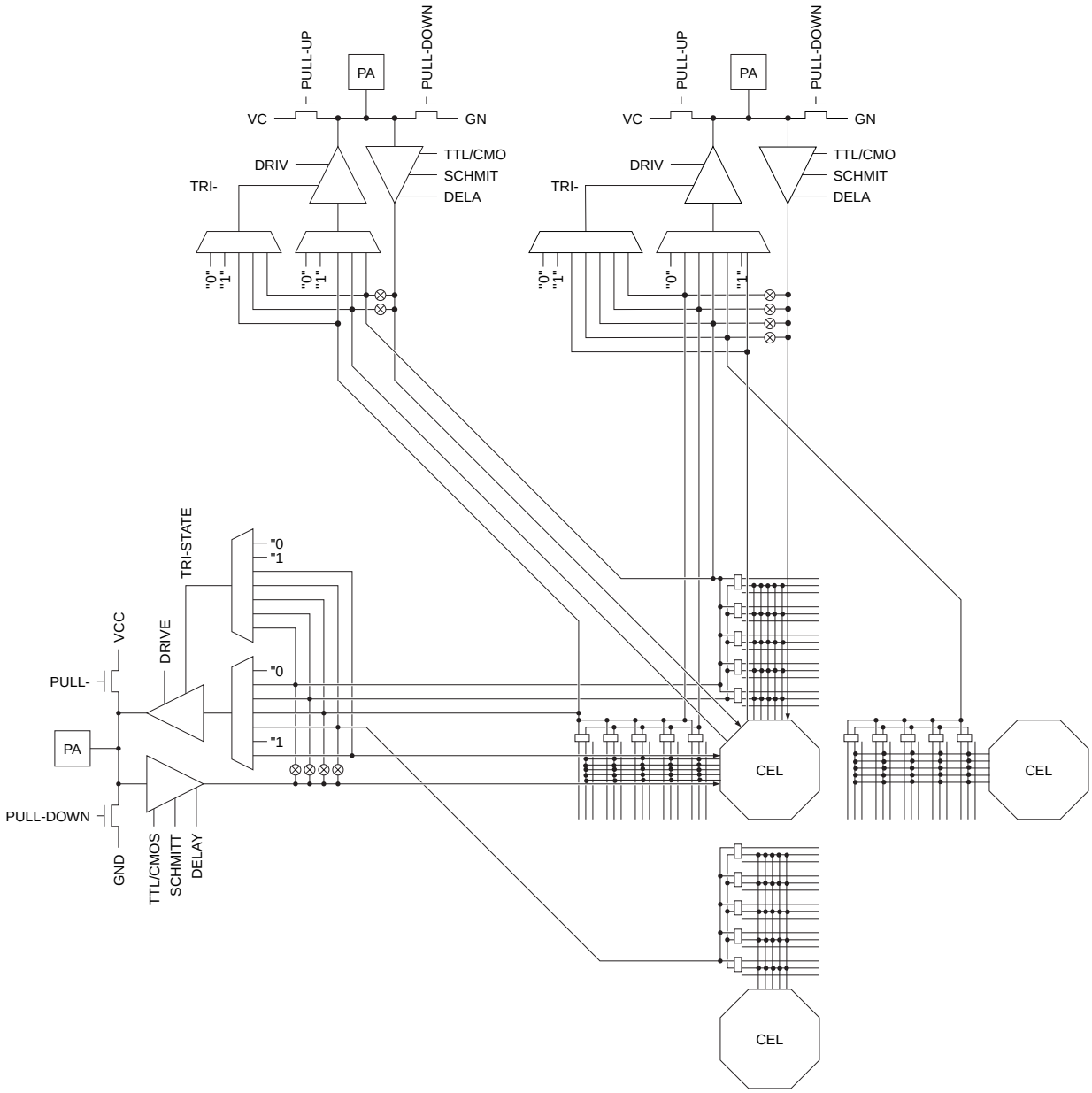


(a) Primary



(a) Secondary

Figure 14. North/West Corner, (similar for NE/SE/SW corners)



AC Timing Characteristics - 5V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Max delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-2	Units	Notes
Async RAM					
Write	t_{WECYC}(min)	cycle time	8.0	ns	
Write	t_{WEL}(min)	we	3.0	ns	pulse width low
Write	t_{WEH}(min)	we	3.0	ns	pulse width high
Write	t_{setup}(min)	wr addr setup-> we	2.0	ns	
Write	t_{hold}(min)	wr addr hold -> we	0.0	ns	
Write	t_{setup}(min)	din setup -> we	2.0	ns	
Write	t_{hold}(min)	din hold -> we	0.0	ns	
Write	t_{hold}(min)	oe hold -> we	0.0	ns	
Write/Read	t_{PD}(max)	din -> dout	4.6	ns	rd addr = wr addr
Read	t_{PD}(max)	rd addr -> dout	3.1	ns	
Read	t_{PZX}(max)	oe -> dout	1.6	ns	
Read	t_{PXZ}(max)	oe -> dout	2.0	ns	
Sync RAM					
Write	t_{CYC}(min)	cycle time	8.0	ns	
Write	t_{CLKL}(min)	clk	3.0	ns	pulse width low
Write	t_{CLKH}(min)	clk	3.0	ns	pulse width high
Write	t_{setup}(min)	we setup-> clk	2.0	ns	
Write	t_{hold}(min)	we hold -> clk	0.0	ns	
Write	t_{setup}(min)	wr addr setup-> clk	2.0	ns	
Write	t_{hold}(min)	wr addr hold -> clk	0.0	ns	
Write	t_{setup}(min)	wr data setup-> clk	2.0	ns	
Write	t_{hold}(min)	wr data hold -> clk	0.0	ns	
Write/Read	t_{PD}(max)	din -> dout	4.6	ns	rd addr = wr addr
Write/Read	t_{PD}(max)	clk -> dout	3.5	ns	rd addr = wr addr
Read	t_{PD}(max)	rd addr -> dout	3.1	ns	
Read	t_{PZX}(max)	oe -> dout	1.6	ns	
Read	t_{PXZ}(max)	oe -> dout	2.0	ns	

Absolute Maximum Ratings - 3.3V Commercial/Industrial*

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Supply Voltage	With respect to GND	-0.5	7.0	V
V_I	DC Input Voltage(1)	With respect ot GND	-0.5	7.0	V
V_O	DC Output Voltaage	With respect ot GND	-0.5	7.0	V
T_{STG}	Storage Temperature		-65°C	+150°C	
T_J	Junction Temperature			+150°C	
T_L	Lead Temperature (Soldering, 10 sec.)			+250°C	
ESD		R_{ZAP} = 1.5K, C_{ZAP} = 100 pF		2000	V

Note: 1. Minimum voltage of -0.5V DC which may undershoot to -2.0V for pulses of less than 20 ns.

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range - 3.3V Operation

		AT40K05LV-4/3/2 AT40K10LV-4/3/2 AT40K20LV-4/3/2 AT40K40LV-4/3/2 Commercial	**AT40K05LV-4/3/2 AT40K10LV-4/3/2 AT40K20LV-4/3/2 AT40K40LV-4/3/2 Industrial**
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply		3.3V ± 0.3V	3.3V ± 0.3V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% V_{CC}

AC Timing Characteristics - 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.00V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.60V, temperature = 0°C
Max delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-3	Units	Notes
Core					
2 input gate	t_{PD}(max)	x/y -> x/y	2.9	ns	1 unit load
3 input gate	t_{PD}(max)	x/y/z -> x/y	2.8	ns	1 unit load
3 input gate	t_{PD}(max)	x/y/w -> x/y	3.4	ns	1 unit load
4 input gate	t_{PD}(max)	x/y/w/z -> x/y	3.4	ns	1 unit load
fast carry	t_{PD}(max)	y -> y	2.3	ns	1 unit load
fast carry	t_{PD}(max)	x -> y	2.9	ns	1 unit load
fast carry	t_{PD}(max)	y -> x	3.0	ns	1 unit load
fast carry	t_{PD}(max)	x -> x	2.3	ns	1 unit load
fast carry	t_{PD}(max)	w -> y	3.4	ns	1 unit load
fast carry	t_{PD}(max)	w -> x	3.4	ns	1 unit load
fast carry	t_{PD}(max)	z -> y	3.4	ns	1 unit load
fast carry	t_{PD}(max)	z -> x	2.4	ns	1 unit load
DFF	t_{PD}(max)	q -> x/y	2.8	ns	1 unit load
DFF	t_{setup}(min)	x/y -> clk		ns	
DFF	t_{hold}(min)	x/y -> clk		ns	
DFF	t_{PD}(max)	R -> x/y	3.2	ns	1 unit load
DFF	t_{PD}(max)	S -> x/y	3.0	ns	1 unit load
DFF	t_{PD}(max)	q -> w	2.7	ns	
incremental --> L	t_{PD}(max)	x/y -> L	2.4	ns	1 unit load
Local output enable	t_{PZX}(max)	oe -> L	2.8	ns	1 unit load
Local output enable	t_{PXZ}(max)	oe -> L	2.4	ns	

AC Timing Characteristics - 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C
Max delays are the average of t_{PDLH} and t_{PDHL}.

Clocks and Reset Input buffers are measured from a VIH of 1.5V at the input pad to the internal VIH of 50% of VCC. Maximum times for clock input buffers and internal drivers are measured for rising edge delays only.

Cell Function	Parameter	Path	Device	-3	Units	Notes
Global Clocks and Set/Reset						
GCK Input buffer	t_{PD}(max)	pad -> clock	AT40K05	1.3	ns	rising edge clock
		pad -> clock	AT40K10	1.5	ns	
		pad -> clock	AT40K20	1.6	ns	
		pad -> clock	AT40K40	1.9	ns	
FCK Input buffer	t_{PD}(max)	pad -> clock	AT40K05	0.7	ns	rising edge clock
		pad -> clock	AT40K10	0.8	ns	
		pad -> clock	AT40K20	0.8	ns	
		pad -> clock	AT40K40	0.9	ns	
Clock column driver	t_{PD}(max)	clock -> colclk	AT40K05	1.5	ns	rising edge clock
		clock -> colclk	AT40K10	1.8	ns	
		clock -> colclk	AT40K20	2.0	ns	
		clock -> colclk	AT40K40	2.5	ns	
Clock sector driver	t_{PD}(max)	colclk -> secclk	AT40K05	1.0	ns	rising edge clock
		colclk -> secclk	AT40K10	1.0	ns	
		colclk -> secclk	AT40K20	1.0	ns	
		colclk -> secclk	AT40K40	1.0	ns	
GSRN Input buffer	t_{PD}(max)	pad -> GSRN	AT40K05	4.5	ns	
		colclk -> secclk	AT40K10	5.4	ns	
		colclk -> secclk	AT40K20	6.3	ns	
		colclk -> secclk	AT40K40	8.2	ns	
Global clock to output	t_{PD}(max)	clock pad -> out	AT40K05	13.0	ns	rising edge clock
		clock pad -> out	AT40K10	13.4	ns	fully loaded clock tree
		clock pad -> out	AT40K20	13.8	ns	rising edge DFF
		clock pad -> out	AT40K40	14.5	ns	20mA output buffer
						50 pf pin load
Fast clock to output	t_{PD}(max)	clock pad -> out	AT40K05	12.4	ns	rising edge clock
		clock pad -> out	AT40K10	12.7	ns	fully loaded clock tree
		clock pad -> out	AT40K20	13.0	ns	rising edge DFF
		clock pad -> out	AT40K40	13.5	ns	20mA output buffer
						50 pf pin load

AC Timing Characteristics - 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C

Cell Function	Parameter	Path	-4	-3	Units	Notes
Async RAM						
Write	t_{WECYC}(min)	cycle time	14.0	12.0	ns	
Write	t_{WEL}(min)	we	6.0	5.0	ns	pulse width low
Write	t_{WEH}(min)	we	6.0	5.0	ns	pulse width high
Write	t_{setup}(min)	wr addr setup-> we	5.3	5.3	ns	
Write	t_{hold}(min)	wr addr hold -> we	0.0	0.0	ns	
Write	t_{setup}(min)	din setup -> we	6.0	5.0	ns	
Write	t_{hold}(min)	din hold -> we	0.0	0.0	ns	
Write	t_{hold}(min)	oe hold -> we	0.0	0.0	ns	
Write/Read	t_{PD}(max)	din -> dout	12.1	8.7	ns	rd addr = wr addr
Read	t_{PD}(max)	rd addr -> dout	9.7	6.3	ns	
Read	t_{PZX}(max)	oe -> dout	4.2	2.9	ns	
Read	t_{PXZ}(max)	oe -> dout	3.5	3.5	ns	
Sync RAM						
Write	t_{CYC}(min)	cycle time	12.0	12.0	ns	
Write	t_{CLKL}(min)	clk	6.0	5.0	ns	pulse width low
Write	t_{CLKH}(min)	clk	6.0	5.0	ns	pulse width high
Write	t_{setup}(min)	we setup-> clk	3.2	3.2	ns	
Write	t_{hold}(min)	we hold -> clk	0.0	0.0	ns	
Write	t_{setup}(min)	wr addr setup-> clk	6.0	5.0	ns	
Write	t_{hold}(min)	wr addr hold -> clk	0.0	0.0	ns	
Write	t_{setup}(min)	wr data setup-> clk	3.0	3.9	ns	
Write	t_{hold}(min)	wr data hold -> clk	0.0	0.0	ns	
Write/Read	t_{PD}(max)	din -> dout	12.1	8.7	ns	rd addr = wr addr
Write/Read	t_{PD}(max)	clk -> dout	9.9	5.8	ns	rd addr = wr addr
Read	t_{PD}(max)	rd addr -> dout	9.7	6.3	ns	
Read	t_{PZX}(max)	oe -> dout	4.01	2.9	ns	
Read	t_{PXZ}(max)	oe -> dout	3.5	3.5	ns	

Notes:
1. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. Buffer delay is to a pad voltage of 1.5V with one output switching.
3. Parameter based on characterization and simulation; not tested in production.
4. Exact power calculation is available in Atmel FPGA Designer Software.

Part/Package Availability

	AT40K05	AT40K10	AT40K20	AT40K40
PC 84	X	X	X	
RQ100	X	X		
VQ 100	X	X	X	
TQ 144	X	X	X	X
PQ 160	X	X	X	
PQ 208	X	X	X	X
PQ 240		X	X	X
PQ 304			X	X
BG 225			X	X
BG 352			X	X
BG 432				X
PG 475				X

USER I/O Counts - (Including Dual-Function Pins)

	AT40K05	AT40K10	AT40K20	AT40K40
PC 84	62	62	62	
RQ 100	78	78		
VQ 100	78	78	78	
TQ 144	114	114	114	114
PQ 160	128	130	130	
PQ 208	128	161	161	161
PQ 240		192	193	193
PQ 304			256	256
BG 225			192	192
BG 352			256	289
BG 432				352
PG 475				384

Devices in same packages are pin-for-pin replaceable.

AT40K05	AT40K10	AT40K20	AT40K40	Left Side (Top to Bottom)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
	I/O18	I/O22	I/O30							F1	21	279	J25	L30
			GND											GND*
			I/O31											M30
			I/O32											M28
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
			I/O33										J26	M29
			I/O34										L23	M31
		I/O23	I/O35									278	L24	N31
		I/O24	I/O36									277	K25	N28
		GND	GND								22		GND(1)	GND(1)
			VCC										VCC(1)	VCC(1)
			I/O37											N29
			I/O38											N30
		I/O25	I/O39									276	L25	P30
		I/O26	I/O40									275	L26	P28
	I/O19	I/O27	I/O41						19	G4	23	274	M23	P29
	I/O20	I/O28	I/O42						20	G3	24	273	M24	R31
			GND											GND(1)
I/O13	I/O21	I/O29	I/O43				13	15	21	G2	25	272	M25	R30
I/O14	I/O22	I/O30	I/O44		11	8	14	16	22	G1	26	271	M26	R28
			I/O45											
			I/O46											
I/O15 (A22)	I/O23 (A22)	I/O31 (A22)	I/O47 (A22)	19	12	9	15	17	23	G5	27	270	N24	R29
I/O16 (A23)	I/O24 (A23)	I/O32 (A23)	I/O48 (A23)	20	13	10	16	18	24	H3	28	269	N25	T31
GND	GND	GND	GND	21	14	11	17	19	25	GND(1)	29	268	GND(1)	GND(1)
VCC	VCC	VCC	VCC	22	15	12	18	20	26	VCC(1)	30	267	VCC(1)	VCC(1)
I/O17	I/O25	I/O33	I/O49	23	16	13	19	21	27	H4	31	266	N26	T30
I/O18	I/O26	I/O34	I/O50	24	17	14	20	22	28	H5	32	265	P25	T29
			I/O51											
			I/O52											
I/O19	I/O27	I/O35	I/O53		18	15	21	23	29	J2	33	264	P23	U31
I/O20	I/O28	I/O36	I/O54				22	24	30	J1	34	263	P24	U30
			GND											GND(1)
	I/O29	I/O37	I/O55						31	J3	35	262	R26	U28
	I/O30	I/O38	I/O56						32	J4	36	261	R25	U29
		I/O39	I/O57									260	R24	V30
		I/O40	I/O58									259	R23	V29
			I/O59											V28
			I/O60											W31
			VCC										VCC(1)	VCC(1)
		GND	GND								37		GND(1)	GND(1)
		I/O41	I/O61									258	T26	W30
		I/O42	I/O62									257	T25	W29

Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

AT40K05	AT40K10	AT40K20	AT40K40	Bottom Side (Left to Right)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
I/O41	I/O61	I/O81	I/O121				46	52	68	R5	76	209	AD18	AJ22
I/O42	I/O62	I/O82	I/O122				47	53	69	M6	77	208	AE19	AK22
I/O43	I/O63	I/O83	I/O123	38	34	31	48	54	70	N6	78	207	AC17	AL22
I/O44	I/O64	I/O84	I/O124	39	35	32	49	55	71	P6	79	206	AD17	AJ21
	VCC	VCC	VCC							VCC(1)	80	204	VCC(1)	VCC(1)
	I/O65	I/O85	I/O125						72	R6	81	203	AE18	AH20
	I/O66	I/O86	I/O126						73	M7	82	202	AF18	AK21
			GND											GND(1)
			I/O127											AJ20
			I/O128											AH19
			I/O129										AC16	AK20
			I/O130										AD16	AJ19
		I/O87	I/O131									201	AE17	AL20
		I/O88	I/O132									200	AE16	AH18
		GND	GND								83		GND(1)	GND(1)
			VCC										VCC(1)	VCC(1)
		I/O89	I/O133									199	AF16	AK19
		I/O90	I/O134									198	AC15	AJ18
	I/O67	I/O91	I/O135							N7	84	197	AD15	AL19
	I/O68	I/O92	I/O136							P7	85	196	AE15	AK18
I/O45	I/O69	I/O93	I/O137		36	33	50	56	74	R7	86	195	AF15	AH17
I/O46	I/O70	I/O94	I/O138		37	34	51	57	75	L7	87	194	AD14	AJ17
			GND											GND(1)
			I/O139											
			I/O140											
			I/O141											AK17
			I/O142											AL17
I/O47 (D15)	I/O71 (D15)	I/O95 (D15)	I/O143 (D15)	40	38	35	52	58	76	N8	88	193	AE14	AJ16
I/O48 (INIT)	I/O72 (INIT)	I/O96 (INIT)	I/O144 (INIT)	41	39	36	53	59	77	P8	89	192	AF14	AK16
VCC	VCC	VCC	VCC	42	40	37	54	60	78	VCC(1)	90	191	VCC(1)	VCC(1)
GND	GND	GND	GND	43	41	38	55	61	79	GND(1)	91	190	GND(1)	GND(1)
I/O49 (D14)	I/O73 (D14)	I/O97 (D14)	I/O145 (D14)	44	42	39	56	62	80	L8	92	189	AE13	AL16
I/O50 (D13)	I/O74 (D13)	I/O98 (D13)	I/O146 (D13)	45	43	40	57	63	81	P9	93	188	AC13	AH15
			I/O147											AL15
			I/O148											AJ15
			I/O149											
			I/O150											
			GND											GND(1)
I/O51	I/O75	I/O99	I/O151		44	41	58	64	82	R9	94	187	AD13	AK15
I/O52	I/O76	I/O100	I/O152		45	42	59	65	83	N9	95	186	AF12	AJ14
	I/O77	I/O101	I/O153						84	M9	96	185	AE12	AH14
	I/O78	I/O102	I/O154						85	L9	97	184	AD12	AK14
		I/O103	I/O155									183	AC12	AL13

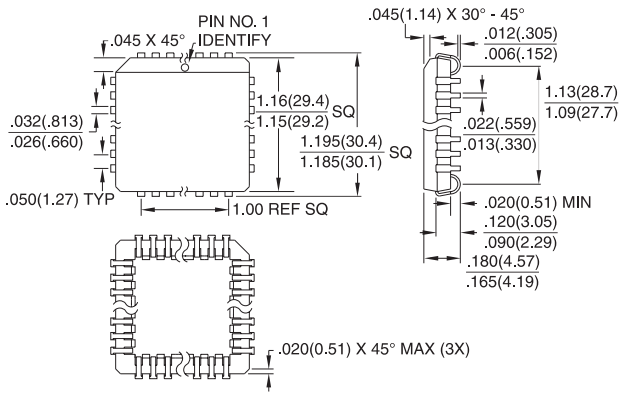
Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

AT40K05	AT40K10	AT40K20	AT40K40	Top Side (Right to Left)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
			GND											GND(1)
			I/O331											
			I/O332											
			I/O333											A15
			I/O334											C16
I/O111 (A6)	I/O167 (A6)	I/O223 (A6)	I/O335 (A6)	83	89	86	125	139	180	C8	209	41	A13	B16
I/O112 (A7)	I/O168 (A7)	I/O224 (A7)	I/O336 (A7)	84	90	87	126	140	181	B8	210	40	B14	A16
GND	GND	GND	GND	1	91	88	127	141	182	GND(1)	211	39	GND(1)	GND(1)
VCC	VCC	VCC	VCC	2	92	89	128	142	183	VCC(1)	212	38	VCC(1)	VCC(1)
I/O113 (A8)	I/O169 (A8)	I/O225 (A8)	I/O337 (A8)	3	93	90	129	143	184	E8	213	37	D14	D17
I/O114 (A9)	I/O170 (A9)	I/O226 (A9)	I/O338 (A9)	4	94	91	130	144	185	B7	214	36	C14	A17
			I/O339											C17
			I/O340											B17
			I/O341											
			I/O342											
			GND											GND(1)
I/O115	I/O171	I/O227	I/O343		95	92	131	145	186	A7	215	35	A15	C18
I/O116	I/O172	I/O228	I/O344		96	93	132	146	187	C7	216	34	B15	D18
	I/O173	I/O229	I/O345						188	D7	217	33	C15	B18
	I/O174	I/O230	I/O346						189	E7	218	32	D15	A19
I/O117 (A10)	I/O175 (A10)	I/O231 (A10)	I/O347 (A10)	5	97	94	133	147	190	A6	220	31	A16	B19
I/O118 (A11)	I/O176 (A11)	I/O232 (A11)	I/O348 (A11)	6	98	95	134	148	191	B6	221	30	B16	C19
			VCC										VCC(1)	VCC(1)
		GND	GND										GND(1)	GND(1)
		I/O233	I/O349									29	C16	D19
		I/O234	I/O350									28	B17	A20
			I/O351										D16	B20
			I/O352										A18	C20
			I/O353											B21
			I/O354											D20
			GND											GND(1)
		I/O235	I/O355									27	C17	C21
		I/O236	I/O356									26	B18	A22
	VCC	VCC	VCC							VCC(1)	222	25	VCC(1)	VCC(1)
	I/O177	I/O237	I/O357							C6	223	23	C18	B22
	I/O178	I/O238	I/O358							F7	224	22	D17	C22
I/O119	I/O179	I/O239	I/O359				135	149	192	A5	225	21	A20	B23
I/O120	I/O180	I/O240	I/O360				136	150	193	B5	226	20	B19	A24

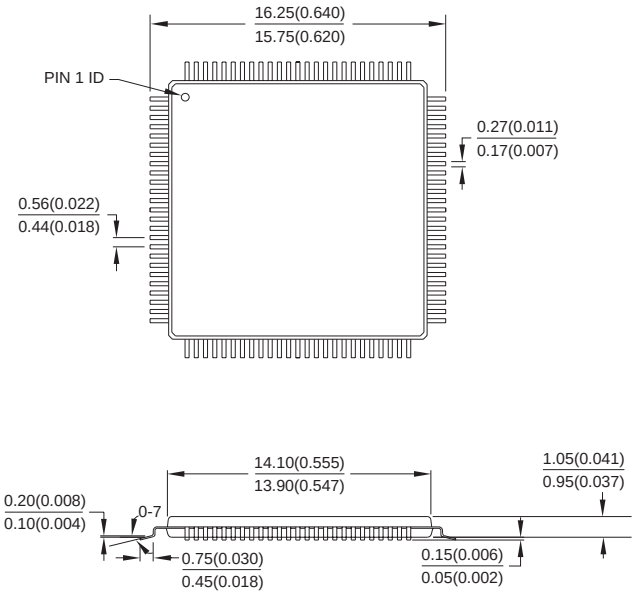
Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

Packaging Information

84J, 84-lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AF

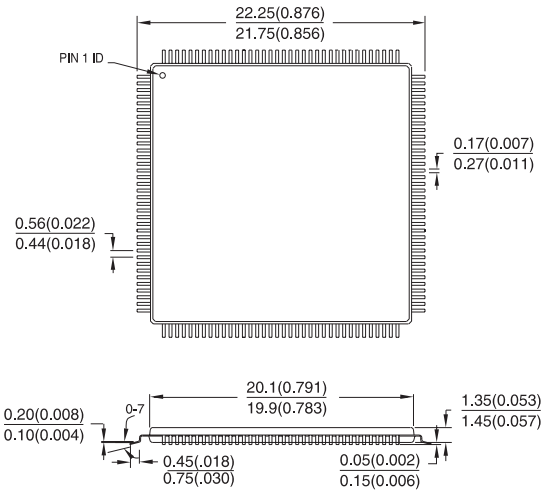


100Q, 100-lead, Plastic Gull Wing Quad Flat Package (VQFP)
Dimensions in Millimeters and (Inches)*



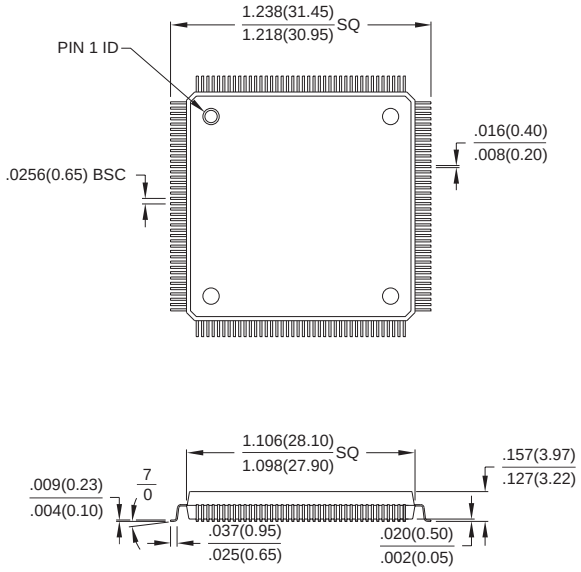
*Controlling dimension: millimeters

144Q, 144-lead, Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*



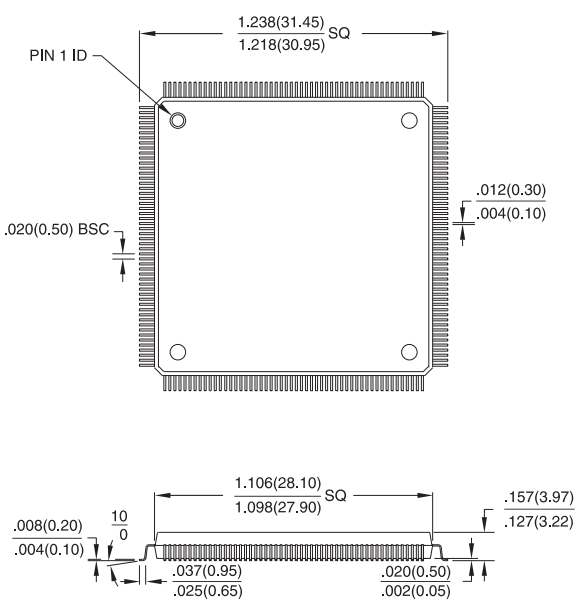
*Controlling dimension: millimeters

160Q, 160-lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in (Millimeters) and Inches



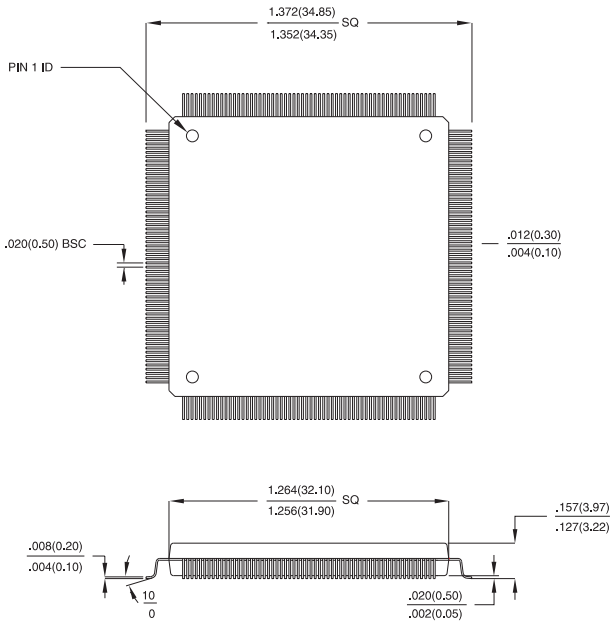
Packaging Information

208Q, 208-lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in (Millimeters) and Inches



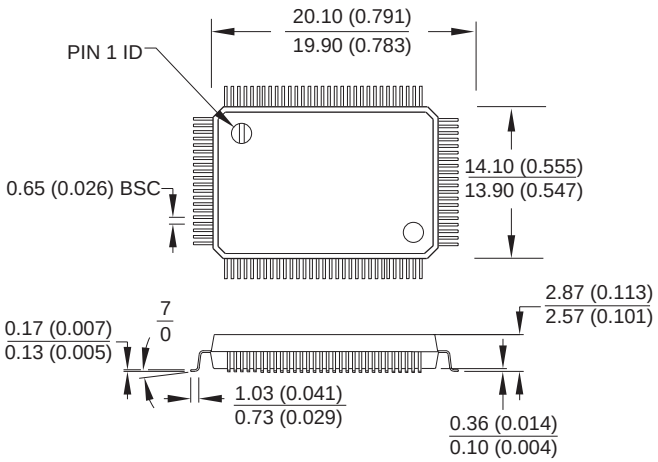
*Controlling dimension: millimeters

240Q, 240-lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in (Millimeters) and Inches



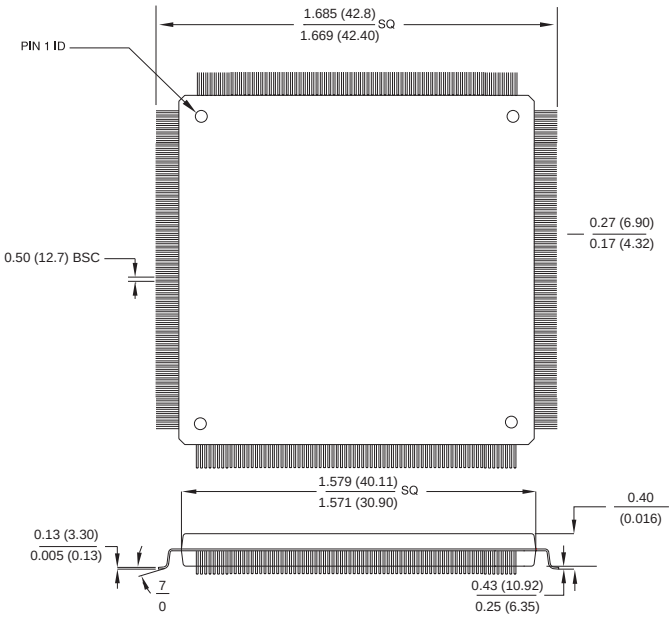
*Controlling dimension: millimeters

100RQ, 100-lead, Rectangular Plastic Gull Wing Quad Flat Pack (RQFP)
Dimensions in Millimeters and (Inches)*



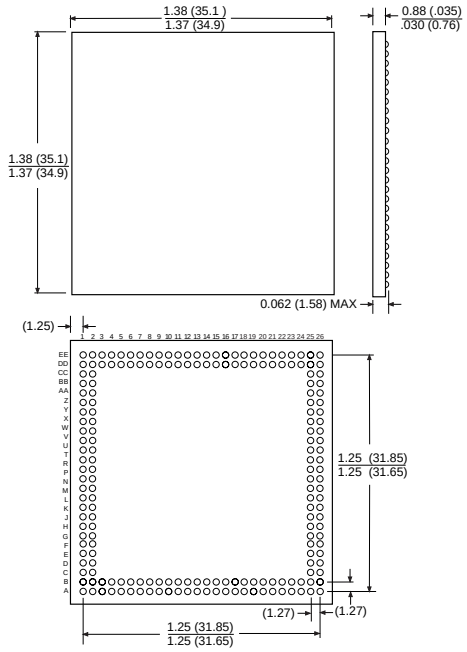
*Controlling dimension: millimeters

304Q, 304-lead, Plastic Gull Wing Quad Flat Pack (PQFP)
Dimensions in (Millimeters) and Inches



Packaging Information

352B, 352-ball Ball Grid Array (BGA)
Dimensions in (Millimeters) and Inches



432B, 432-ball Ball Grid Array (BGA)
Dimensions in (Millimeters) and Inches