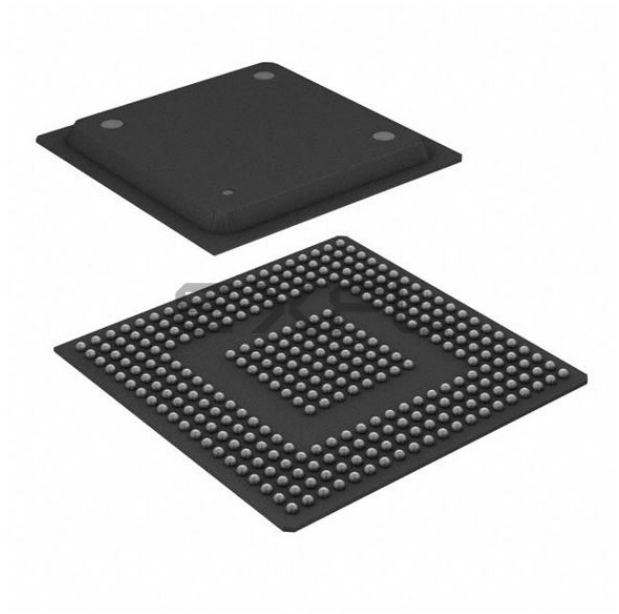
Infineon Technologies - MB91F469QAPB-GSK6E1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

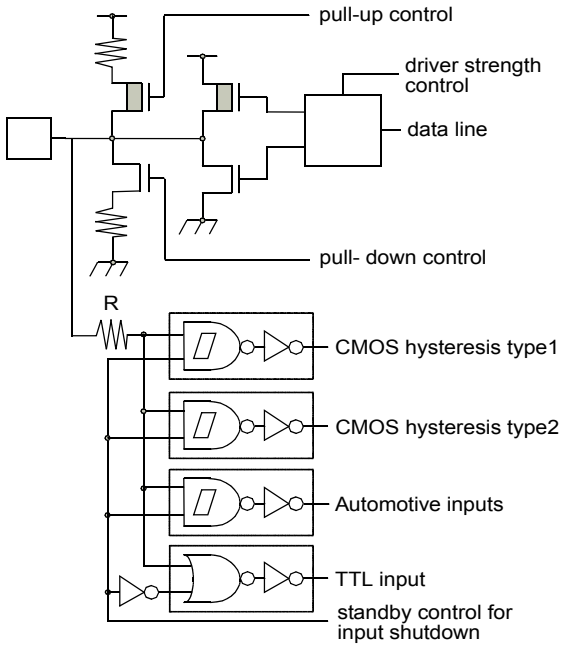
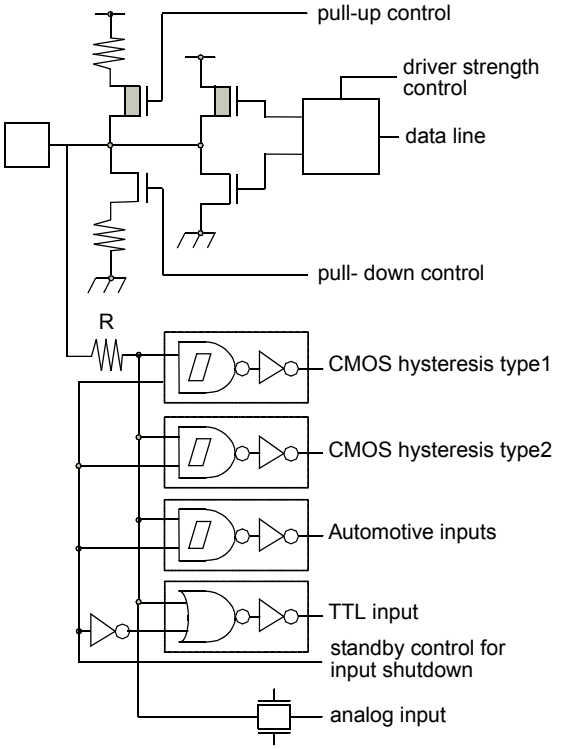
Applications of "Embedded - Microcontrollers"

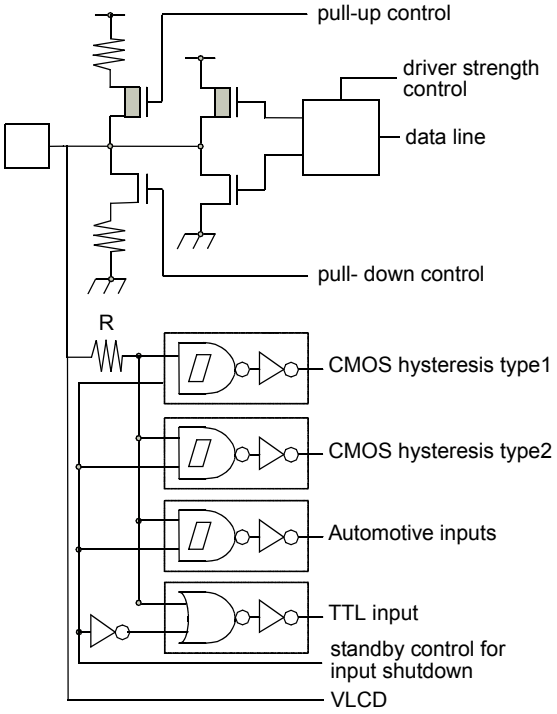
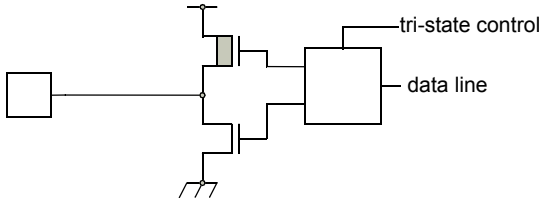
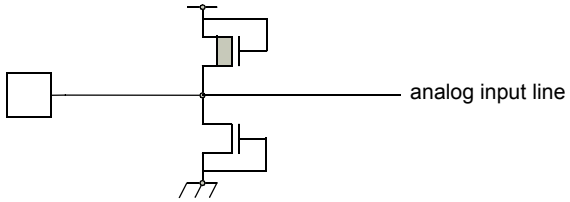
Details	
Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	205
Program Memory Size	2.0625MB (2.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	112K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 40x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	320-BBGA
Supplier Device Package	320-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f469qapb-gsk6e1

JEDEC	Pin no.	Pin name	I/O	I/O circuit type [1]	Description
C20	56	P28_3	I/O	B	General-purpose input/output port
		AN11			Analog input pin of A/D converter
B20	57	P28_5	I/O	B	General-purpose input/output port
		AN13			Analog input pin of A/D converter
A19	59	P28_7	I/O	B	General-purpose input/output port
		AN15			Analog input pin of A/D converter
A17	61	P27_2	I/O	B	General-purpose input/output port
		AN18			Analog input pin of A/D converter
		INT18			External interrupt pin
A14	64	P26_0	I/O	B	General-purpose input/output port
		AN24			Analog input pin of A/D converter
		INT24			External interrupt pin
A13	65	P35_4	I/O	A	General-purpose input/output port
		SIN9			Data input of USART9
		INT12			External interrupt input pin
A12	66	P35_5	I/O	A	General-purpose input/output port
		SOT9			Data output pin of USART9
A11	67	P22_3	I/O	A	General-purpose input/output port
		TX5			TX output pin of CAN5
A10	68	P22_6	I/O	C	General-purpose input/output port
		SDA1			I^2C bus data input/output pin (open drain)
		INT15			External interrupt input pin
		ICU8			Input capture input pin [2]
A9	69	P14_2	I/O	A	General-purpose input/output port
		ICU2			Input capture input pin
		TIN2			External trigger input pin of reload timer
		TTG10/2			External trigger input pin of PPG timer
A8	70	P14_6	I/O	A	General-purpose input/output port
		ICU6			Input capture input pin
		TIN6			Input capture input pin
		TTG14/6			External trigger input pin of PPG timer
A7	71	P16_1	I/O	A	General-purpose input/output port
		PPG9			Output pin of PPG timer
A6	72	P16_5	I/O	A	General-purpose input/output port
		PPG13			Output pin of PPG timer
		SG0			SG0 output pin of sound generator

JEDEC	Pin no.	Pin name	I/O	I/O circuit type [1]	Description
C7	201	P16_3	I/O	A	General-purpose input/output port
		PPG11			Output pin of PPG timer
C6	202	P16_7	I/O	A	General-purpose input/output port
		PPG15			Output pin of PPG timer
		ATGX			A/D converter external trigger input pin
C5	203	P15_2	I/O	A	General-purpose input/output port
		OCU2			Output compare output pin
		TOT2			Reload timer output pin
C4	204	P15_6	I/O	A	General-purpose input/output port
		OCU6			Output compare output pin
		TOT6			Reload timer output pin
E4	206	P24_7	I/O	C	General-purpose input/output port
		INT7			External interrupt input pin
		SCL3			I^2C bus clock input/output pin (open drain)
G4	208	P09_2	I/O	A	General-purpose input/output port
		CSX2			Chip select output pin
J4	210	P08_1	I/O	A	General-purpose input/output port
		WRX1			External write strobe output pin
L4	212	P07_0	I/O	A	General-purpose input/output port
		A0			Signal pin of external address bus (bit0)
M4	213	P07_4	I/O	A	General-purpose input/output port
		A4			Signal pin of external address bus (bit4)
P4	215	P06_3 A11	I/O	A	General-purpose input/output port
					Signal pin of external address bus (bit11)
T4	217	P05_2	I/O	A	General-purpose input/output port
		A18			Signal pin of external address bus (bit18)
U5	219	P03_5	I/O	A	General-purpose input/output port
		D5			Signal pin of external data bus (bit5)
U7	221	P02_4	I/O	A	General-purpose input/output port
		D12			Signal pin of external data bus (bit12)
U9	223	P01_3	I/O	A	General-purpose input/output port
		D19			Signal pin of external data bus (bit19)
U11	225	P00_2	I/O	A	General-purpose input/output port
		D26			Signal pin of external data bus (bit26)
U12	226	P10_3	I/O	A	General-purpose input/output port
		WEX			Write enable output pin
U14	228	TCK	I	I	Boundary Scan Test Clock input pin

4. I/O Circuit Types

Type	Circuit	Remarks
A		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
B		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

Type	Circuit	Remarks
L		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input LCD Voltage input
M		CMOS level tri-state output (I_{OL} = 5mA, I_{OH} = -5mA)
N		Analog input pin with protection

10.5 Poweron Sequence in parallel programming mode

The flash memory can be accessed in programming mode after a certain wait time, which is needed for Security Vector fetch:

- Minimum wait time after VDD5/VDD5R power on : 2.76 ms
- Minimum wait time after INITX rising : 1.0 ms

10.6 Flash Security

10.6.1 Vector addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the Flash Security Module:

FSV1: 0x24:8000 BSV1: 0x24:8004
FSV2: 0x24:8008 BSV2: 0x24:800C

10.6.2 Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 Kbytes sectors.

FSV1 (bit31 to bit16)

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Explanation of the bits in the Flash Security Vector FSV1 [31:16]

FSV1[31:19]	FSV1[18] Write Protection Level	FSV1[17] Write Protection	FSV1[16] Read Protection	Flash Security Mode
set all to “0”	set to “0”	set to “0”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”)
set all to “0”	set to “0”	set to “1”	set to “0”	Write Protection (all device modes, without exception)
set all to “0”	set to “0”	set to “1”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”) and Write Protection (all device modes)
set all to “0”	set to “1”	set to “0”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”)
set all to “0”	set to “1”	set to “1”	set to “0”	Write Protection (all device modes, except INTVEC mode MD[2:0] = “000”)
set all to “0”	set to “1”	set to “1”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”) and Write Protection (all device modes except INTVEC mode MD[2:0] = “000”)

10.6.3 Security Vector FSV2

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 Kbytes sectors. It is only evaluated if write protection bit FSV1 [17] is set.

Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[0]	SA8	set to “0”	set to “1”	
FSV2[1]	SA9	set to “0”	set to “1”	
FSV2[2]	SA10	set to “0”	set to “1”	
FSV2[3]	SA11	set to “0”	set to “1”	
FSV2[4]	SA12	set to “0”	set to “1”	
FSV2[5]	SA13	set to “0”	set to “1”	
FSV2[6]	SA14	set to “0”	set to “1”	
FSV2[7]	SA15	set to “0”	set to “1”	
FSV2[8]	SA16	set to “0”	set to “1”	
FSV2[9]	SA17	set to “0”	set to “1”	
FSV2[10]	SA18	set to “0”	set to “1”	
FSV2[11]	SA19	set to “0”	set to “1”	
FSV2[12]	SA20	set to “0”	set to “1”	
FSV2[13]	SA21	set to “0”	set to “1”	
FSV2[14]	SA22	set to “0”	set to “1”	
FSV2[15]	SA23	set to “0”	set to “1”	
FSV2[16]	SA24	set to “0”	set to “1”	
FSV2[17]	SA25	set to “0”	set to “1”	
FSV2[18]	SA26	set to “0”	set to “1”	
FSV2[19]	SA27	set to “0”	set to “1”	
FSV2[20]	SA28	set to “0”	set to “1”	
FSV2[21]	SA29	set to “0”	set to “1”	
FSV2[22]	SA30	set to “0”	set to “1”	
FSV2[23]	SA31	set to “0”	set to “1”	
FSV2[24]	SA32	set to “0”	set to “1”	
FSV2[25]	SA33	set to “0”	set to “1”	
FSV2[26]	SA34	set to “0”	set to “1”	
FSV2[27]	SA35	set to “0”	set to “1”	
FSV2[28]	SA36	set to “0”	set to “1”	
FSV2[29]	SA37	set to “0”	set to “1”	
FSV2[30]	SA38	set to “0”	set to “1”	
FSV2[31]	SA39	set to “0”	set to “1”	

Note : See section “Flash access in CPU mode” for an overview about the sector organization of the Flash Memory.

10.7 Notes About Flash Memory CRC Calculation

The Flash Security macro contains a feature to calculate the 32-bit checksum over addresses located in the Flash Memory address space. This feature is described in the MB91460 Series Hardware Manual, chapter 55.4.1 “Flash Security Control Register”.

Additional notes are given here:

The CRC calculation runs on the internal RC clock. It is recommended to switch the RC clock frequency to 2 MHz for shortening the calculation time. However, the CPU clock (CLKB) must be faster then RC clock, otherwise the CRC calculation may not start correctly.

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
000058_H	SCR03[R/W,W] 00000000	SMR03 [R/W,W] 00000000	SSR03 [R/W,R] 00001000	RDR03/TDR02 [R/W] 00000000	LIN-USART 3
$00005C_H$	ESCR03 [R/W] 00000X00	ECCR03 [R/W,R,W] -00000XX	reserved		
000060_H	SCR04 [R/W,W] 00000000	SMR04 [R/W,W] 00000000	SSR04 [R/W,R] 00001000	RDR04/TDR04 [R/W] 00000000	LIN-USART 4 with FIFO
000064_H	ESCR04 [R/W] 00000X00	ECCR04 [R/W,R,W] -00000XX	FSR04 [R] - - - 00000	FCR04 [R/W] 0001 - 000	
000068_H	SCR05 [R/W,W] 00000000	SMR05 [R/W,W] 00000000	SSR05 [R/W,R] 00001000	RDR05/TDR05 [R/W] 00000000	LIN-USART 5 with FIFO
$00006C_H$	ESCR05 [R/W] 00000X00	ECCR05 [R/W,R,W] -00000XX	FSR05 [R] - - - 00000	FCR05 [R/W] 0001 - 000	
000070_H	SCR06 [R/W,W] 00000000	SMR06 [R/W,W] 00000000	SSR06 [R/W,R] 00001000	RDR06/TDR06 [R/W] 00000000	LIN-USART 6 with FIFO
000074_H	ESCR06 [R/W] 00000X00	ECCR06 [R/W,R,W] -00000XX	FSR06 [R] - - - 00000	FCR06 [R/W] 0001 - 000	
000078_H	SCR07 [R/W,W] 00000000	SMR07 [R/W,W] 00000000	SSR07 [R/W,R] 00001000	RDR07/TDR07 [R/W] 00000000	LIN-USART 7 with FIFO
$00007C_H$	ESCR07 [R/W] 00000X00	ECCR07 [R/W,R,W] -00000XX	FSR07 [R] - - - 00000	FCR07 [R/W] 0001 - 000	
000080_H	BGR100 [R/W] 00000000	BGR000 [R/W] 00000000	BGR101 [R/W] 00000000	BGR001 [R/W] 00000000	Baudrate Generator LIN-USART 0-7
000084_H	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	BGR103 [R/W] 00000000	BGR003 [R/W] 00000000	
000088_H	BGR104 [R/W] 00000000	BGR004 [R/W] 00000000	BGR105 [R/W] 00000000	BGR005 [R/W] 00000000	
$00008C_H$	BGR106 [R/W] 00000000	BGR006 [R/W] 00000000	BGR107 [R/W] 00000000	BGR007 [R/W] 00000000	
000090_H - $0000CC_H$	reserved				reserved
$0000D0_H$ - 0000D8H	reserved				reserved
$0000DC_H$	IBCR1 [R/W] 00000000	IBSR1 [R] 00000000	ITBAH1 [R/W] - - - - - - 00	ITBAL1 [R/W] 00000000	I2C 1
$0000E0_H$	ITMKH1 [R/W] 00 - - - - 11	ITMKL1 [R/W] 11111111	ISMK1 [R/W] 01111111	ISBA1 [R/W] - 0000000	
$0000E4_H$	reserved	IDAR1 [R/W] 00000000	ICCR1 [R/W] 00011111	reserved	

	Register				
Address	+0	+1	+2	+3	Block
000280_H	SCR08 [R/W,W] 00000000	SMR08 [R/W,W] 00000000	SSR08 [R/W,R] 00001000	RDR08/TDR08 [R/W] 00000000	LIN-USART (FIFO) 8
000284_H	ESCR08 [R/W] 00000X00	ECCR08 [R/W,R,W] -00000XX	FSR08 [R] - - - 00000	FCR08 [R/W] 0001 - 000	
000288_H	SCR09 [R/W,W] 00000000	SMR09 [R/W,W] 00000000	SSR09 [R/W,R] 00001000	RDR09/TDR09 [R/W] 00000000	LIN-USART (FIFO) 9
$00028C_H$	ESCR09 [R/W] 00000X00	ECCR09 [R/W,R,W] -00000XX	FSR09 [R] - - - 00000	FCR09 [R/W] 0001 - 000	
000290_H	SCR10 [R/W,W] 00000000	SMR10 [R/W,W] 00000000	SSR10 [R/W,R] 00001000	RDR10/TDR10 [R/W] 00000000	LIN-USART (FIFO) 10
000294_H	ESCR10 [R/W] 00000X00	ECCR10 [R/W,R,W] -00000XX	FSR10 [R] - - - 00000	FCR10 [R/W] 0001 - 000	
000298_H	SCR11 [R/W,W] 00000000	SMR11 [R/W,W] 00000000	SSR11 [R/W,R] 00001000	RDR00/TDR00 [R/W] 00000000	LIN-USART (FIFO) 11
$00029C_H$	ESCR11 [R/W] 00000X00	ECCR11 [R/W,R,W] -00000XX	FSR11 [R] - - - 00000	FCR11 [R/W] 0001 - 000	
$0002A0_H$ - $0002BC_H$	reserved				reserved
$0002C0_H$	BGR108 [R/W] 00000000	BGR008 [R/W] 00000000	BGR109 [R/W] 00000000	BGR009 [R/W] 00000000	Baudrate Generator LIN-USART 8-11
$0002C4_H$	BGR110 [R/W] 00000000	BGR010 [R/W] 00000000	BGR111 [R/W] 00000000	BGR011 [R/W] 00000000	
$0002C8_H$ - $0002CC_H$	reserved				reserved
$0002D0_H$	reserved	ICS45 [R/W] 00000000	reserved	ICS67 [R/W] 00000000	Input Capture 4-7
$0002D4_H$	IPCP4 [R] XXXXXXXX XXXXXXXX		IPCP5 [R] XXXXXXXX XXXXXXXX		
$0002D8_H$	IPCP6 [R] XXXXXXXX XXXXXXXX		IPCP7 [R] XXXXXXXX XXXXXXXX		
$0002DC_H$	OCS45 [R/W] - - -0 - -00 0000 - -00		OCS67 [R/W] - - -0 - -00 0000 - -00		Output Compare 4-7
$0002E0_H$	OCCP4 [R/W] XXXXXXXX XXXXXXXX		OCCP5 [R/W] XXXXXXXX XXXXXXXX		
$0002E4_H$	OCCP6 [R/W] XXXXXXXX XXXXXXXX		OCCP7 [R/W] XXXXXXXX XXXXXXXX		
$0002E8_H$ - $0002EC_H$	reserved				reserved

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
000480_H	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXX – 00	CTBR [W] XXXXXXXX	Clock Control Unit
000484_H	CLKR [R/W] ---- 0000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488_H	reserved				reserved
$00048C_H$	PLLDIVM [R/W] - - - - 0000	PLLDIVN [R/W] - - 000000	PLLDIVG [R/W] - - - - 0000	PLLMULG [W] 00000000	PLL Clock Gear Unit
000490_H	PLLCTRL [R/W] - - - - 0000	reserved			
000494_H	OSCC1 [R/W] - - - - - 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] - - - - - 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control
000498_H	PORTEN [R/W] - - - - - - 00	reserved			Port Input Enable Control
$00049C_H$	reserved				reserved
$0004A0_H$	reserved	WTCER [R/W] - - - - - - 00	WTCR [R/W] 00000000 000 – 00 – 0		Watchdog Timer
$0004A4_H$	reserved	WTBR [R/W] - - - XXXXX XXXXXXXX XXXXXXXX			
$0004A8_H$	WTHR [R/W] - - - 00000	WTMR [R/W] - - 000000	WTSR [R/W] - - 000000	reserved	
$0004AC_H$	CSVTR [R/W] - - - 00010	CSVCR [R/W] 00011100	CSCFG [R/W] 0X000000	CMCFG [R/W] 00000000	Clock-Supervisor / Selector /Monitor
$0004B0_H$	CUCR [R/W] - - - - - - - - - - - 0 - - 00		CUTD [R/W] 10000000 00000000		Calibration Unit of Sub Oscillation
$0004B4_H$	CUTR1 [R] - - - - - - - - 00000000		CUTR2 [R] 00000000 00000000		
$0004B8_H$	CMPR [R/W] - - 000010 11111101		reserved	CMCR [R/W] - 001 - - 00	Clock Modulation
$0004BC_H$	CMT1 [R/W] 00000000 1 - - - 0000		CMT2 [R/W] - - 000000 - - 000000		
$0004C0_H$	CANPRE [R/W] 0 - - - 0000	CANCKD [R/W] - - 0 - - - 00[1]	reserved		CAN Clock Control
$0004C4_H$	LVSEL [R/W] 00000111	LVDET [R/W] -000 0 - 00	HWWDE [R/W] - - - - - - 00	HWWD [R/W,W] 00011000	LV Detection / Hardware-Watchdog
$0004C8_H$	OSCRH [R/W] 000 - - 001	OSCRL [R/W] - - - - - 000	WPCRH [R/W] 000 - - 000	WPCRL [R/W] - - - - - - 00	Main-/Sub-Oscillation Stabilisation Timer
$0004CC_H$	OSCCR [R/W] - - - - - - 00	reserved	REGSEL [R/W] - - 000110	REGCTR [R/W] - - - X - - 00	Main- Oscillation Standby Control Main/Sub Regulator Control

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$0004D0_H$ - $0005DC_H$	reserved				reserved
$0005E0_H$	AD1ERH [R/W] 00000000 00000000		AD1ERL [R/W] 00000000 00000000		A/D Converter 1
$0005E4_H$	AD1CS1 [R/W] 00000000	AD1CS0 [R/W] 00000000	AD1CR1 [R] 000000XX	AD1CR0 [R] XXXXXXXX	
$0005E8_H$	AD1CT1 [R/W] 00010000	AD1CT0 [R/W] 00101100	AD1SCH [R/W] - - - 00000	AD1ECH [R/W] - - - 00000	
$0005EC_H$	reserved				
$0005F0_H$	reserved	ICS89 [R/W] 00000000	reserved	reserved	Input Capture 8-9
$0005F4_H$	IPCP8 [R] XXXXXXXX XXXXXXXX		IPCP9 [R] XXXXXXXX XXXXXXXX		
$0005F8_H$	reserved		rederved		
$0005FC_H$ - 000604_H	reserved				reserved
000608_H	TCDT8 [R/W] XXXXXXXX XXXXXXXX		reserved	TCCS8 [R/W] 00000000	Free Running Timer 8 (ICU 8-9)
$00060C_H$ - $00063C_H$	reserved				reserved

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$00C140_H$	IF2CREQ1 [R/W] 00000000 00000001		IF2CMSK1 [R/W] 00000000 00000000		CAN 1 IF 2 Register
$00C144_H$	IF2MSK21 [R/W] 11111111 11111111		IF2MSK11 [R/W] 11111111 11111111		
$00C148_H$	IF2ARB21 [R/W] 00000000 00000000		IF2ARB11 [R/W] 00000000 00000000		
$00C14C_H$	IF2MCTR1 [R/W] 00000000 00000000		reserved		
$00C150_H$	IF2DTA11 [R/W] 00000000 00000000		IF2DTA21 [R/W] 00000000 00000000		
$00C154_H$	IF2DTB11 [R/W] 00000000 00000000		IF2DTB21 [R/W] 00000000 00000000		
$00C158_H$ - $00C15C_H$	reserved				reserved
$00C160_H$	IF2DTA21 [R/W] 00000000 00000000		IF2DTA11 [R/W] 00000000 00000000		CAN 1 IF 2 Register mirror
$00C164_H$	IF2DTB21 [R/W] 00000000 00000000		IF2DTB11 [R/W] 00000000 00000000		
$00C168_H$ - $00C17C_H$	reserved				reserved

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$00C580_H$	TREQR25 [R] 00000000 00000000		TREQR15 [R] 00000000 00000000		CAN 5 Status Flags
$00C584_H$	TREQR45 [R] 00000000 00000000		TREQR35 [R] 00000000 00000000		
$00C588_H$	TREQR65 [R] 00000000 00000000		TREQR55 [R] 00000000 00000000		
$00C58C_H$	TREQR85 [R] 00000000 00000000		TREQR75 [R] 00000000 00000000		
$00C590_H$	NEWDT25 [R] 00000000 00000000		NEWDT15 [R] 00000000 00000000		
$00C594_H$	NEWDT45 [R] 00000000 00000000		NEWDT35 [R] 00000000 00000000		
$00C598_H$	NEWDT65 [R] 00000000 00000000		NEWDT55 [R] 00000000 00000000		
$00C59C_H$	NEWDT85 [R] 00000000 00000000		NEWDT75 [R] 00000000 00000000		
$00C5A0_H$	INTPND25 [R] 00000000 00000000		INTPND15 [R] 00000000 00000000		
$00C5A4_H$	INTPND45 [R] 00000000 00000000		INTPND35 [R] 00000000 00000000		
$00C5A8_H$	INTPND65 [R] 00000000 00000000		INTPND55 [R] 00000000 00000000		
$00C5AC_H$	INTPND85 [R] 00000000 00000000		INTPND75 [R] 00000000 00000000		
$00C5B0_H$	MSGVAL25 [R] 00000000 00000000		MSGVAL15 [R] 00000000 00000000		
$00C5B4_H$	MSGVAL45 [R] 00000000 00000000		MSGVAL35 [R] 00000000 00000000		
$00C5B8_H$	MSGVAL65 [R] 00000000 00000000		MSGVAL55 [R] 00000000 00000000		
$00C5BC_H$	MSGVAL85 [R] 00000000 00000000		MSGVAL75 [R] 00000000 00000000		
$00C5C0_H$ - $00EFFC_H$	reserved				reserved

	Register				
Address	+0	+1	+2	+3	Block
$00F000_H$	BCTRL [R/W] -------- -------- 11111100 00000000				EDSU / MPU Control + IRQ
$00F004_H$	BSTAT [R/W] -------- -----000 00000000 10--0000				
$00F008_H$	BIAC [R] -------- -------- 00000000 00000000				
$00F00C_H$	BOAC [R] -------- -------- 00000000 00000000				
$00F010_H$	BIRQ [R/W] -------- -------- 00000000 00000000				
$00F014_H$ - $00F01C_H$	reserved				reserved
$00F020_H$	BCR0 [R/W] -------- 00000000 00000000 00000000				EDSU / MPU Control
$00F024_H$	BCR1 [R/W] -------- 00000000 00000000 00000000				
$00F028_H$	BCR2 [R/W] -------- 00000000 00000000 00000000				
$00F02C_H$	BCR3 [R/W] -------- 00000000 00000000 00000000				
$00F030_H$ - $00F07C_H$	reserved				reserved
$00F080_H$	BAD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU ch. 0
$00F084_H$	BAD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F088_H$	BAD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F08C_H$	BAD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F090_H$	BAD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU ch. 1
$00F094_H$	BAD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F098_H$	BAD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F09C_H$	BAD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

32bit read/write	dat[31:0]				dat[31:0]				Block
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
200000_H to $21FFFF_H$	SA36 (64kB)				SA37 (64kB)				ROMS10
220000_H to $23FFFF_H$	SA38 (64kB)				SA39 (64kB)				
240000_H to $243FFF_H$	SA0 (8kB)				SA1 (8kB)				
244000_H to $247FFF_H$	SA2 (8kB)				SA3 (8kB)				
248000_H to $24BFFF_H$	SA4 (8kB)				SA5 (8kB)				
$24C000_H$ to $24FFFF_H$	SA6 (8kB)				SA7 (8kB)				
250000_H to $27FFFF_H$	reserved								
280000_H to $2FFFF8_H$	External Bus Area								ROMS11
300000_H to $37FFF8_H$									ROMS12
380000_H to $3FFFF8_H$									ROMS13
400000_H to $47FFF8_H$									ROMS14
480000_H to $4FFFF8_H$									ROMS15

Note: Write operations to address $0FFFF8_H$ and $0FFFFC_H$ are not possible. When reading these addresses, the values shown above will be read.

(Continued)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Reference voltage range	AVRH	AVRH5	0.75 × $AV_{CC}5$	—	$AV_{CC}5$	V	
	AVRL	$AV_{SS}5$	$AV_{SS}5$	—	$AV_{CC}5 \times 0.25$	V	
Power supply current	I_A	$AV_{CC}5$	—	2.5	5	mA	A/D Converter active
	I_{AH}	$AV_{CC}5$	—	—	5	µA	A/D Converter not operated *1
Reference voltage current	I_R	AVRH5	—	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH5	—	—	5	µA	A/D Converter not operated *2

*1 : Supply current at $AV_{CC}5$, if A/D converter and ALARM comparator are not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)

*2 : Input current at AVRH5, if A/D converter is not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)

Sampling Time Calculation
$T_{samp} = (2.6\ kOhm + R_{EXT}) \times 11pF \times 7$; for $4.5V \leq AV_{CC}5 \leq 5.5V$
$T_{samp} = (12.1\ kOhm + R_{EXT}) \times 11pF \times 7$; for $3.0V \leq AV_{CC}5 \leq 4.5V$

Conversion Time Calculation
$T_{conv} = T_{samp} + T_{comp}$

Definition of A/D converter terms

- Resolution
  Analog variation that is recognizable by the A/D converter.
- Nonlinearity error
  Deviation between actual conversion characteristics and a straight line connecting the zero transition point ($00\ 0000\ 0000_B \leftrightarrow 00\ 0000\ 0001_B$) and the full scale transition point ($11\ 1111\ 1110_B \leftrightarrow 11\ 1111\ 1111_B$).
- Differential nonlinearity error
  Deviation of the input voltage from the ideal value that is required to change the output code by 1 LSB.
- Total error
  This error indicates the difference between actual and theoretical values, including the zero transition error, full scale transition error, and nonlinearity error.

16.7.4 I^2C AC Timings at $V_{DD}5$ = 3.0 to 5.5 V

- Conditions during AC measurements
  All AC tests were measured under the following conditions:
  - IO_{drive} = 3 mA
  - $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
  - $V_{SS}5$ = 0 V
  - Ta = − 40°C to + 105°C
  - C_l = 50 pF
  - VOL = 0.3 × $V_{DD}5$
  - VOH = 0.7 × $V_{DD}5$
  - EPILR = 0, PILR = 0 (CMOS Hysteresis 0.3 × $V_{DD}5$/0.7 × $V_{DD}5$)

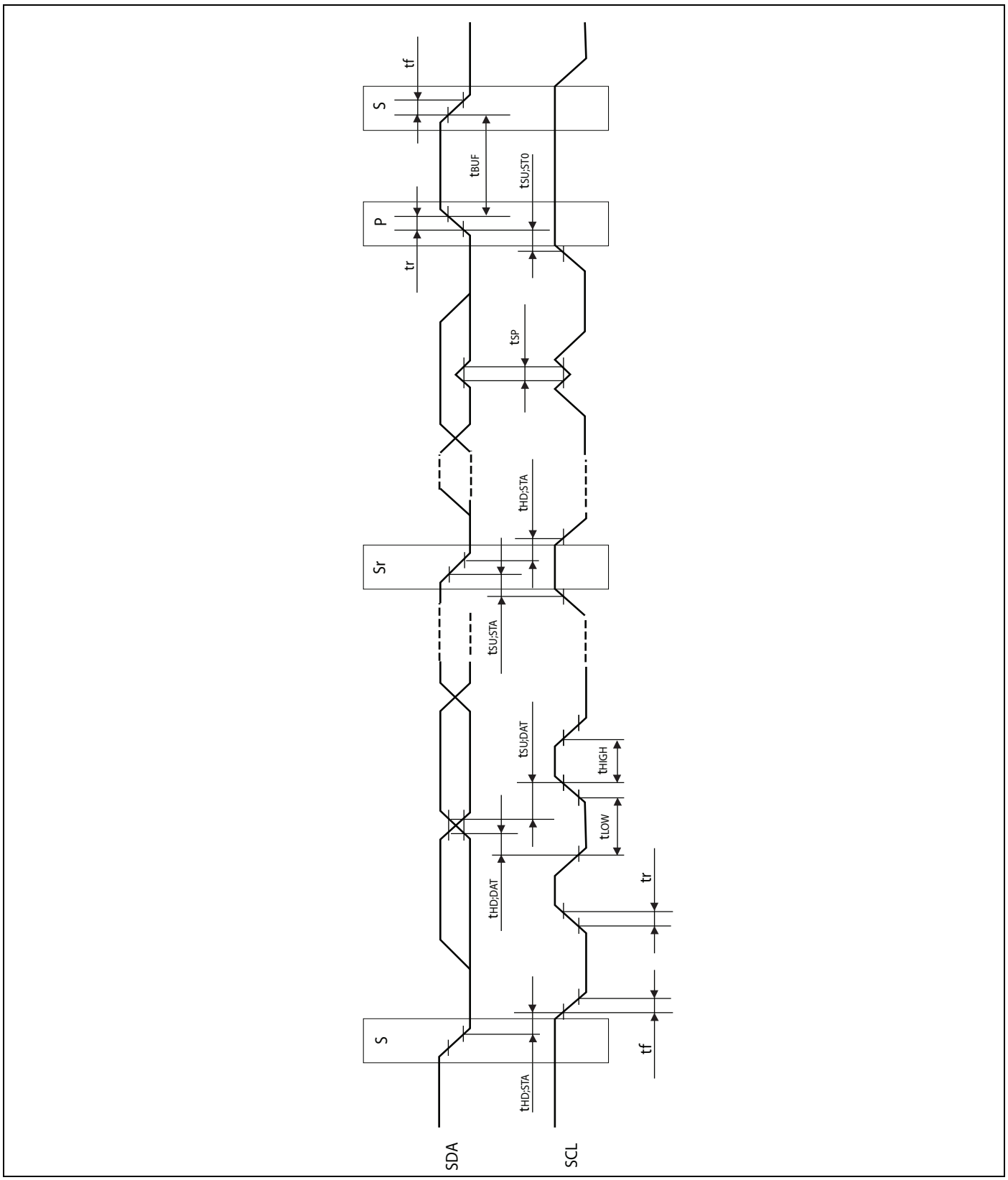
Fast mode:

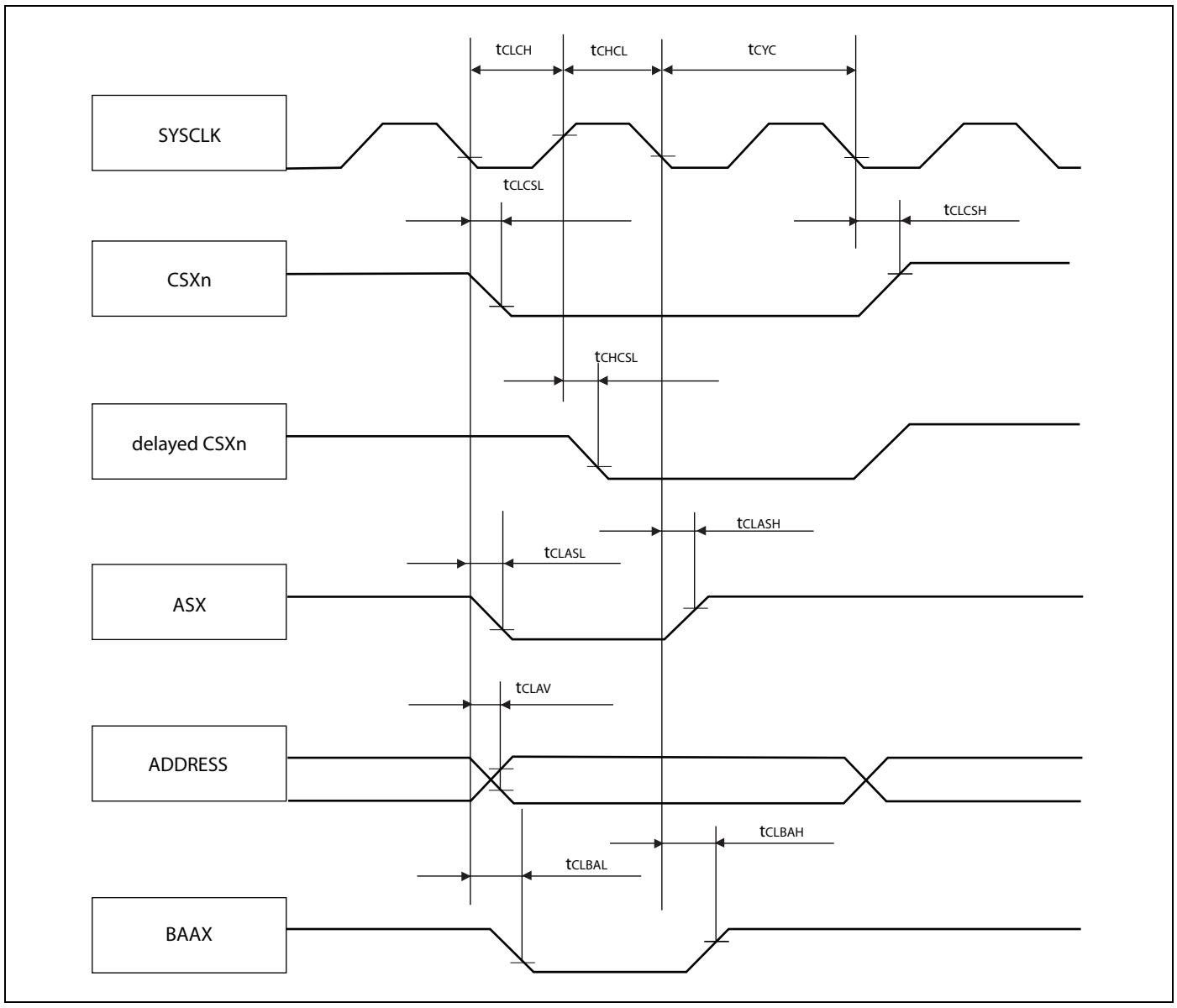
($V_{DD}5$ = 3.5 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = −40°C to + 105°C)

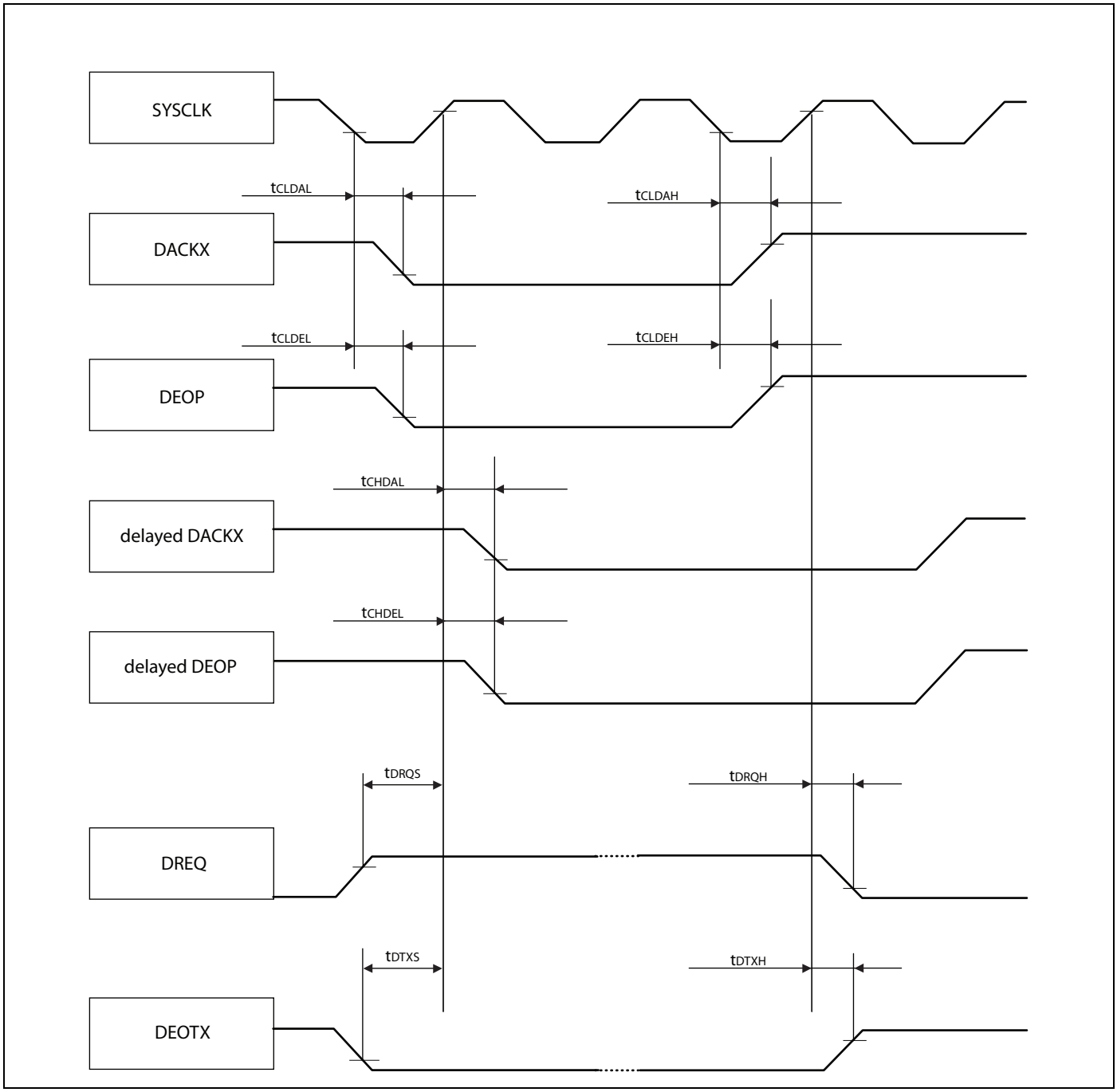
Parameter	Symbol	Pin name	Value		Unit	Remark
			Min	Max		
SCL clock frequency	f_{SCL}	SCLn	0	400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	SCLn, SDAn	0.6	—	µs	
LOW period of the SCL clock	t_{LOW}	SCLn	1.3	—	µs	
HIGH period of the SCL clock	t_{HIGH}	SCLn	0.6	—	µs	
Setup time for a repeated START condition	$t_{SU;STA}$	SCLn, SDAn	0.6	—	µs	
Data hold time for I^2C-bus devices	$t_{HD;DAT}$	SCLn, SDAn	0	0.9	µs	
Data setup time	$t_{SU;DAT}$	SCLn SDAn	100	—	ns	
Rise time of both SDA and SCL signals	t_r	SCLn, SDAn	20 + 0.1Cb	300	ns	
Fall time of both SDA and SCL signals	t_f	SCLn, SDAn	20 + 0.1Cb	300	ns	
Setup time for STOP condition	$t_{SU;STO}$	SCLn, SDAn	0.6	—	µs	
Bus free time between a STOP and START condition	t_{BUF}	SCLn, SDAn	1.3	—	µs	
Capacitive load for each bus line	C_b	SCLn, SDAn	—	400	pF	
Pulse width of spike suppressed by input filter	t_{SP}	SCLn, SDAn	0	(1..1.5) × t_{CLKP}	ns	*1

*1 : The noise filter will suppress single spikes with a pulse width of 0ns and between (1 to 1.5) cycles of peripheral clock, depending on the phase relationship between I2C signals (SDA, SCL) and peripheral clock.

Note: t_{CLKP} is the cycle time of the peripheral clock.


tf
S
tBUF
tSU;STO
P
tr
tSP
tHD;STA
Sr
tSU;STA
tSU;DAT
tHIGH
tLOW
tHD;DAT
tr
tf
S
tHD;STA
SDA
SCL


tCLCH
tCHCL
tCYC
SYSCLK
tCLCSL
tCLCSH
CSXn
tCHCSL
delayed CSXn
tCLASH
tCLASL
ASX
tCLAV
ADDRESS
tCLBAH
tCLBAL
BAAX


SYSCLK
tCLDAL
tCLDAH
DACKX
tCLDEL
tCLDEH
DEOP
tCHDAL
delayed DACKX
tCHDEL
delayed DEOP
tDRQS
tDRQH
DREQ
tDTXS
tDTXH
DEOTX