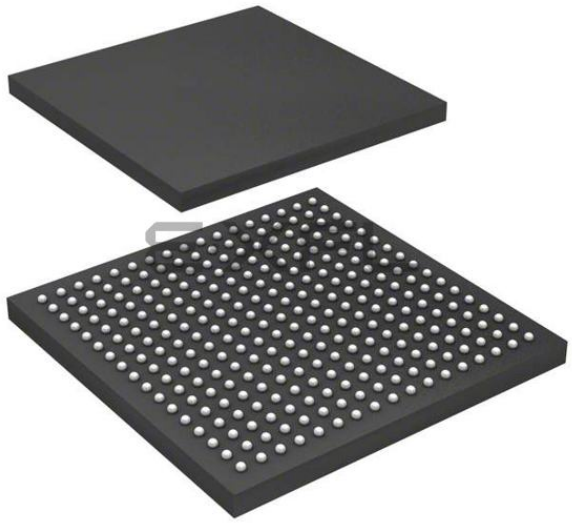

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	528MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	LVDS
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx6g1cvm05aa

2 Architectural overview

The following subsections provide an architectural overview of the i.MX 6UltraLite processor system.

2.1 Block diagram

Figure 2 shows the functional modules in the i.MX 6UltraLite processor system.

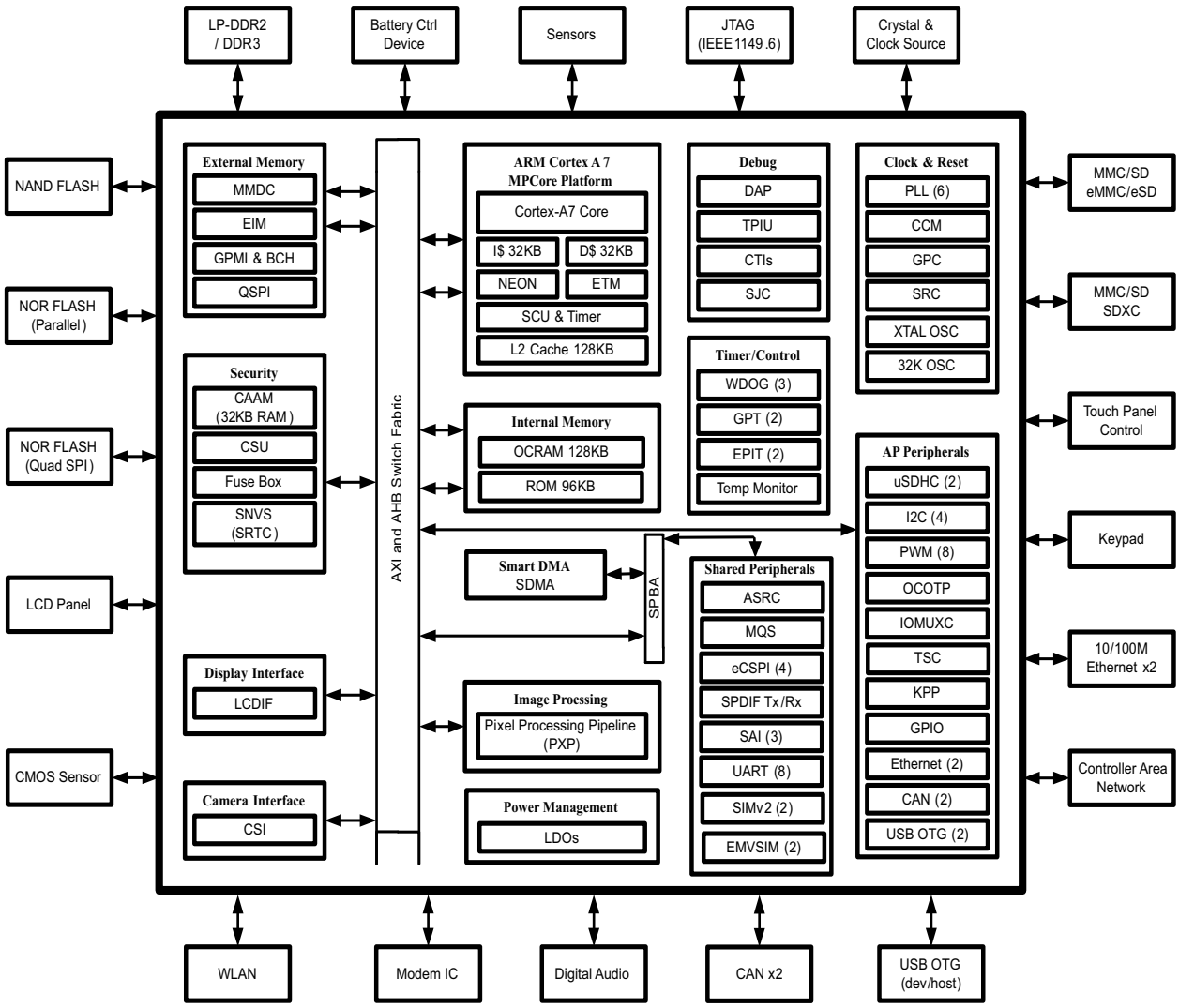

Figure 2. i.MX 6UltraLite System Block Diagram[1]

1. Some modules shown in this block diagram are not offered on all derivatives. See Table 2 for exceptions.

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A7 Core Platform.
eCSPI1 eCSPI2 eCSPI3 eCSPI4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit NOR-Flash memories, at slow frequency • Multiple chip selects
EMV SIM1 EMV SIM2	Europay, Master and Visa Subscriber Identification Module	Connectivity peripherals	EMV SIM is designed to facilitate communication to Smart Cards compatible to the EMV version 4.3 standard (Book 1) and Smart Cards compatible with ISO/IEC 7816-3 standard.
ENET1 ENET2	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100 Mbit/s Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the reference manual for details.
EPIT1 EPIT2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
FLEXCAN1 FLEXCAN2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
GPIO1 GPIO2 GPIO3 GPIO4 GPIO5	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
QSPI	Quad SPI	Connectivity peripherals	Quad SPI module act as an interface to external serial flash devices. This module contains the following features: • Flexible sequence engine to support various flash vendor devices • Single pad/Dual pad/Quad pad mode of operation • Single Data Rate/Double Data Rate mode of operation • Parallel Flash mode • DMA support • Memory mapped read access to connected flash devices • Multi-master access with priority and flexible and configurable buffer for each master
SAI1 SAI2 SAI3	—	—	The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast context-switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Support of byte-swapping • Library of Scripts and API is available
2x SIMv2	Smart Card	Connectivity peripherals	Smart card interface compliant with ISO7816.

Table 11. Operating Ranges (continued)

DDR I/O supply	NVCC_DRAM	LPDDR2	1.14	1.2	1.3	V	—
		DDR3L	1.28	1.35	1.45	V	—
		DDR3	1.43	1.5	1.575	V	—
	NVCC_DRAM2P5	—	2.25	2.5	2.75	V	—
GPIO supplies	NVCC_CSI	—	1.65	1.8, 2.8, 3.3	3.6	V	All digital I/O supplies (NVCC_xxxx) must be powered (unless otherwise specified in this data sheet) under normal conditions whether the associated I/O pins are in use or not.
	NVCC_ENET						
	NVCC_GPIO						
	NVCC_UART						
	NVCC_LCD						
	NVCC_NAND						
	NVCC_SD1						
A/D converter	VDDA_ADC_3P3	—	3.0	3.15	3.6	V	VDDA_ADC_3P3 must be powered when chip is in RUN mode, IDLE mode, or SUSPEND mode. VDDA_ADC_3P3 should not be powered when chip is in SNVS mode.
Temperature Operating Ranges							
Junction temperature	Tj	Industrial	-40	—	105	°C	See the application note, i.MX 6UltraLite Product Lifetime Usage Estimates for information on product lifetime (power-on years) for this processor.

1 Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (V_{min} + the supply tolerance). This result in an optimized power/speed ratio.

2 In setting VDD_HIGH_IN voltage, refer to the Errata ERR010690 (SNVS_LP Registers Reset Issue).

3 In setting VDD_SNVS_IN voltage with regards to Charging Currents and RTC, refer to the *i.MX 6UltraLite Hardware Development Guide* (IMX6ULHDG).

Table 12 shows on-chip LDO regulators that can supply on-chip loads.

Table 12. On-Chip LDOs[1] and their On-Chip Loads

Voltage Source	Load	Comment
VDD_HIGH_CAP	NVCC_DRAM_2P5	Board-level connection to VDD_HIGH_CAP

1 On-chip LDOs are designed to supply i.MX6UltraLite loads and must not be used to supply external loads.

4.1.4 External clock sources

Each i.MX 6UltraLite processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

4.1.6 Low power mode supply currents

Table 15 shows the current core consumption (not including I/O) of i.MX 6UltraLite processors in selected low power modes.

Table 15. Low Power Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Units
SYSTEM IDLE: LDO Enabled	• LDO_ARM and LDO_SOC are set to 1.15 V • LDO_2P5 set to 2.5 V, LDO_1P1 set to 1.1 V • CPU in WFI, CPU clock gated • DDR is in self refresh • 24 MHz XTAL is ON • 528 PLL is active, other PLLS are power down • High-speed peripheral clock gated, but remain powered	VDD_SOC_IN (1.275 V)	7.7	mA
		VDD_HIGH_IN (3.0 V)	10.5	
		VDD_SNVS_IN (3.0 V)	0.06	
		Total	41.5	mW
SYSTEM IDLE: LDO Bypassed	• LDO_ARM and LDO_SOC are set to bypass mode • LDO_2P5 set to 2.5 V, LDO_1P1 set to 1.1 V • CPU in WFI, CPU clock gated • DDR is in self refresh • 24 MHz XTAL is ON • 528 PLL is active, other PLLs are power down • High-speed peripheral clock gated, but remain powered	VDD_SOC_IN (1.15 V)	7.5	mA
		VDD_HIGH_IN (3.0 V)	9.5	
		VDD_SNVS_IN (3.0 V)	0.06	
		Total	37.3	mW
LOW POWER IDLE: LDO Enabled	• LDO_SOC is set to 1.15 V, LDO_ARM is in PG mode • LDO_2P5 and LDO_1P1 are set to weak mode • CPU in power gate mode • DDR is in self refresh • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC used as clock source • High-speed peripheral are powered off	VDD_SOC_IN (1.275 V)	3.2	mA
		VDD_HIGH_IN (3.0 V)	1.5	
		VDD_SNVS_IN (3.0 V)	0.05	
		Total	8.7	mW
LOW POWER IDLE: LDO Bypassed	• LDO_SOC is in bypass mode, LDO_ARM is in PG mode • LDO-2P5 and LDO_1P1 are set to weak mode • CPU in power gate mode • DDR is in self refresh • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC used as clock source • High-speed peripheral are powered off	VDD_SOC_IN (1.15 V)	2.8	mA
		VDD_HIGH_IN (3.0 V)	0.4	
		VDD_SNVS_IN (3.0 V)	0.05	
		Total	4.57	mW
SUSPEND (DSM)	• LDO_SOC is in bypass mode, LDO_ARM is in PG mode • LDO_2P5 and LDO_1P1 are shut off • CPU in power gate mode • DDR is in self refresh • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC is off • All clocks are shut off, except 32 kHz RTC • High-speed peripheral are powered off	VDD_SOC_IN (0.9 V)	0.44	mA
		VDD_HIGH_IN (3.0 V)	0.03	
		VDD_SNVS_IN (3.0 V)	0.03	
		Total	0.58	mW

NOTE

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the *i.MX 6UltraLite Reference Manual* (IMX6ULRM) for further details and to ensure that all necessary requirements are being met.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG1_VBUS and USB_OTG2_VBUS are not part of the power supply sequence and may be powered at any time.

4.2.2 Power-Down sequence

The following restrictions must be followed:

- VDD_SNVS_IN supply must be turned off after any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is removed after any other supply is switched off.

CAUTION

For power sequence control on VDD_HIGH_IN and VDD_SOC_IN, refer to the ERR010690 (SNVS_LP Registers Reset Issue).

4.2.3 Power supplies usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Rail” columns in pin list tables of Section 6, “Package information and contact assignments".”

4.3 Integrated LDO voltage regulator parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX 6UltraLite Reference Manual* (IMX6ULRM) for details on the power tree scheme.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO operation only.

4.8 Output buffer impedance parameters

This section defines the I/O impedance parameters of the i.MX 6UltraLite processors for the following I/O types:

- Single Voltage General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2, and DDR3/DDR3L modes

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 6).

4.9 System modules timing

This section contains the timing and electrical parameters for the modules in each i.MX 6UltraLite processor.

4.9.1 Reset timings parameters

Figure 7 shows the reset timing and Table 36 lists the timing parameters.

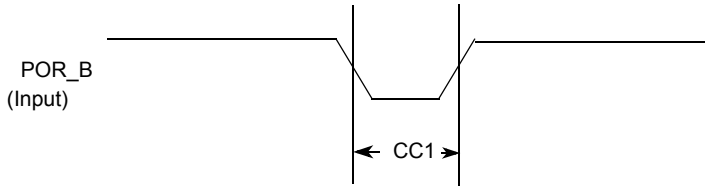

Figure 7. Reset Timing Diagram

Table 36. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid.	1	—	RTC_XTALI cycle

4.9.2 WDOG reset timing parameters

Figure 8 shows the WDOG reset timing and Table 37 lists the timing parameters.

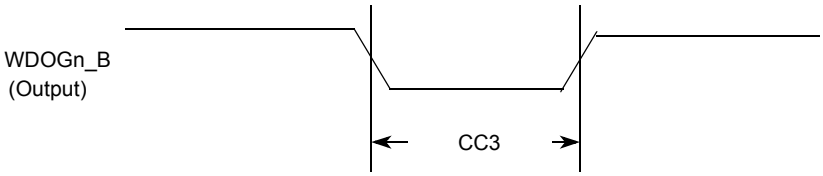

Figure 8. WDOGn_B Timing Diagram

Table 37. WDOGn_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOGn_B Assertion	1	—	RTC_XTALI cycle

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 µs.

NOTE

WDOG1_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

4.9.3.2 General EIM timing-synchronous mode

Figure 9, Figure 10, and Table 39 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the EIM_BCLK rising edge according to corresponding assertion/negation control fields.

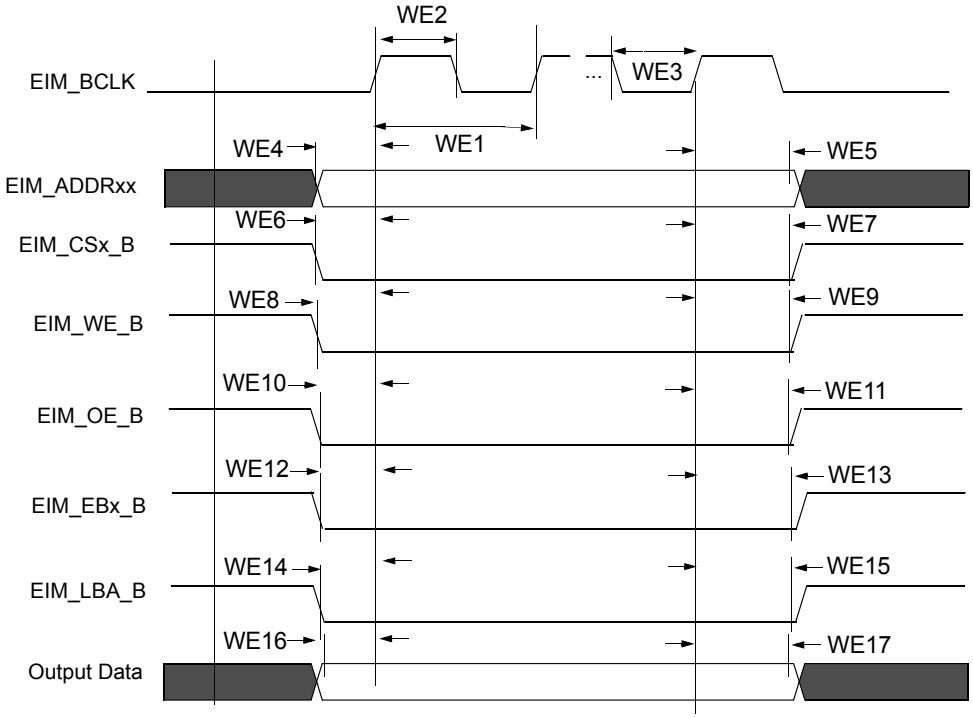

Figure 9. EIM Outputs Timing Diagram

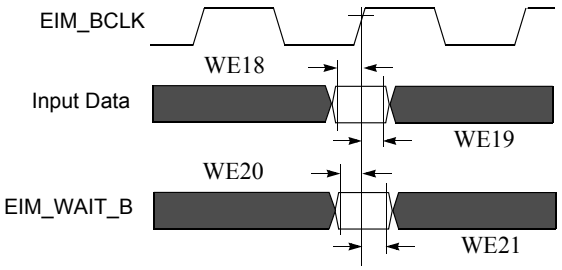

Figure 10. EIM Inputs Timing Diagram

4.9.3.3 Examples of EIM synchronous accesses

Table 39. EIM Bus Timing Parameters

ID	Parameter	Min[1]	Max[1]	Unit
WE1	EIM_BCLK Cycle time[2]	t x (k + 1)	—	ns
WE2	EIM_BCLK Low Level Width	0.4 x t x (k + 1)	—	ns
WE3	EIM_BCLK High Level Width	0.4 x t x (k + 1)	—	ns
WE4	Clock rise to address valid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns

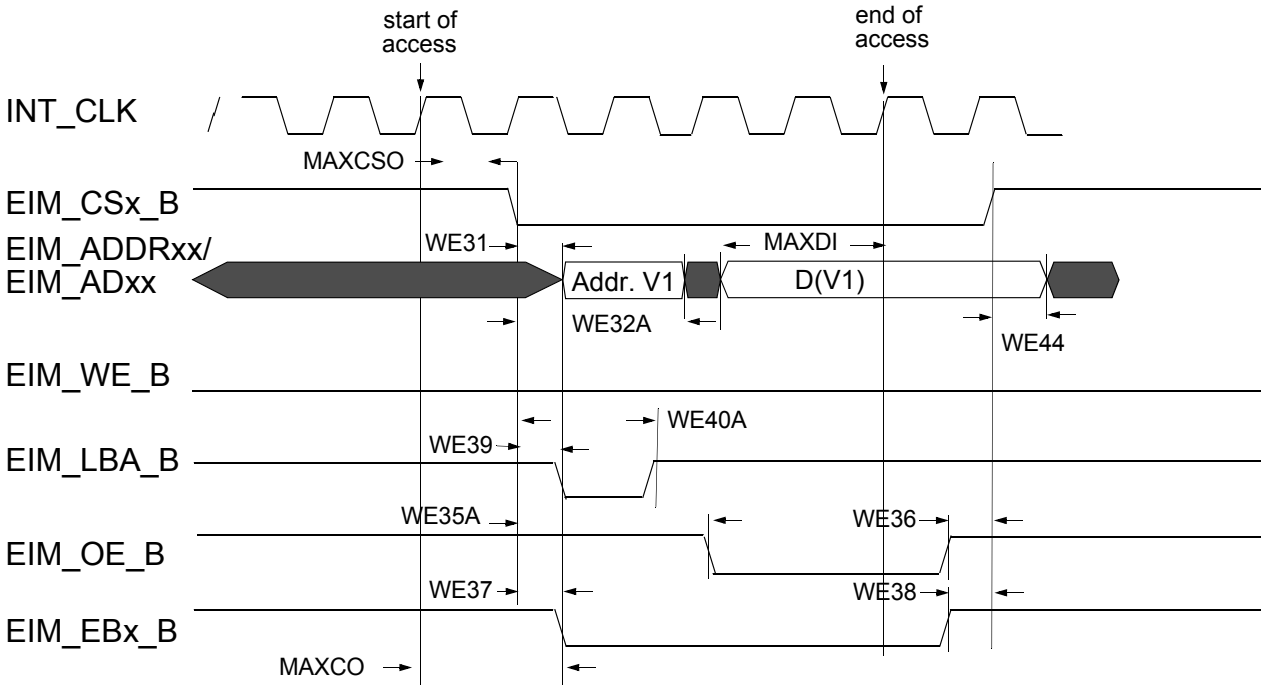

Figure 16. Asynchronous A/D Muxed Read Access (RWSC = 5)

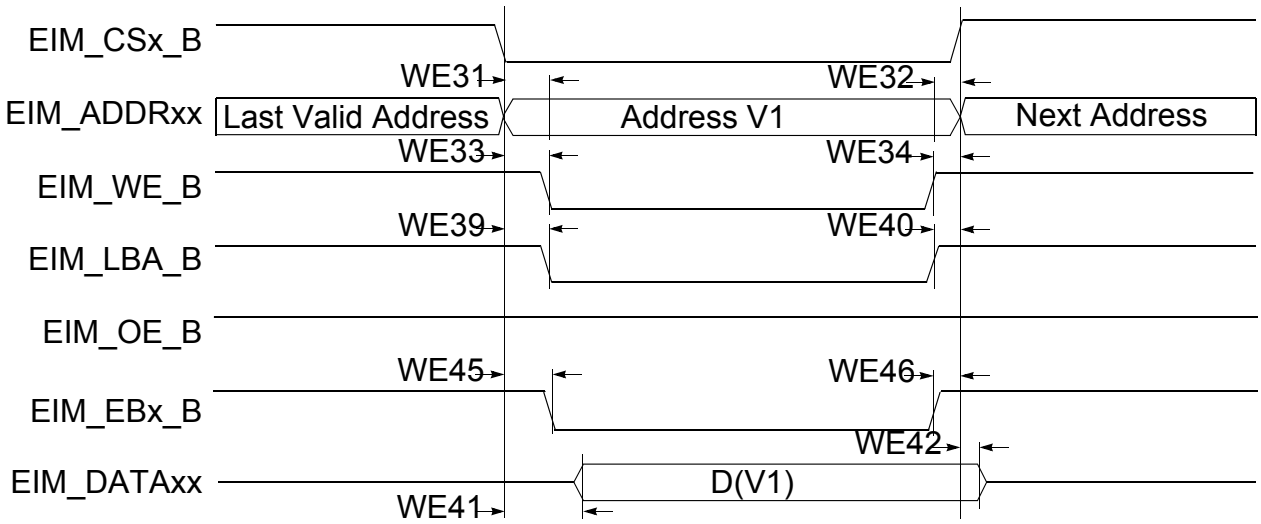

Figure 17. Asynchronous Memory Write Access

(VSYNC), then CSI_HSYNC (HSYNC) is asserted and holds for the entire line. The pixel clock, CSI_PIXCLK (PIXCLK), is valid as long as HSYNC is asserted.

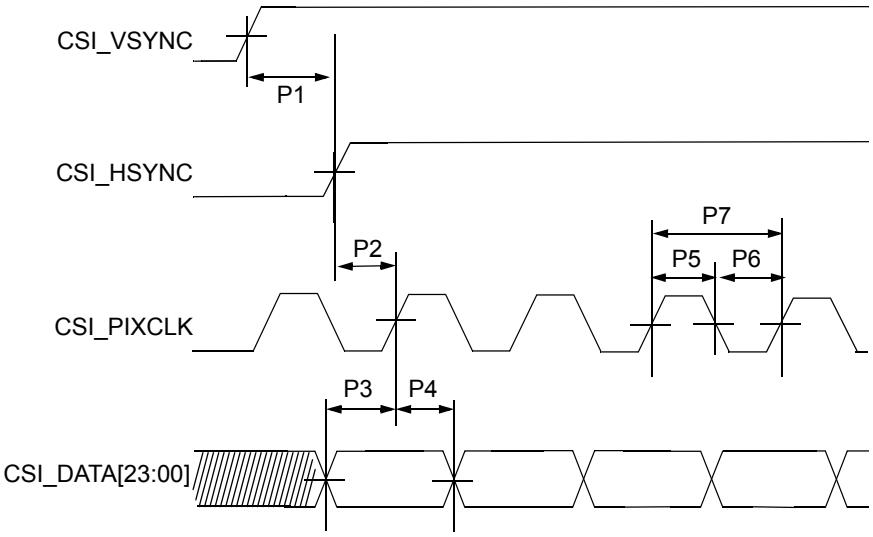

Figure 32. CSI Gated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

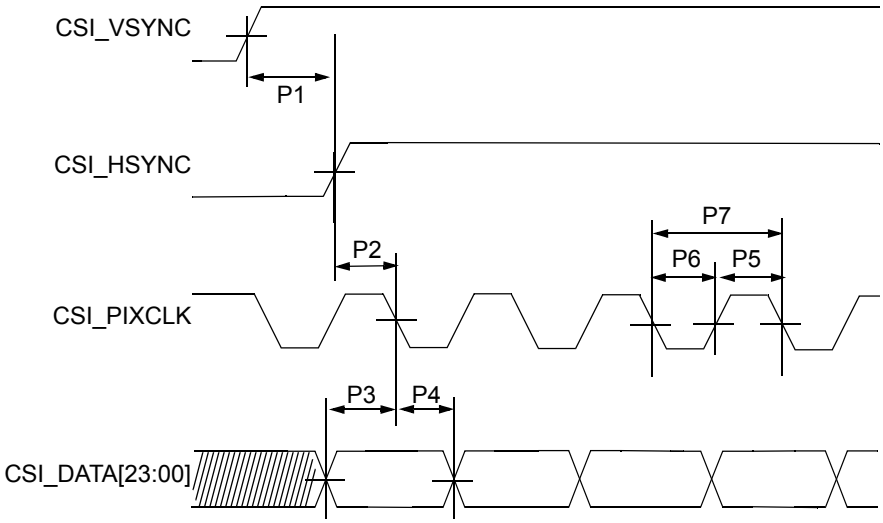

Figure 33. CSI Gated Clock Mode—Sensor Data at Rising Edge, Latch Data at Falling Edge

Table 45. CSI Gated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI_VSYNC to CSI_HSYNC time	tV2H	33.5	—	ns
P2	CSI_HSYNC setup time	tHsu	1	—	ns
P3	CSI DATA setup time	tDsu	1	—	ns

Table 45. CSI Gated Clock Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Units
P4	CSI DATA hold time	tDh	1	—	ns
P5	CSI pixel clock high time	tCLKh	3.75	—	ns
P6	CSI pixel clock low time	tCLKl	3.75	—	ns
P7	CSI pixel clock frequency	fCLK	—	133	MHz

4.12.1.0.2 Ungated clock mode timing

Figure 34 shows the ungated clock mode timings of CSI, and Table 46 describes the timing parameters (P1–P6) that are shown in the figure. In ungated mode the CSI_VSYNC and CSI_PIXCLK signals are used, and the CSI_HSYNC signal is ignored.

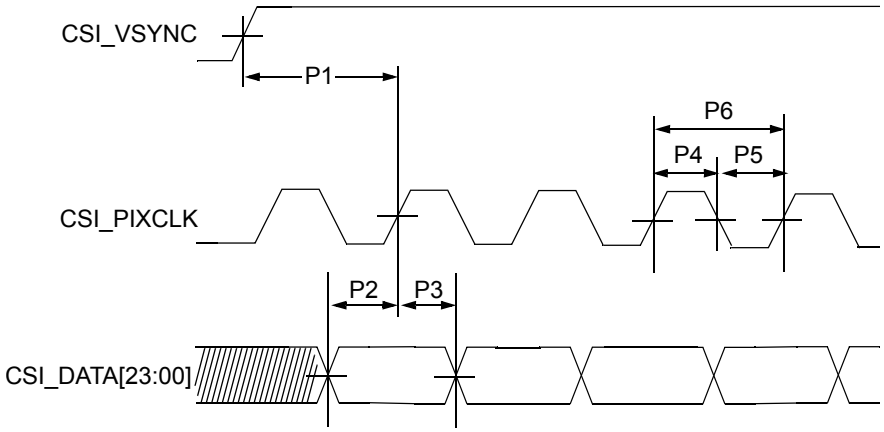

Figure 34. CSI Ungated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

Table 46. CSI Ungated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI_VSYNC to pixel clock time	tVSYNC	33.5	—	ns
P2	CSI DATA setup time	tDsu	1	—	ns
P3	CSI DATA hold time	tDh	1	—	ns
P4	CSI pixel clock high time	tCLKh	3.75	—	ns
P5	CSI pixel clock low time	tCLKl	3.75	—	ns
P6	CSI pixel clock frequency	fCLK	—	133	MHz

The CSI enables the chip to connect directly to external CMOS image sensors, which are classified as dumb or smart as follows:

- Dumb sensors only support traditional sensor timing (vertical sync (VSYNC) and horizontal sync (HSYNC)) and output-only Bayer and statistics data.
- Smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

4.12.4.1.4 MII serial management channel timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 44 shows MII asynchronous input timings. Table 56 describes the timing parameters (M10–M15) shown in the figure.

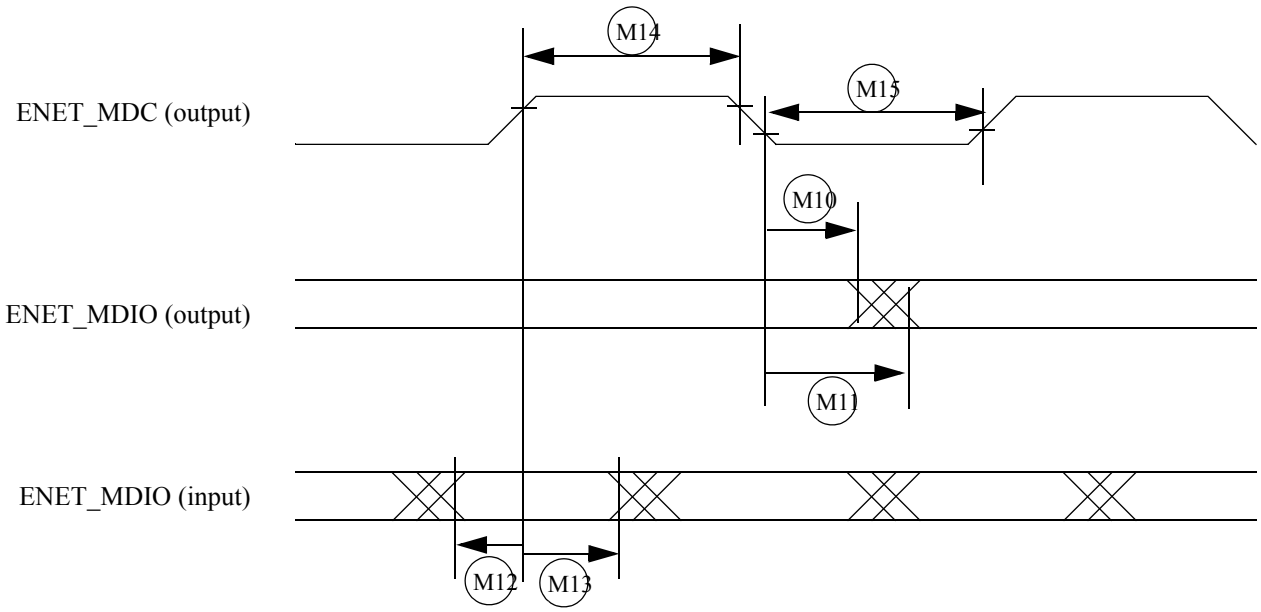

Figure 44. MII Serial Management Channel Timing Diagram

Table 56. MII Serial Management Channel Timing

ID	Characteristic	Min.	Max.	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

4.12.4.2 RMII mode timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the ENET_RX_EN in RMII. Other signals under RMII mode include ENET_TX_EN, ENET_TX_DATA[1:0], ENET_RX_DATA[1:0] and ENET_RX_ER.

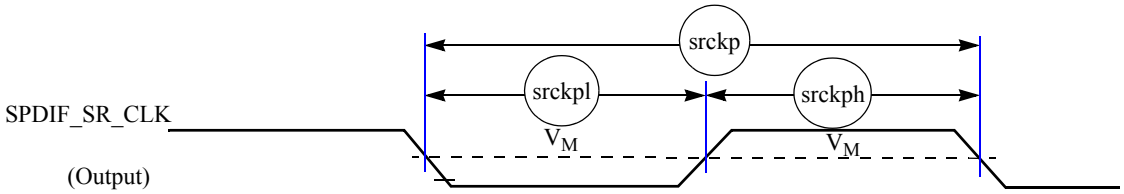

Figure 61. SPDIF_SR_CLK Timing Diagram

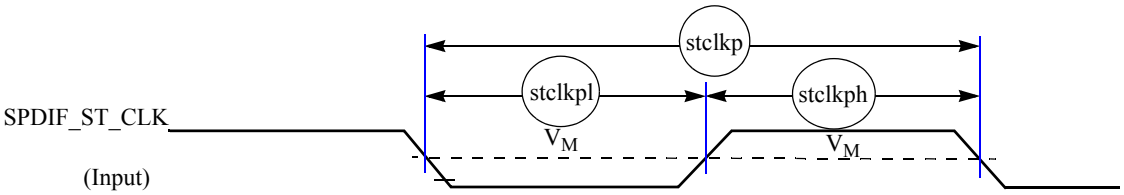

Figure 62. SPDIF_ST_CLK Timing Diagram

4.12.13 UART I/O configuration and timing parameters

4.12.13.1 UART RS-232 serial mode timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.12.13.1.1 UART transmitter

Figure 63 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 72 lists the UART RS-232 serial mode transmits timing characteristics.

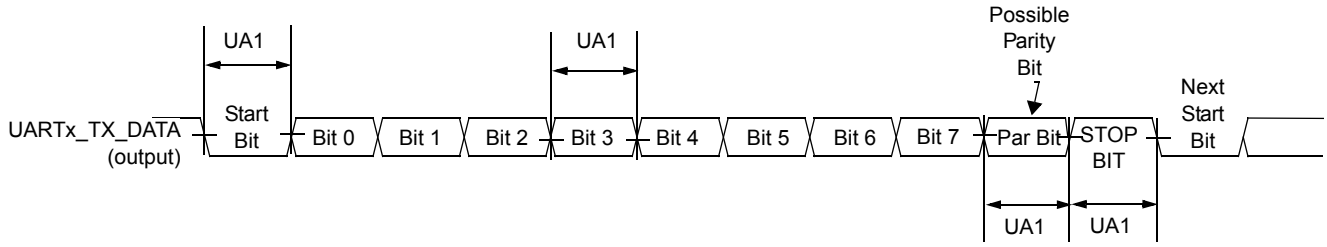

Figure 63. UART RS-232 Serial Mode Transmit Timing Diagram

Table 72. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] - T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

Table 78. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at reset	eFuse name	Details
LCD_DATA00	Input with 100 K pull-down	BT_CFG1[0]	Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
LCD_DATA01	Input with 100 K pull-down	BT_CFG1[1]	
LCD_DATA02	Input with 100 K pull-down	BT_CFG1[2]	
LCD_DATA03	Input with 100 K pull-down	BT_CFG1[3]	
LCD_DATA04	Input with 100 K pull-down	BT_CFG1[4]	
LCD_DATA05	Input with 100 K pull-down	BT_CFG1[5]	
LCD_DATA06	Input with 100 K pull-down	BT_CFG1[6]	
LCD_DATA07	Input with 100 K pull-down	BT_CFG1[7]	
LCD_DATA08	Input with 100 K pull-down	BT_CFG2[0]	
LCD_DATA09	Input with 100 K pull-down	BT_CFG2[1]	
LCD_DATA10	Input with 100 K pull-down	BT_CFG2[2]	
LCD_DATA11	Input with 100 K pull-down	BT_CFG2[3]	
LCD_DATA12	Input with 100 K pull-down	BT_CFG2[4]	
LCD_DATA13	Input with 100 K pull-down	BT_CFG2[5]	
LCD_DATA14	Input with 100 K pull-down	BT_CFG2[6]	
LCD_DATA15	Input with 100 K pull-down	BT_CFG2[7]	
LCD_DATA16	Input with 100 K pull-down	BT_CFG4[0]	
LCD_DATA17	Input with 100 K pull-down	BT_CFG4[1]	
LCD_DATA18	Input with 100 K pull-down	BT_CFG4[2]	
LCD_DATA19	Input with 100 K pull-down	BT_CFG4[3]	
LCD_DATA20	Input with 100 K pull-down	BT_CFG4[4]	
LCD_DATA21	Input with 100 K pull-down	BT_CFG4[5]	
LCD_DATA22	Input with 100 K pull-down	BT_CFG4[6]	
LCD_DATA23	Input with 100 K pull-down	BT_CFG4[7]	

5.2 Boot device interface allocation

The following tables list the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The tables also describe the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 79. QSPI Boot trough QSPI

Ball Name	Signal Name	Mux Mode	Common	Quad Mode	+ Port A DQS	+ Port A CS1	+ Port B	+ Port B DQS	+ Port B CS1
NAND_WP_B	qspi.A_SCLK	Alt2	Yes	Yes					
NAND_DQS	qspi.A_SS0_B	Alt2	Yes	Yes					

Table 84. NAND Boot through GPMI (continued)

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG1[3:2]= 01b	BOOT_CFG1[3:2]= 10b
NAND_DATA00	rawnand.DATA00	Alt 0	Yes		
NAND_DATA01	rawnand.DATA01	Alt 0	Yes		
NAND_DATA02	rawnand.DATA02	Alt 0	Yes		
NAND_DATA03	rawnand.DATA03	Alt 0	Yes		
NAND_DATA04	rawnand.DATA04	Alt 0	Yes		
NAND_DATA05	rawnand.DATA05	Alt 0	Yes		
NAND_DATA06	rawnand.DATA06	Alt 0	Yes		
NAND_DATA07	rawnand.DATA07	Alt 0	Yes		
NAND_DQS	rawnand.DQS	Alt 0	Yes		
CSI_MCLK	rawnand.CE2_B	Alt 2			Yes
CSI_PIXCLK	rawnand.CE3_B	Alt 2			Yes

Table 85. SD/MMC Boot through USDHC1

Ball Name	Signal Name	Mux Mode	Common	4-bit	8-bit	BOOT_CFG1[1]=1 (SD Power Cycle)	SDMMC MFG mode
UART1_RTS_B	usdhc1.CD_B	Alt 2					Yes
SD1_CLK	usdhc1.CLK	Alt 0	Yes				
SD1_CMD	usdhc1.CMD	Alt 0	Yes				
SD1_DATA0	usdhc1.DATA0	Alt 0	Yes				
SD1_DATA1	usdhc1.DATA1	Alt 0		Yes	Yes		
SD1_DATA2	usdhc1.DATA2	Alt 0		Yes	Yes		
SD1_DATA3	usdhc1.DATA3	Alt 0	Yes				
NAND_READY_B	usdhc1.DATA4	Alt 1			Yes		
NAND_CE0_B	usdhc1.DATA5	Alt 1			Yes		
NAND_CE1_B	usdhc1.DATA6	Alt 1			Yes		
NAND_CLE	usdhc1.DATA7	Alt 1			Yes		
GPIO1_IO09	usdhc1.RESET_B	Alt 5				Yes	
GPIO1_IO05	usdhc1.VSELECT	Alt 4				Yes	

6 Package information and contact assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 14x14 mm package information

6.1.1 14x14 mm, 0.8 mm pitch, ball matrix

Figure 68 shows the top, bottom, and side views of the 14x14 mm BGA package.

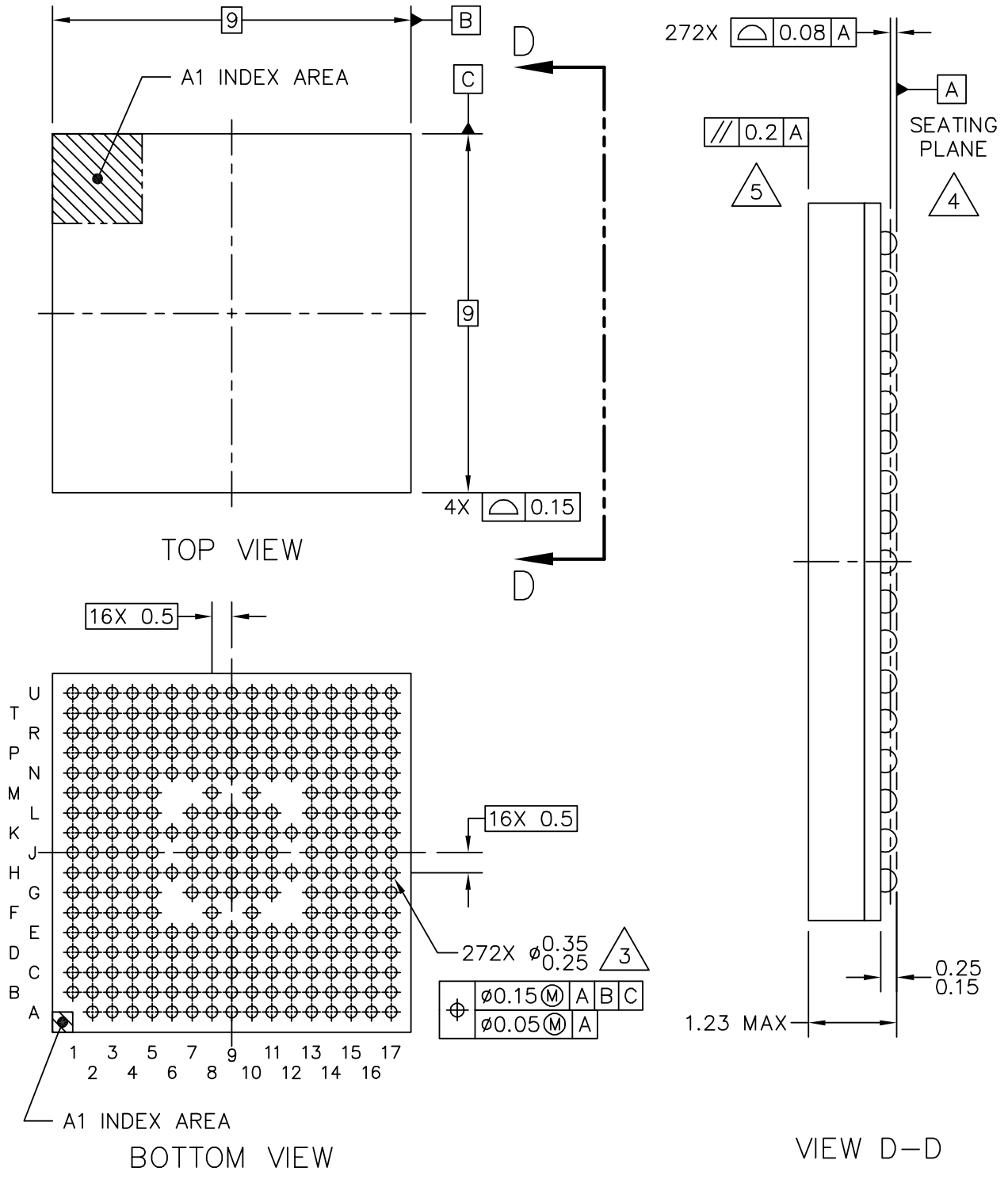

Figure 69. 9X9 mm BGA, Case x Package Top, Bottom, and Side Views

Table 94. 9x9 mm Functional Contact Assignments (continued)

DRAM_ADDR07	J4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR07	Output	100 kΩ pull-up
DRAM_ADDR08	J5	NVCC_DRAM	DDR	ALT0	DRAM_ADDR08	Output	100 kΩ pull-up
DRAM_ADDR09	J1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR09	Output	100 kΩ pull-up
DRAM_ADDR10	M2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR10	Output	100 kΩ pull-up
DRAM_ADDR11	K5	NVCC_DRAM	DDR	ALT0	DRAM_ADDR11	Output	100 kΩ pull-up
DRAM_ADDR12	L3	NVCC_DRAM	DDR	ALT0	DRAM_ADDR12	Output	100 kΩ pull-up
DRAM_ADDR13	H4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR13	Output	100 kΩ pull-up
DRAM_ADDR14	E3	NVCC_DRAM	DDR	ALT0	DRAM_ADDR14	Output	100 kΩ pull-up
DRAM_ADDR15	E2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR15	Output	100 kΩ pull-up
DRAM_CAS_B	G4	NVCC_DRAM	DDR	ALT0	DRAM_CAS_B	Output	100 kΩ pull-up
DRAM_CS0_B	L1	NVCC_DRAM	DDR	ALT0	DRAM_CS0_B	Output	100 kΩ pull-up
DRAM_CS1_B	H5	NVCC_DRAM	DDR	ALT0	DRAM_CS1_B	Output	100 kΩ pull-up
DRAM_DATA00	T3	NVCC_DRAM	DDR	ALT0	DRAM_DATA00	Input	100 kΩ pull-up
DRAM_DATA01	N5	NVCC_DRAM	DDR	ALT0	DRAM_DATA01	Input	100 kΩ pull-up
DRAM_DATA02	T4	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	100 kΩ pull-up
DRAM_DATA03	T5	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	100 kΩ pull-up
DRAM_DATA04	U5	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	100 kΩ pull-up
DRAM_DATA05	T6	NVCC_DRAM	DDR	ALT0	DRAM_DATA05	Input	100 kΩ pull-up
DRAM_DATA06	R4	NVCC_DRAM	DDR	ALT0	DRAM_DATA06	Input	100 kΩ pull-up
DRAM_DATA07	U3	NVCC_DRAM	DDR	ALT0	DRAM_DATA07	Input	100 kΩ pull-up
DRAM_DATA08	P1	NVCC_DRAM	DDR	ALT0	DRAM_DATA08	Input	100 kΩ pull-up

Table 96. GPIO Behaviors during Reset (continued)[1]

Ball Name	Mux Mode	Function	Input/Output	Value
LCD_DATA10	ALT6	SRC_BT_CFG[10]	Input	100 kΩ pull-down
LCD_DATA11	ALT6	SRC_BT_CFG[11]	Input	100 kΩ pull-down
LCD_DATA12	ALT6	SRC_BT_CFG[12]	Input	100 kΩ pull-down
LCD_DATA13	ALT6	SRC_BT_CFG[13]	Input	100 kΩ pull-down
LCD_DATA14	ALT6	SRC_BT_CFG[14]	Input	100 kΩ pull-down
LCD_DATA15	ALT6	SRC_BT_CFG[15]	Input	100 kΩ pull-down
LCD_DATA16	ALT6	SRC_BT_CFG[16]	Input	100 kΩ pull-down
LCD_DATA17	ALT6	SRC_BT_CFG[17]	Input	100 kΩ pull-down
LCD_DATA18	ALT6	SRC_BT_CFG[18]	Input	100 kΩ pull-down
LCD_DATA19	ALT6	SRC_BT_CFG[19]	Input	100 kΩ pull-down
LCD_DATA20	ALT6	SRC_BT_CFG[20]	Input	100 kΩ pull-down
LCD_DATA21	ALT6	SRC_BT_CFG[21]	Input	100 kΩ pull-down
LCD_DATA22	ALT6	SRC_BT_CFG[22]	Input	100 kΩ pull-down
LCD_DATA23	ALT6	SRC_BT_CFG[23]	Input	100 kΩ pull-down

1 Others are same as value in the column “Out of Reset Condition” of Table 91 and Table 94.