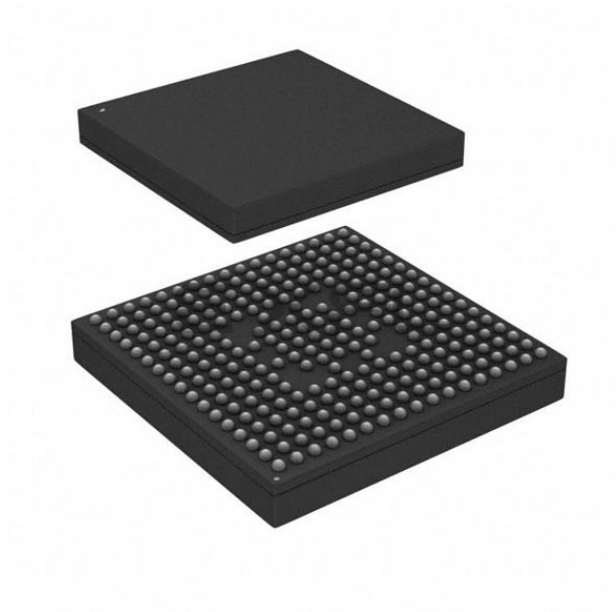

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	528MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	LCD, LVDS
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	272-LFBGA
Supplier Device Package	272-MAPBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6g2cvk05aa

- IoT Gateway
- Access control panels
- Human Machine Interfaces (HMI)
- Smart appliances

The features of the i.MX 6UltraLite processor include[1]:

- Single-core ARM Cortex-A7—The single core A7 provides a cost-effective and power-efficient solution.
- Multilevel memory system—The multilevel memory system of each device is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The device supports many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, NAND Flash (MLC and SLC), OneNAND™, Quad SPI, and managed NAND, including eMMC up to rev 4.4/4.41/4.5.
- Smart speed technology—Power management implemented throughout the IC that enables multimedia features and peripherals to consume minimum power in both active and various low power modes.
- Dynamic voltage and frequency scaling—The processor improves the power efficiency by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—Multimedia performance is enhanced by a multilevel cache system, NEON™ MPE (Media Processor Engine) co-processor, a programmable smart DMA (SDMA) controller, an asynchronous audio sample rate converter, and a Pixel processing pipeline (PXP) to support 2D image processing, including color-space conversion, scaling, alpha-blending, and rotation.
- Ethernet interfaces—10/100 Mbps Ethernet controllers.
- Human-machine interface—Support one digital parallel display interface.
- Interface flexibility—Each processor supports connections to a variety of interfaces: High-speed USB on-the-go with PHY, multiple expansion card port (high-speed MMC/SDIO host and other), 12-bit ADC module, CAN port, smart card interface compatible with EMV Standard v4.3, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio).
- Advanced security—The processor deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the *i.MX 6UltraLite Security Reference Manual* (IMX6ULSRM).
- Integrated power management—The processor integrates linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

For a comprehensive list of the i.MX 6UltraLite features, see Section 1.2, “Features"”.

1. The actual feature set depends on the part numbers as described in the Table 1 and Table 2.

Table 2. Detailed Peripherals Information (continued)[1,2,3]

Peripheral Name	Instance	G0	G1	G2	G3
SDIO	uSDHC1	Y	Y	Y	Y
	uSDHC2	Y	Y	Y	Y
UART	UART1	Y	Y	Y	Y
	UART2	Y	Y	Y	Y
	UART3	Y	Y	Y	Y
	UART4	Y	Y	Y	Y
	UART5	NA	Y	Y	Y
	UART6	NA	Y	Y	Y
	UART7	NA	Y	Y	Y
	UART8	NA	Y	Y	Y
ISO7816-3	SIM1	NA	Y	Y	Y
	SIM2	NA	Y	Y	Y
I2C	I2C1	Y	Y	Y	Y
	I2C2	Y	Y	Y	Y
	I2C3	NA	Y	Y	Y
	I2C4	NA	Y	Y	Y
SPI	ECSPI1	Y	Y	Y	Y
	ECSPI2	Y	Y	Y	Y
	ECSPI3	NA	Y	Y	Y
	ECSPI4	NA	Y	Y	Y
I2S/SAI	SAI1	Y	Y	Y	Y
	SAI2	NA	Y	Y	Y
	SAI3	NA	Y	Y	Y

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistances between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

7 Thermal resistance between the die and the central solder balls on the bottom of the package based on simulation.

4.1.3 Operating ranges

Table 11 provides the operating ranges of the i.MX 6UltraLite processors. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

Table 11. Operating Ranges

Parameter Description	Symbol	Operating Conditions	Min	Typ	Max[1]	Unit	Comment
Run Mode: LDO Enabled	VDD_SOC_IN	—	1.275	—	1.5	V	VDD_SOC_IN must be 125 mV higher than the LDO Output Set Point (VDD_ARM_CAP and VDD_SOC_CAP) for correct supply voltage regulation.
	VDD_ARM_CAP	A7 core at 528 MHz	1.15	—	1.3	V	Output voltage must be set to the following rules: • VDD_ARM_CAP <= VDD_SOC_CAP • VDD_SOC_CAP - VDD_ARM_CAP < 330 mV
		A7 core at 396 MHz	1.00	—	1.3		
		A7 core at 198 MHz	0.925	—	1.3		
	VDD_SOC_CAP	—	1.15	—	1.3	V	—
Run Mode: LDO Bypassed	VDD_SOC_IN	A7 core operation at 528 MHz or below	1.15	—	1.3	V	A7 core operation above 528 MHz is not supported when LDO is bypassed.
SUSPEND (DSM) Mode	VDD_SOC_IN	—	0.90	—	1.3	V	Refer to Table 15 Low Power Mode Current and Power Consumption on page 15
VDD_HIGH internal Regulator	VDD_HIGH_IN[2]	—	2.80	—	3.6	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[3]	—	2.40	—	3.6	V	Can be combined with VDDHIGH_IN, if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG1_VBUS	—	4.40	—	5.5	V	—
	USB_OTG2_VBUS	—	4.40	—	5.5	V	—

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can be used instead of the RTC_XTALI if accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

Table 13 shows the interface frequency requirements.

Table 13. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1,2]	f_{ckil}	—	32.768[3]/32.0	—	kHz
XTALI Oscillator[2,4]	f_{xtal}	—	24	—	MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 The required frequency stability of this clock source is application dependent. For recommendations, see the Hardware Development Guide for *i.MX 6UltraLite Applications Processors* (IMX6ULHDG).

3 Recommended nominal frequency 32.768 kHz.

4 External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 13 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available.

- On-chip 40 kHz ring oscillator—this clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit:
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision time-out.

4.1.5 Maximum supply currents

The data shown in Table 14 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

[2] Vref – DDR3/DDR3L external reference voltage

4.6.4 LVDS I/O DC parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

Table 28 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 28. LVDS I/O DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Differential Voltage	VOD	Rload-100 Ω Diff	250	350	450	mV
Output High Voltage	VOH	IOH = 0 mA	1.25	1.375	1.6	V
Output Low Voltage	VOL	IOL = 0 mA	0.9	1.025	1.25	V
Offset Voltage	VOS	—	1.125	1.2	1.375	V

4.7 I/O AC parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 4 and Figure 5.

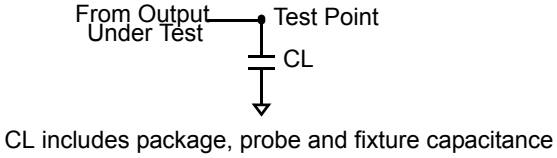


Figure 4. Load Circuit for Output

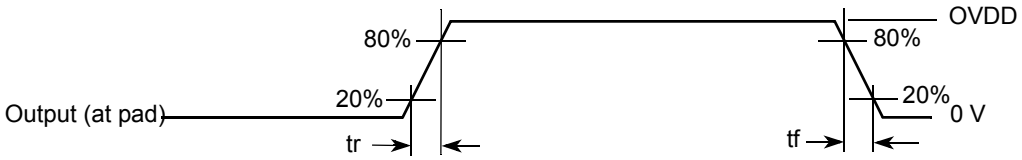
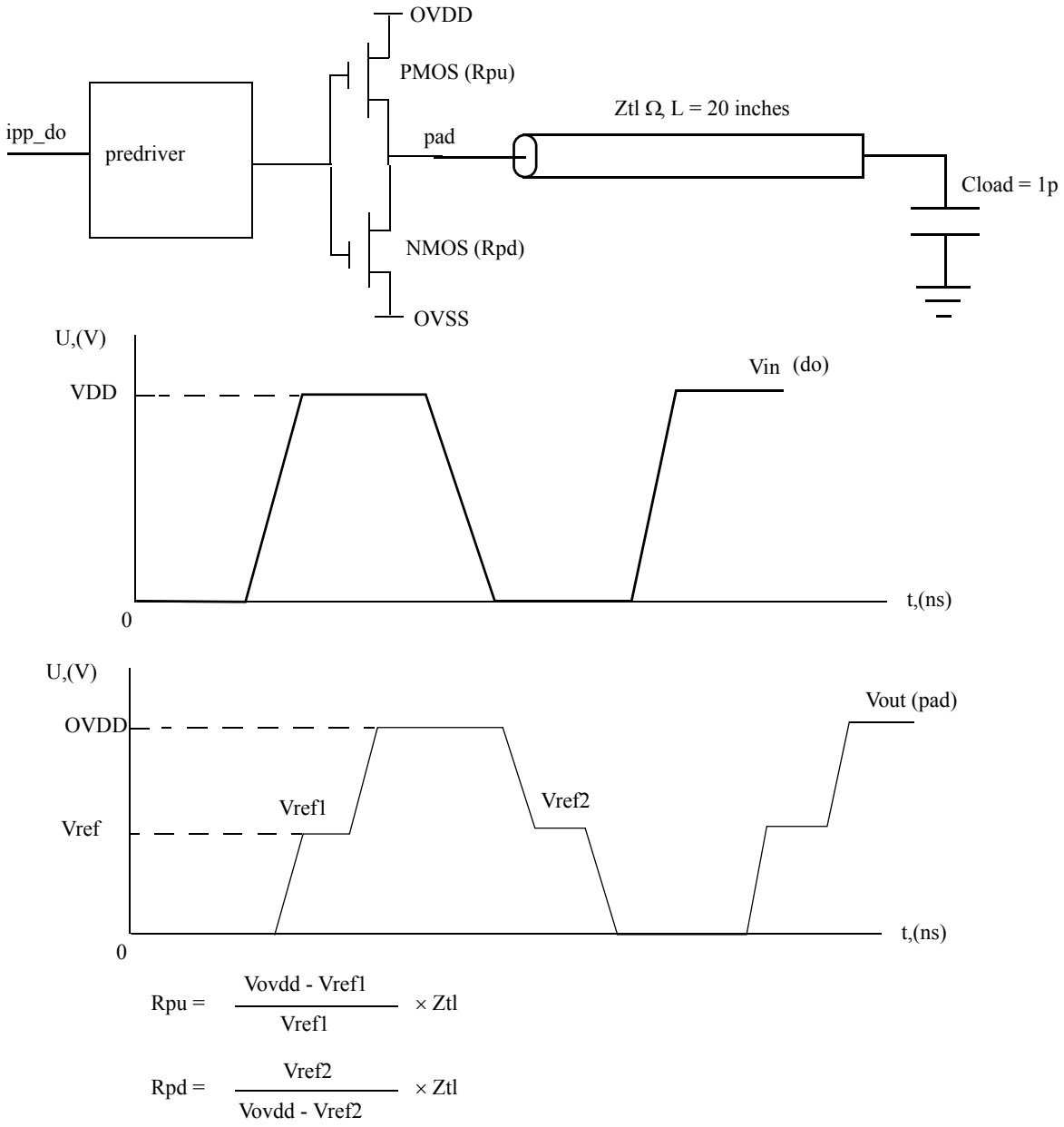


Figure 5. Output Transition Time Waveform

4.7.1 General Purpose I/O AC parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 29 and Table 30, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 6. Impedance Matching Load for Measurement

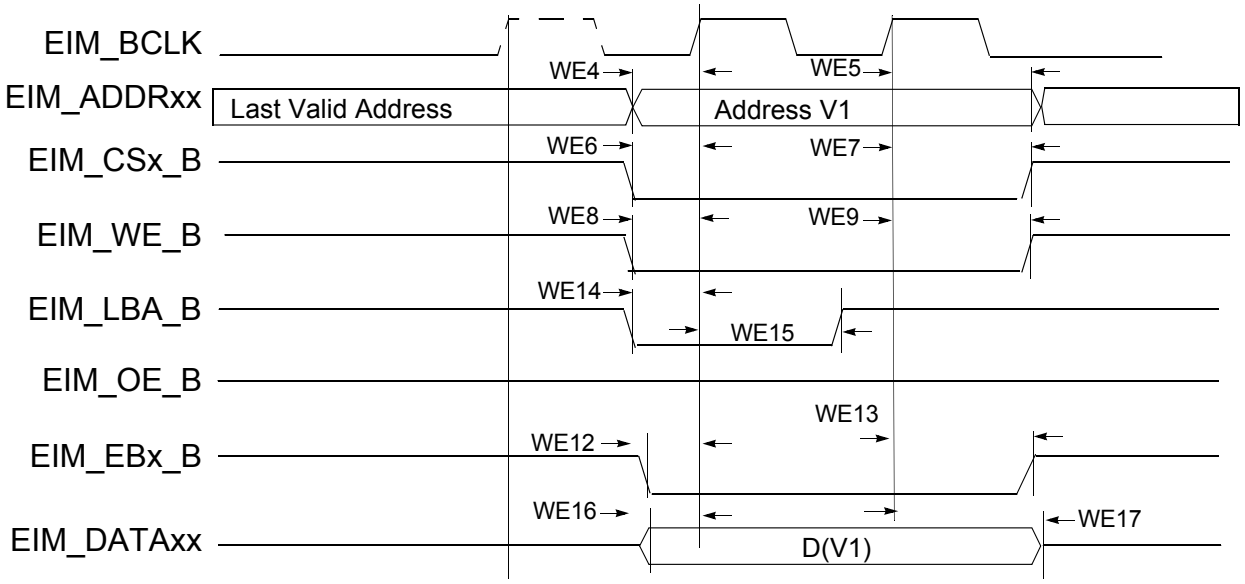


Figure 12. Synchronous Memory, Write Access, WSC=1, WBEA=0 and WADVN=0

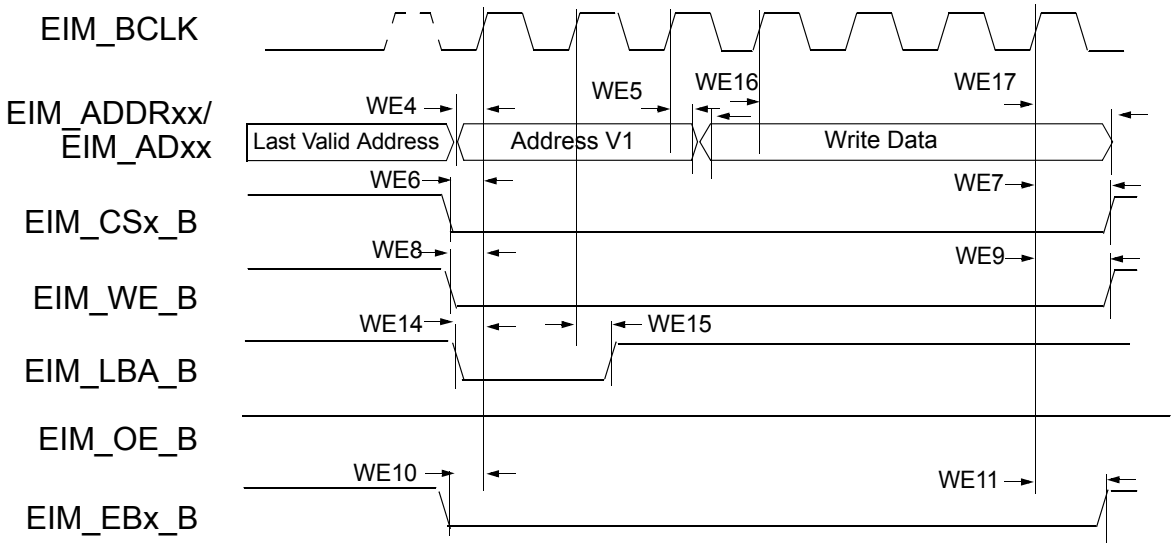


Figure 13. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6, ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

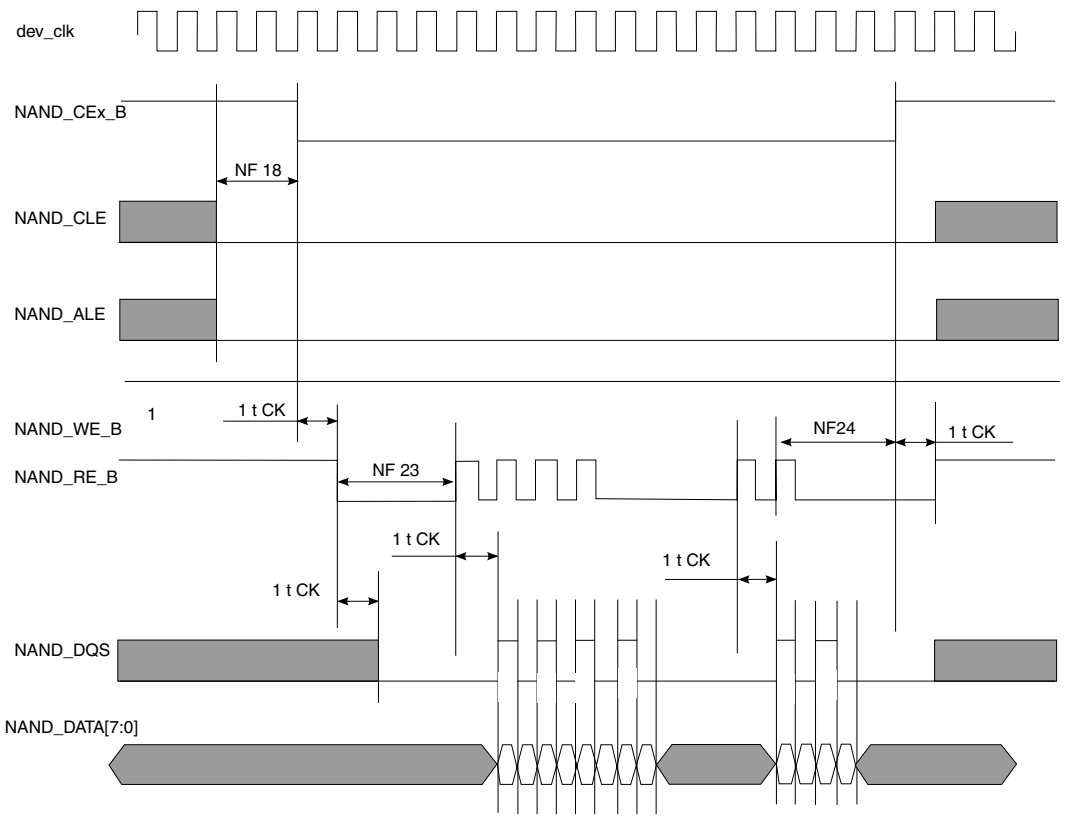


Figure 31. Samsung Toggle Mode Data Read Timing

Table 44. Samsung Toggle Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see 2,3]		—
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see 2]		—
NF3	NAND_CE0_B setup time	tCS	(AS + DS) × T - 0.58 [see 3,2]		—
NF4	NAND_CE0_B hold time	tCH	DH × T - 1 [see 2]		—
NF5	NAND_WE_B pulse width	tWP	DS × T [see 2]		—
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see 3,2]		—
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see 2]		—
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see 2]		—
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see 2]		—
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see 4,2]	—	ns
NF22	Clock period	tCK	—	—	ns
NF23	Preamble delay	tPRE	PRE_DELAY × T [see 5,2]	—	ns
NF24	Postamble delay	tPOST	POST_DELAY × T +0.43 [see 2]	—	ns

Figure 45 shows RMII mode timings. Table 57 describes the timing parameters (M16–M21) shown in the figure.

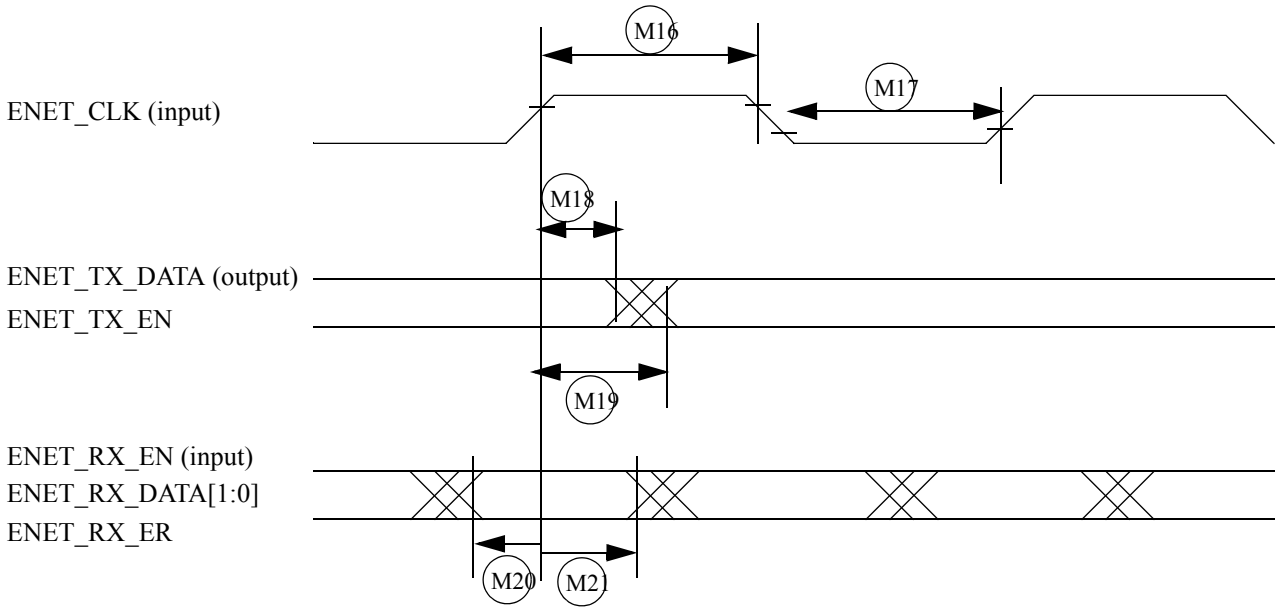


Figure 45. RMII Mode Signal Timing Diagram

Table 57. RMII Signal Timing

ID	Characteristic	Min.	Max.	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA valid	—	13	ns
M20	ENET_RX_DATAD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	2	—	ns
M21	ENET_CLK to ENET_RX_DATAD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

4.12.5 Flexible Controller Area Network (FLEXCAN) AC electrical specifications

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. The processor has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the *i.MX 6UltraLite Reference Manual* (IMX6ULRM) to see which pins expose Tx and Rx pins; these ports are named FLEXCAN_TX and FLEXCAN_RX, respectively.

4.12.7 Pulse Width Modulator (PWM) timing parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 47 depicts the timing of the PWM, and Table 59 lists the PWM timing parameters.

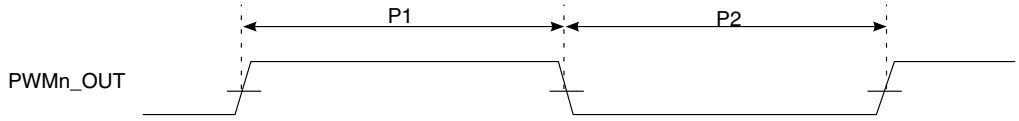


Figure 47. PWM Timing

Table 59. PWM Output Timing Parameters

ID	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	ipg_clk	MHz
P1	PWM output pulse width high	15	—	ns
P2	PWM output pulse width low	15	—	ns

4.12.8 LCD Controller (LCDIF) parameters

Figure 48 shows the LCDIF timing and Table 60 lists the timing parameters.

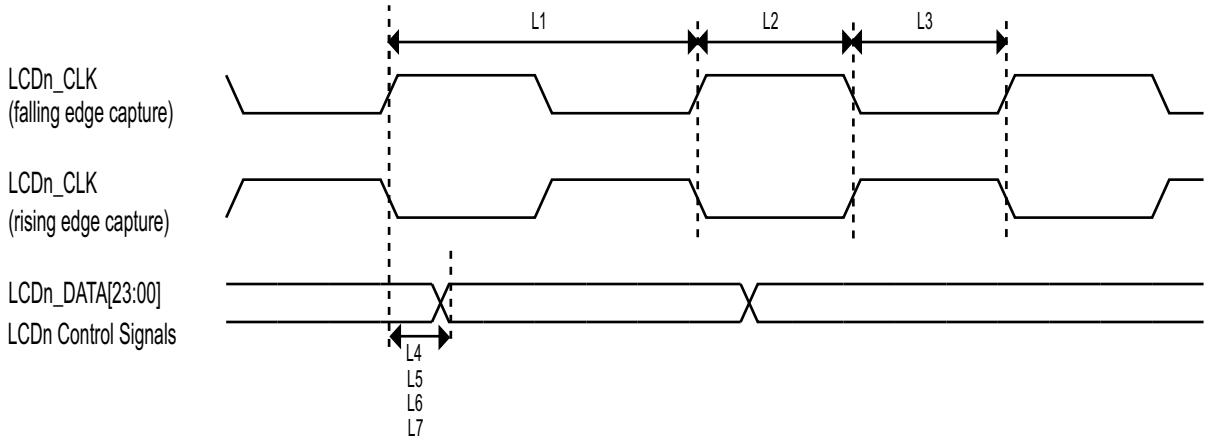


Figure 48. LCD Timing

Table 70. JTAG Timing (continued)

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns
SJ12	JTAG_TRST_B assert time	100	—	ns
SJ13	JTAG_TRST_B set-up time to JTAG_TCK low	40	—	ns

1 T_{DC} = target frequency of SJC
2 V_M = mid-point voltage

4.12.12 SPDIF timing parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 71 and Figure 61 and Figure 62 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 71. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT1 output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

Table 84. NAND Boot through GPMI (continued)

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG1[3:2]= 01b	BOOT_CFG1[3:2]= 10b
NAND_DATA00	rawnand.DATA00	Alt 0	Yes		
NAND_DATA01	rawnand.DATA01	Alt 0	Yes		
NAND_DATA02	rawnand.DATA02	Alt 0	Yes		
NAND_DATA03	rawnand.DATA03	Alt 0	Yes		
NAND_DATA04	rawnand.DATA04	Alt 0	Yes		
NAND_DATA05	rawnand.DATA05	Alt 0	Yes		
NAND_DATA06	rawnand.DATA06	Alt 0	Yes		
NAND_DATA07	rawnand.DATA07	Alt 0	Yes		
NAND_DQS	rawnand.DQS	Alt 0	Yes		
CSI_MCLK	rawnand.CE2_B	Alt 2			Yes
CSI_PIXCLK	rawnand.CE3_B	Alt 2			Yes

Table 85. SD/MMC Boot through USDHC1

Ball Name	Signal Name	Mux Mode	Common	4-bit	8-bit	BOOT_CFG1[1]=1 (SD Power Cycle)	SDMMC MFG mode
UART1_RTS_B	usdhc1.CD_B	Alt 2					Yes
SD1_CLK	usdhc1.CLK	Alt 0	Yes				
SD1_CMD	usdhc1.CMD	Alt 0	Yes				
SD1_DATA0	usdhc1.DATA0	Alt 0	Yes				
SD1_DATA1	usdhc1.DATA1	Alt 0		Yes	Yes		
SD1_DATA2	usdhc1.DATA2	Alt 0		Yes	Yes		
SD1_DATA3	usdhc1.DATA3	Alt 0	Yes				
NAND_READY_B	usdhc1.DATA4	Alt 1			Yes		
NAND_CE0_B	usdhc1.DATA5	Alt 1			Yes		
NAND_CE1_B	usdhc1.DATA6	Alt 1			Yes		
NAND_CLE	usdhc1.DATA7	Alt 1			Yes		
GPIO1_IO09	usdhc1.RESET_B	Alt 5				Yes	
GPIO1_IO05	usdhc1.VSELECT	Alt 4				Yes	

Table 88. Serial Download through UART1

Ball Name	Signal Name	Mux Mode	Common
UART1_TX_DATA	uart1.TX_DATA	Alt 0	Yes
UART1_RX_DATA	uart1.RX_DATA	Alt 0	Yes

Table 89. Serial Download through UART2

Ball Name	Signal Name	Mux Mode	Common
UART2_TX_DATA	uart2.TX_DATA	Alt 0	Yes
UART2_RX_DATA	uart2.RX_DATA	Alt 0	Yes

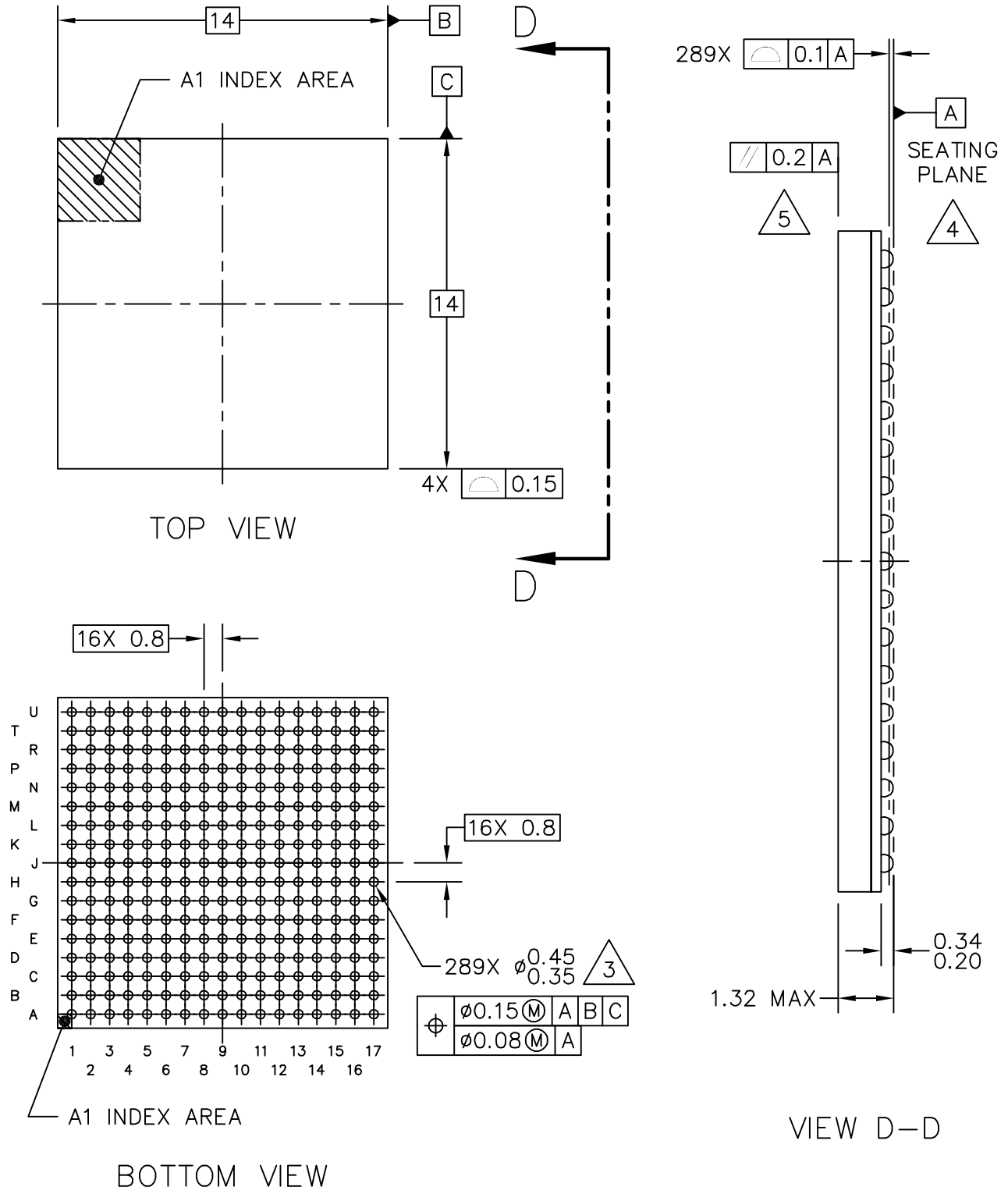


Figure 68. 14x14 mm BGA, Case x Package Top, Bottom, and Side Views

6.1.2 14x14 mm supplies contact assignments and functional contact assignments

Table 90 shows the device connection list for ground, sense, and reference contact signals.

Table 90. 14x14 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
ADC_VREFH	M13	—
DRAM_VREF	P4	—
GPANAIO	R13	—
NGND_KEL0	M12	—
NVCC_CSI	F4	—
NVCC_DRAM	G6, H6, J6, K6, L6, M6	—
NVCC_DRAM_2P5	N6	—
NVCC_ENET	F13	—
NVCC_GPIO	J13	—
NVCC_LCD	E13	—
NVCC_NAND	E7	—
NVCC_PLL	P13	—
NVCC_SD1	C4	—
NVCC_UART	H13	—
VDD_ARM_CAP	G9, G10, G11, H11	—
VDD_HIGH_CAP	R14, R15	—
VDD_HIGH_IN	N13	—
VDD_SNVS_CAP	N12	—
VDD_SNVS_IN	P12	—
VDD_SOC_CAP	G8, H8, J8, J11, K8, K11, L8, L9, L10, L11	—
VDD_SOC_IN	H9, H10, J9, J10, K9, K10	—
VDD_USB_CAP	R12	—
VDDA_ADC_3P3	L13	—
VSS	A1, A17, C3, C7, C11, C15, E8, E11, F6, F7, F8, F9, F10,F11, F12, G3, G5, G7, G12, G15, H7, H12, J5, J7, J12, K7, K12, L3, L7, L12, M7, M8, M9, M10, M11, N3, N5, R3, R5, R7, R11, R16, R17, T14, U1, U14, U17	—

Table 91 shows an alpha-sorted list of functional contact assignments for the 14x14 mm package.

Table 91. 14x14 mm Functional Contact Assignments

Ball Name	14x14 Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
BOOT_MODE0	T10	VDD_SNVS_IN	GPIO	ALT5	BOOT_MODE0	Input	100 kΩ pull-down
BOOT_MODE1	U10	VDD_SNVS_IN	GPIO	ALT5	BOOT_MODE1	Input	100 kΩ pull-down
CCM_CLK1_N	P16	VDD_HIGH_CAP	LVDS	—	CCM_CLK1_N	—	—
CCM_CLK1_P	P17	VDD_HIGH_CAP	LVDS	—	CCM_CLK1_P	—	—
CCM_PMIC_STBY_REQ	U9	VDD_SNVS_IN	GPIO	ALT0	CCM_PMIC_STBY_REQ	Output	—
CSI_DATA00	E4	NVCC_CSI	GPIO	ALT5	CSI_DATA00	Input	Keeper
CSI_DATA01	E3	NVCC_CSI	GPIO	ALT5	CSI_DATA01	Input	Keeper
CSI_DATA02	E2	NVCC_CSI	GPIO	ALT5	CSI_DATA02	Input	Keeper
CSI_DATA03	E1	NVCC_CSI	GPIO	ALT5	CSI_DATA03	Input	Keeper
CSI_DATA04	D4	NVCC_CSI	GPIO	ALT5	CSI_DATA04	Input	Keeper
CSI_DATA05	D3	NVCC_CSI	GPIO	ALT0	CSI_DATA05	Input	Keeper
CSI_DATA06	D2	NVCC_CSI	GPIO	ALT5	CSI_DATA06	Input	Keeper
CSI_DATA07	D1	NVCC_CSI	GPIO	ALT5	CSI_DATA07	Input	Keeper
CSI_HSYNC	F3	NVCC_CSI	GPIO	ALT5	CSI_HSYNC	Input	Keeper
CSI_MCLK	F5	NVCC_CSI	GPIO	ALT5	CSI_MCLK	Input	Keeper
CSI_PIXCLK	E5	NVCC_CSI	GPIO	ALT5	CSI_PIXCLK	Input	Keeper
CSI_VSYNC	F2	NVCC_CSI	GPIO	ALT5	CSI_VSYNC	Input	Keeper
DRAM_ADDR00	L5	NVCC_DRAM	DDR	ALT0	DRAM_ADDR00	Output	100 kΩ pull-up
DRAM_ADDR01	H2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR01	Output	100 kΩ pull-up
DRAM_ADDR02	K1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR02	Output	100 kΩ pull-up
DRAM_ADDR03	M2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR03	Output	100 kΩ pull-up
DRAM_ADDR04	K4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR04	Output	100 kΩ pull-up
DRAM_ADDR05	L1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR05	Output	100 kΩ pull-up
DRAM_ADDR06	G2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR06	Output	100 kΩ pull-up

Table 92. 14x14 mm, 0.8 mm Pitch, Ball Map (continued)

N	M	L	K	J	H	G
DRAM_ODT0	DRAM_SDBA0	DRAM_ADDR05	DRAM_ADDR02	DRAM_SDWE_B	DRAM_SDBA1	DRAM_ADDR14
DRAM_CS0_B	DRAM_ADDR03	DRAM_ADDR09	DRAM_SDBA2	DRAM_CAS_B	DRAM_ADDR01	DRAM_ADDR06
VSS	DRAM_SDCKE0	VSS	DRAM_ADDR11	DRAM_SDCKE1	DRAM_ADDR13	VSS
DRAM_ZQPAD	DRAM_ADDR10	DRAM_ADDR12	DRAM_ADDR04	DRAM_ADDR08	DRAM_ADDR07	DRAM_RESET
VSS	DRAM_RAS_B	DRAM_ADDR00	DRAM_ADDR15	VSS	DRAM_CS1_B	VSS
NVCC_DRAM_2P5	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM
TEST_MODE	VSS	VSS	VSS	VSS	VSS	VSS
SNVS_TAMPER5	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP
SNVS_TAMPER8	VSS	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_CAP
SNVS_TAMPER7	VSS	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_CAP
SNVS_TAMPER6	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_ARM_CAP	VDD_ARM_CAP
VDD_SNVS_CAP	NGND_KEL0	VSS	VSS	VSS	VSS	VSS
VDD_HIGH_IN	ADC_VREFH	VDDA_ADC_3P3	GPIO1_IO00	NVCC_GPIO	NVCC_UART	UART5_RX_DATA
JTAG_TRST_B	JTAG_TCK	GPIO1_IO02	UART1_TX_DATA	UART1_RTS_B	UART2_RTS_B	UART3_RTS_B
JTAG_TDO	GPIO1_IO09	GPIO1_IO01	UART1_CTS_B	UART2_CTS_B	UART3_CTS_B	VSS
JTAG_TDI	GPIO1_IO04	GPIO1_IO07	UART1_RX_DATA	UART2_RX_DATA	UART3_RX_DATA	UART4_RX_DATA
GPIO1_IO08	GPIO1_IO05	GPIO1_IO03	GPIO1_IO06	UART2_TX_DATA	UART3_TX_DATA	UART4_TX_DATA
N	M	L	K	J	H	G

Table 94 shows an alpha-sorted list of functional contact assignments for the 9x9 mm package.

Table 94. 9x9 mm Functional Contact Assignments

Ball Name	9x9 Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
BOOT_MODE0	T8	VDD_SNVS_IN	GPIO	ALT5	BOOT_MODE0	Input	100 kΩ pull-down
BOOT_MODE1	U8	VDD_SNVS_IN	GPIO	ALT5	BOOT_MODE1	Input	100 kΩ pull-down
CCM_CLK1_N	U16	VDD_HIGH_CAP	LVDS	—	CCM_CLK1_N	—	—
CCM_CLK1_P	T16	VDD_HIGH_CAP	LVDS	—	CCM_CLK1_P	—	—
CCM_PMIC_STBY_REQ	U7	VDD_SNVS_IN	GPIO	ALT0	CCM_PMIC_STBY_REQ	Output	—
CSI_DATA00	C3	NVCC_CSI	GPIO	ALT5	CSI_DATA00	Input	Keeper
CSI_DATA01	D4	NVCC_CSI	GPIO	ALT5	CSI_DATA01	Input	Keeper
CSI_DATA02	B2	NVCC_CSI	GPIO	ALT5	CSI_DATA02	Input	Keeper
CSI_DATA03	D1	NVCC_CSI	GPIO	ALT5	CSI_DATA03	Input	Keeper
CSI_DATA04	C4	NVCC_CSI	GPIO	ALT5	CSI_DATA04	Input	Keeper
CSI_DATA05	B3	NVCC_CSI	GPIO	ALT0	CSI_DATA05	Input	Keeper
CSI_DATA06	A3	NVCC_CSI	GPIO	ALT5	CSI_DATA06	Input	Keeper
CSI_DATA07	C2	NVCC_CSI	GPIO	ALT5	CSI_DATA07	Input	Keeper
CSI_HSYNC	D2	NVCC_CSI	GPIO	ALT5	CSI_HSYNC	Input	Keeper
CSI_MCLK	C1	NVCC_CSI	GPIO	ALT5	CSI_MCLK	Input	Keeper
CSI_PIXCLK	D5	NVCC_CSI	GPIO	ALT5	CSI_PIXCLK	Input	Keeper
CSI_VSYNC	D3	NVCC_CSI	GPIO	ALT5	CSI_VSYNC	Input	Keeper
DRAM_ADDR00	G1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR00	Output	100 kΩ pull-up
DRAM_ADDR01	G2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR01	Output	100 kΩ pull-up
DRAM_ADDR02	H1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR02	Output	100 kΩ pull-up
DRAM_ADDR03	J2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR03	Output	100 kΩ pull-up
DRAM_ADDR04	M4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR04	Output	100 kΩ pull-up
DRAM_ADDR05	H2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR05	Output	100 kΩ pull-up
DRAM_ADDR06	E4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR06	Output	100 kΩ pull-up

Table 94. 9x9 mm Functional Contact Assignments (continued)

JTAG_MOD	R13	NVCC_GPIO	GPIO	ALT5	JTAG_MOD	Input	100 kΩ pull-up
JTAG_TCK	R17	NVCC_GPIO	GPIO	ALT5	JTAG_TCK	Input	47 kΩ pull-up
JTAG_TDI	P17	NVCC_GPIO	GPIO	ALT5	JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	R16	NVCC_GPIO	GPIO	ALT5	JTAG_TDO	Output	Keeper
JTAG_TMS	R14	NVCC_GPIO	GPIO	ALT5	JTAG_TMS	Input	47 kΩ pull-up
JTAG_TRST_B	P13	NVCC_GPIO	GPIO	ALT5	JTAG_TRST_B	Input	47 kΩ pull-up
LCD_CLK	C11	NVCC_LCD	GPIO	ALT5	LCD_CLK	Input	Keeper
LCD_DATA00	D11	NVCC_LCD	GPIO	ALT5	LCD_DATA00	Input	Keeper
LCD_DATA01	B12	NVCC_LCD	GPIO	ALT5	LCD_DATA01	Input	Keeper
LCD_DATA02	D10	NVCC_LCD	GPIO	ALT5	LCD_DATA02	Input	Keeper
LCD_DATA03	B11	NVCC_LCD	GPIO	ALT5	LCD_DATA03	Input	Keeper
LCD_DATA04	A11	NVCC_LCD	GPIO	ALT5	LCD_DATA04	Input	Keeper
LCD_DATA05	D12	NVCC_LCD	GPIO	ALT5	LCD_DATA05	Input	Keeper
LCD_DATA06	D13	NVCC_LCD	GPIO	ALT5	LCD_DATA06	Input	Keeper
LCD_DATA07	C12	NVCC_LCD	GPIO	ALT5	LCD_DATA07	Input	Keeper
LCD_DATA08	B13	NVCC_LCD	GPIO	ALT5	LCD_DATA08	Input	Keeper
LCD_DATA09	A13	NVCC_LCD	GPIO	ALT5	LCD_DATA09	Input	Keeper
LCD_DATA10	D14	NVCC_LCD	GPIO	ALT5	LCD_DATA10	Input	Keeper
LCD_DATA11	C13	NVCC_LCD	GPIO	ALT5	LCD_DATA11	Input	Keeper
LCD_DATA12	C14	NVCC_LCD	GPIO	ALT5	LCD_DATA12	Input	Keeper
LCD_DATA13	A14	NVCC_LCD	GPIO	ALT5	LCD_DATA13	Input	Keeper
LCD_DATA14	B14	NVCC_LCD	GPIO	ALT5	LCD_DATA14	Input	Keeper
LCD_DATA15	A16	NVCC_LCD	GPIO	ALT5	LCD_DATA15	Input	Keeper
LCD_DATA16	A15	NVCC_LCD	GPIO	ALT5	LCD_DATA16	Input	Keeper
LCD_DATA17	D15	NVCC_LCD	GPIO	ALT5	LCD_DATA17	Input	Keeper
LCD_DATA18	B15	NVCC_LCD	GPIO	ALT5	LCD_DATA18	Input	Keeper
LCD_DATA19	E12	NVCC_LCD	GPIO	ALT5	LCD_DATA19	Input	Keeper
LCD_DATA20	B17	NVCC_LCD	GPIO	ALT5	LCD_DATA20	Input	Keeper
LCD_DATA21	C16	NVCC_LCD	GPIO	ALT5	LCD_DATA21	Input	Keeper
LCD_DATA22	B16	NVCC_LCD	GPIO	ALT5	LCD_DATA22	Input	Keeper
LCD_DATA23	C17	NVCC_LCD	GPIO	ALT5	LCD_DATA23	Input	Keeper

Table 96. GPIO Behaviors during Reset (continued)[1]

Ball Name	Mux Mode	Function	Input/Output	Value
LCD_DATA10	ALT6	SRC_BT_CFG[10]	Input	100 kΩ pull-down
LCD_DATA11	ALT6	SRC_BT_CFG[11]	Input	100 kΩ pull-down
LCD_DATA12	ALT6	SRC_BT_CFG[12]	Input	100 kΩ pull-down
LCD_DATA13	ALT6	SRC_BT_CFG[13]	Input	100 kΩ pull-down
LCD_DATA14	ALT6	SRC_BT_CFG[14]	Input	100 kΩ pull-down
LCD_DATA15	ALT6	SRC_BT_CFG[15]	Input	100 kΩ pull-down
LCD_DATA16	ALT6	SRC_BT_CFG[16]	Input	100 kΩ pull-down
LCD_DATA17	ALT6	SRC_BT_CFG[17]	Input	100 kΩ pull-down
LCD_DATA18	ALT6	SRC_BT_CFG[18]	Input	100 kΩ pull-down
LCD_DATA19	ALT6	SRC_BT_CFG[19]	Input	100 kΩ pull-down
LCD_DATA20	ALT6	SRC_BT_CFG[20]	Input	100 kΩ pull-down
LCD_DATA21	ALT6	SRC_BT_CFG[21]	Input	100 kΩ pull-down
LCD_DATA22	ALT6	SRC_BT_CFG[22]	Input	100 kΩ pull-down
LCD_DATA23	ALT6	SRC_BT_CFG[23]	Input	100 kΩ pull-down

1 Others are same as value in the column “Out of Reset Condition” of Table 91 and Table 94.