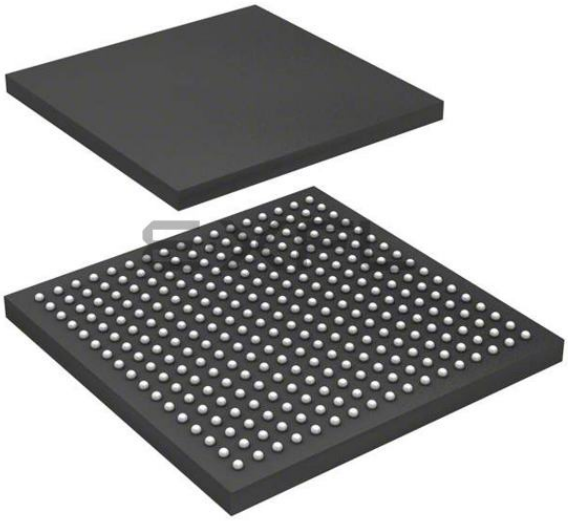

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	528MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	LCD, LVDS
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6g2cvm05aa

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC1 uSDHC2	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6UltraLite specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.5/4.2/4.3/4.4/4.41/ including high-capacity (size > 2 GB) cards HC MMC. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDXC cards up to 2 TB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v3.0 Two ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) • 4-bit or 8-bit transfer mode specifications for eMMC chips up to 200 MHz in HS200 mode (200 MB/s max)
USB	Universal Serial Bus 2.0	Connectivity Peripherals	USBO2 (USB OTG1 and USB OTG2) contains: • Two high-speed OTG 2.0 modules with integrated HS USB PHYs • Support eight Transmit (TX) and eight Receive (Rx) endpoints, including endpoint 0
WDOG1 WDOG3	Watch Dog	Timer Peripherals	The Watch Dog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG2 (TZ)	Watch Dog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW.

3.1 Special signal considerations

Table 4 lists special signal considerations for the i.MX 6UltraLite processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, "Package information and contact assignments"." Signal descriptions are provided in the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

Table 4. Special Signal Considerations

Signal Name	Remarks
CCM_CLK1_P/ CCM_CLK1_N	One general purpose differential high speed clock Input/output is provided. It can be used: • To feed external reference clock to the PLLs and further to the modules inside SoC. • To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals. See the *i.MX 6UltraLite Reference Manual* (IMX6ULRM) for details on the respective clock trees. Alternatively one may use single ended signal to drive CLK1_P input. In this case corresponding CLK1_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. After initialization, the CLK1 input/output can be disabled (if not used). If unused either or both of the CLK1_N/P pairs may remain unconnected.
RTC_XTALI/RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal, (≤100 kΩ ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI, the RTC_XTALO pin must remain unconnected or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be <100 kHz under typical conditions. In case when high accuracy real time clock are not required system may use internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and keep RTC_XTALO unconnected.
XTALI/XTALO	A 24.0 MHz crystal should be connected between XTALI and XTALO. The crystal must be rated for a maximum drive level of 250 μW. An ESR (equivalent series resistance) of typical 80 Ω is recommended. NXP BSP (board support package) software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALO must be directly driven by the external oscillator and XTALI mounted with 18 pF capacitor. Please refer to the EVK board reference design for details. The logic level of this forcing clock cannot exceed NVCC_PLL level. If this clock is used as a reference for USB, then there are strict frequency tolerance and jitter requirements. See OSC24M chapter and relevant interface specifications chapters for details.

4 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6UltraLite processors.

4.1 Chip-Level conditions

This section provides the device-level electrical characteristics for the IC. See Table 7 for a quick reference to the individual tables and sections.

Table 7. i.MX 6UltraLite Chip-Level Conditions

For these characteristics	Topic appears
Absolute maximum ratings	on page 20
Thermal resistance	on page 21
Operating ranges	on page 23
External clock sources	on page 24
Maximum supply currents	on page 25
Low power mode supply currents	on page 27
USB PHY current consumption	on page 28

4.1.1 Absolute maximum ratings

CAUTION

Stress beyond those listed under Table 8 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 8 shows the absolute maximum operating ratings.

Table 8. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core Supplies Input Voltage (LDO Enabled)	VDD_SOC_IN	-0.3	1.6	V
Core Supplies Input Voltage (LDO Bypass)	VDD_SOC_IN	-0.3	1.4	V
VDD_HIGH_IN Supply voltage	VDD_HIGH_IN	-0.3	3.6	V
Core Supplies Output Voltage (LDO Enabled)	VDD_ARM_CAP VDD_SOC_CAP	-0.3	1.4	V
VDD_HIGH_CAP LDO Output Supply Voltage	VDD_HIGH_CAP	-0.3	2.6	V

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can be used instead of the RTC_XTALI if accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

Table 13 shows the interface frequency requirements.

Table 13. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1,2]	f_{ckil}	—	32.768[3]/32.0	—	kHz
XTALI Oscillator[2,4]	f_{xtal}	—	24	—	MHz

[1] External oscillator or a crystal with internal oscillator amplifier.
[2] The required frequency stability of this clock source is application dependent. For recommendations, see the Hardware Development Guide for *i.MX 6UltraLite Applications Processors* (IMX6ULHDG).
[3] Recommended nominal frequency 32.768 kHz.
[4] External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 13 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available.

- On-chip 40 kHz ring oscillator—this clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit:
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision time-out.

4.1.5 Maximum supply currents

The data shown in Table 14 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

See the i.MX 6UltraLite Power Consumption Measurement Application Note (AN5170) for more details on typical power consumption under various use case definitions.

Table 14. Maximum Supply Currents

Power Line	Conditions	Max Current	Unit
VDD_SOC_IN	528 MHz ARM clock based on Dhrystone test	500	mA
VDD_HIGH_IN	—	125[1]	mA
VDD_SNVS_IN	—	500[2]	μA
USB_OTG1_VBUS USB_OTG2_VBUS	—	50[3]	mA
VDDA_ADC_3P3	100 Ohm maximum loading for touch panel	35	mA
Primary Interface (IO) Supplies			
NVCC_DRAM	—	(See[4])	—
NVCC_DRAM_2P5	—	50	mA
NVCC_GPIO	N=16	Use maximum IO Equation[5]	—
NVCC_UART	N=16	Use maximum IO equation[5]	—
NVCC_ENET	N=16	Use maximum IO equation[5]	—
NVCC_LCD	N=29	Use maximum IO equation[5]	—
NVCC_NAND	N=17	Use maximum IO equation[5]	—
NVCC_SD1	N=6	Use maximum IO equation[5]	—
NVCC_CSI	N=12	Use maximum IO equation[5]	—
MISC			
DRAM_VREF	—	1	mA

[1] The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_DRAM_2P5 supplies).

[2] The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA, if available. VDD_SNVS_CAP charge time will increase if less than 1 mA is available.

[3] This is the maximum current per active USB physical interface.

[4] The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination. See the *i.MX 6UltraLite Power Consumption Measurement Application Note* (AN5170) or examples of DRAM power consumption during specific use case scenarios.

[5] General equation for estimated, maximum power consumption of an IO power supply:
Imax = N x C x V x (0.5 x F)
Where:
N—Number of IO pins supplied by the power line
C—Equivalent external capacitive load
V—IO voltage
(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)
In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

Table 25. LPDDR2 I/O DC Electrical Parameters[1] (continued)

Parameters	Symbol	Test Conditions	Min	Max	Unit
DC High-Level input voltage	Vih_DC	—	Vref+0.13	OVDD	V
DC Low-Level input voltage	Vil_DC	—	OVSS	Vref-0.13	V
Differential Input Logic High	Vih_diff	—	0.26	Note[2]	—
Differential Input Logic Low	Vil_diff	—	Note[2]	-0.26	—
Pull-up/Pull-down Impedance Mismatch	Mmpupd	—	-15	15	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper Circuit Resistance	Rkeep	—	110	175	kΩ
Input current (no pull-up/down)	Iin	VI = 0, VI = OVDD	-2.5	2.5	μA

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4.6.3.2 DDR3/DDR3L mode I/O DC parameters

The parameters in Table 27 are guaranteed per the operating ranges in Table 11, unless otherwise noted.

Table 27. DDR3/DDR3L I/O DC Electrical Characteristics

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -0.1mA Voh (for ipp_dse=001)	0.8*OVDD[1]	—	V
Low-level output voltage	VOL	Iol= 0.1mA Vol (for ipp_dse=001)	0.2*OVDD	—	V
High-level output voltage	VOH	Ioh= -1mA Voh (for all except ipp_dse=001)	0.8*OVDD	—	V
Low-level output voltage	VOL	Iol= 1mA Vol (for all except ipp_dse=001)	0.2*OVDD	—	V
Input Reference Voltage	Vref	—	0.49*ovdd	0.51*ovdd	V
DC High-Level input voltage	Vih_DC	—	Vref[2]+0.1	OVDD	V
DC Low-Level input voltage	Vil_DC	—	OVSS	Vref-0.1	V
Differential Input Logic High	Vih_diff	—	0.2	—	V
Differential Input Logic Low	Vil_diff	—	—	-0.2	V
Termination Voltage	Vtt	Vtt tracking OVDD/2	0.49*OVDD	0.51*OVDD	V
Pull-up/Pull-down Impedance Mismatch	Mmpupd	—	-10	10	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper Circuit Resistance	Rkeep	—	105	165	kΩ
Input current (no pull-up/down)	Iin	VI = 0,VI = OVDD	-2.9	2.9	μA

1 OVDD – I/O power supply (1.425 V–1.575 V for DDR3 and 1.283 V–1.45 V for DDR3L)

[2] Vref – DDR3/DDR3L external reference voltage

4.6.4 LVDS I/O DC parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits" for details.

Table 28 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 28. LVDS I/O DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Differential Voltage	VOD	Rload-100 Ω Diff	250	350	450	mV
Output High Voltage	VOH	IOH = 0 mA	1.25	1.375	1.6	V
Output Low Voltage	VOL	IOL = 0 mA	0.9	1.025	1.25	V
Offset Voltage	VOS	—	1.125	1.2	1.375	V

4.7 I/O AC parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 4 and Figure 5.

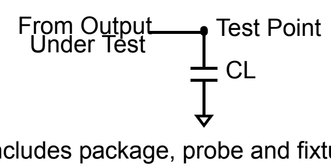

Figure 4. Load Circuit for Output

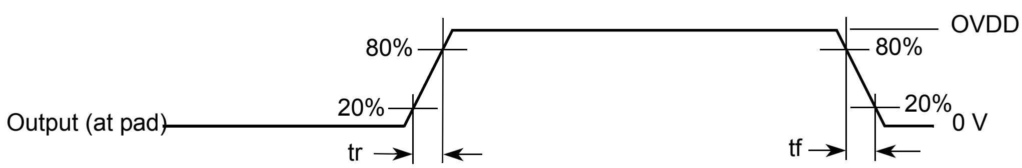

Figure 5. Output Transition Time Waveform

4.7.1 General Purpose I/O AC parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 29 and Table 30, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 31. DDR I/O LPDDR2 Mode AC Parameters[1] (continued)

Parameter	Symbol	Test Condition	Min	Max	Unit
AC differential input low voltage	Vidl(ac)	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	-0.12	0.12	V
Over/undershoot peak	Vpeak	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	0.3	V-ns
Single output slew rate, measured between Vol (ac) and Voh (ac)	tsr	50 Ω to Vref. 5 pF load. Drive impedance = 40 Ω ± 30%	1.5	3.5	V/ns
		50 Ω to Vref. 5pF load.Drive impedance = 60 Ω ± 30%	1	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	0.1	ns

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage | Vtr - Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 32 shows the AC parameters for DDR I/O operating in DDR3/DDR3L mode.

Table 32. DDR I/O DDR3/DDR3L Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref - 0.175	V
AC differential input voltage[2]	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	Vref - 0.15	—	Vref + 0.15	V
Over/undershoot peak	Vpeak	—	—	—	0.4	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.5	V-ns
Single output slew rate, measured between Vol (ac) and Voh (ac)	tsr	Driver impedance = 34 Ω	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC JESD79_3D specification supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage | Vtr-Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.9 System modules timing

This section contains the timing and electrical parameters for the modules in each i.MX 6UltraLite processor.

4.9.1 Reset timings parameters

Figure 7 shows the reset timing and Table 36 lists the timing parameters.

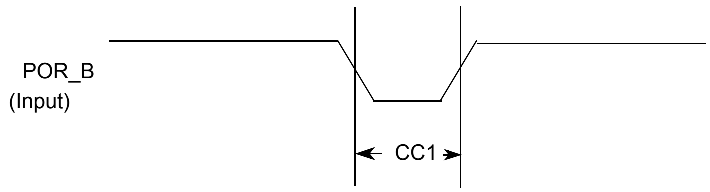

Figure 7. Reset Timing Diagram

Table 36. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid.	1	—	RTC_XTALI cycle

4.9.2 WDOG reset timing parameters

Figure 8 shows the WDOG reset timing and Table 37 lists the timing parameters.

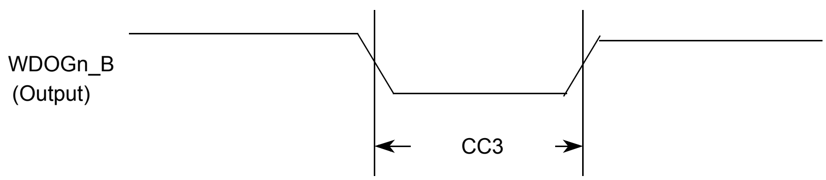

Figure 8. WDOGn_B Timing Diagram

Table 37. WDOGn_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOGn_B Assertion	1	—	RTC_XTALI cycle

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 μs.

NOTE

WDOG1_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

Table 42. Asynchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see [2,3]]		ns
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see [2]]		ns
NF3	NAND_CE0_B setup time	tCS	(AS + DS + 1) × T [see [3,2]]		ns
NF4	NAND_CE0_B hold time	tCH	(DH+1) × T - 1 [see [2]]		ns
NF5	NAND_WE_B pulse width	tWP	DS × T [see [2]]		ns
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see [3,2]]		ns
NF7	NAND_ALE hold time	tALH	(DH × T - 0.42 [see [2]]		ns
NF8	Data setup time	tDS	DS × T - 0.26 [see [2]]		ns
NF9	Data hold time	tDH	DH × T - 1.37 [see [2]]		ns
NF10	Write cycle time	tWC	(DS + DH) × T [see [2]]		ns
NF11	NAND_WE_B hold time	tWH	DH × T [see [2]]		ns
NF12	Ready to NAND_RE_B low	tRR[4]	(AS + 2) × T [see [3,2]]	—	ns
NF13	NAND_RE_B pulse width	tRP	DS × T [see [2]]		ns
NF14	READ cycle time	tRC	(DS + DH) × T [see [2]]		ns
NF15	NAND_RE_B high hold time	tREH	DH × T [see [2]]		ns
NF16	Data setup on read	tDSR	—	(DS × T -0.67)/18.38 [see [5,6]]	ns
NF17	Data hold on read	tDHR	0.82/11.83 [see [5,6]]	—	ns

1 GPMI's Async Mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = GPMI clock period -0.075ns (half of maximum p-p jitter).

4 NF12 is guaranteed by the design.

5 Non-EDO mode.

6 EDO mode, GPMI clock ≈ 100 MHz (AS=DS=DH=1, GPMI_CTL1 [RDN_DELAY] = 8, GPMI_CTL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 24), NF16/NF17 is different from the definition in non-EDO mode (Figure 23). They are called tREA/tRHOH (RE# access time/RE# HIGH to output hold). The typical values for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample NAND_DATAxx at rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the *i.MX 6UltraLite Reference Manual*). The typical value of this control register is 0x8 at 50 MT/s EDO mode. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

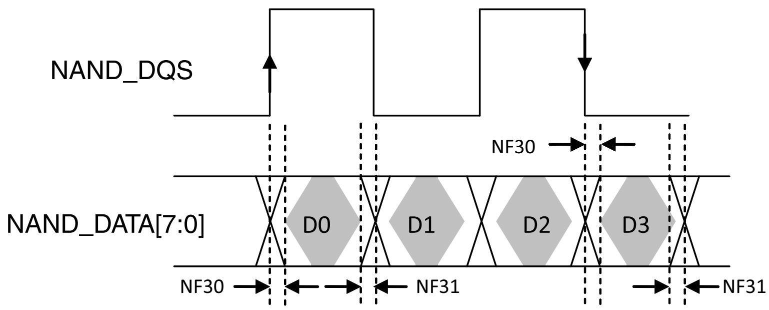

Figure 29. NAND_DQS/NAND_DQ Read Valid Window

Table 43. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	NAND_CE0_B access time	tCE	CE_DELAY × T - 0.79 [see [2]]		ns
NF19	NAND_CE0_B hold time	tCH	0.5 × tCK - 0.63 [see [2]]		ns
NF20	Command/address NAND_DATAxx setup time	tCAS	0.5 × tCK - 0.05		ns
NF21	Command/address NAND_DATAxx hold time	tCAH	0.5 × tCK - 1.23		ns
NF22	Clock period	tCK	—		ns
NF23	Preamble delay	tPRE	PRE_DELAY × T - 0.29 [see [2]]		ns
NF24	Postamble delay	tPOST	POST_DELAY × T - 0.78 [see [2]]		ns
NF25	NAND_CLE and NAND_ALE setup time	tCALS	0.5 × tCK - 0.86		ns
NF26	NAND_CLE and NAND_ALE hold time	tCALH	0.5 × tCK - 0.37		ns
NF27	NAND_CLK to first NAND_DQS latching transition	tDQSS	T - 0.41 [see [2]]		ns
NF28	Data write setup	—	0.25 × tCK - 0.35		—
NF29	Data write hold	—	0.25 × tCK - 0.85		—
NF30	NAND_DQS/NAND_DQ read setup skew	—	—	2.06	—
NF31	NAND_DQS/NAND_DQ read hold skew	—	—	1.95	—

[1] GPMI's source synchronous mode output timing can be controlled by the module's internal registers GPMI_TIMING2_CE_DELAY, GPMI_TIMING_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers settings. In the table, CE_DELAY/PRE_DELAY/POST_DELAY represents each of these settings.

[2] T = tCK(GPMI clock period) -0.075ns (half of maximum p-p jitter).

For DDR Source sync mode, Figure 29 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 0.85ns (max) and 1ns (max) for tQHS at 200MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of a delayed NAND_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the *i.MX 6UltraLite Reference Manual*). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

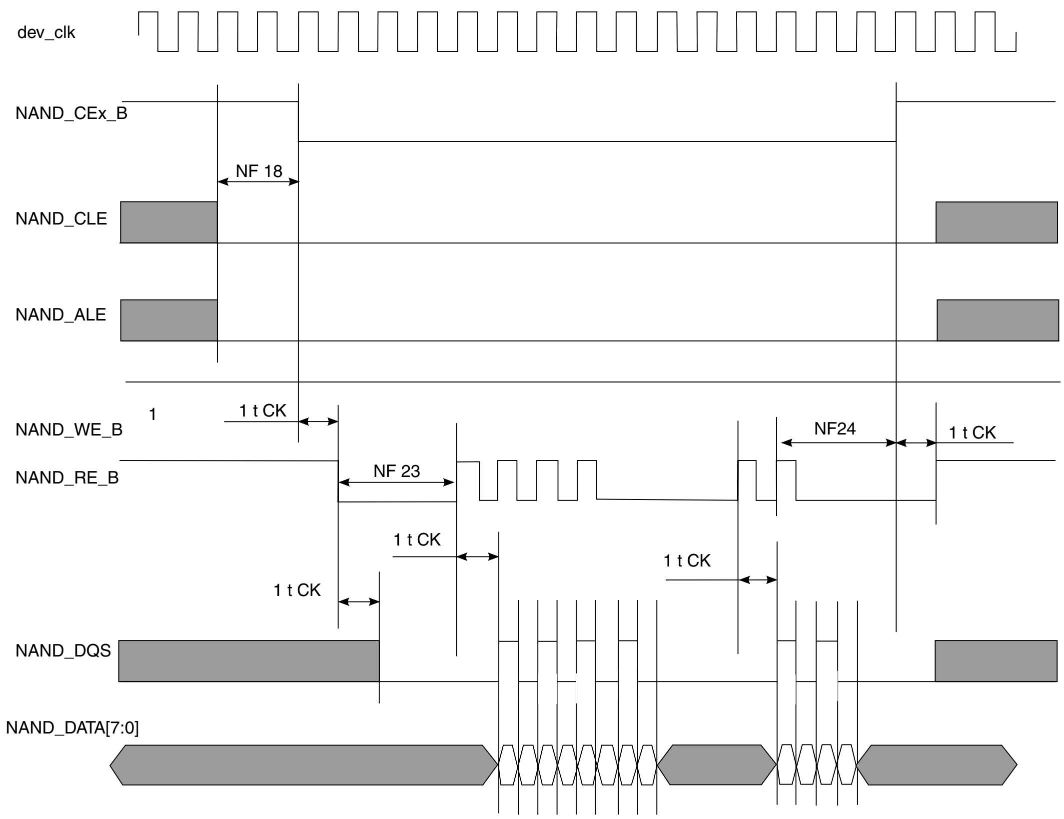

Figure 31. Samsung Toggle Mode Data Read Timing

Table 44. Samsung Toggle Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see [2,3]]		—
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see [2]]		—
NF3	NAND_CE0_B setup time	tCS	(AS + DS) × T - 0.58 [see [3,2]]		—
NF4	NAND_CE0_B hold time	tCH	DH × T - 1 [see [2]]		—
NF5	NAND_WE_B pulse width	tWP	DS × T [see [2]]		—
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see [3,2]]		—
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see [2]]		—
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see [2]]		—
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see [2]]		—
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see [4,2]]	—	ns
NF22	Clock period	tCK	—	—	ns
NF23	Preamble delay	tPRE	PRE_DELAY × T [see [5,2]]	—	ns
NF24	Postamble delay	tPOST	POST_DELAY × T +0.43 [see [2]]	—	ns

Table 49. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

[1] In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

[2] In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0─25 MHz. In high-speed mode, clock frequency can be any value between 0─50 MHz.

[3] In normal (full) speed mode for MMC card, clock frequency can be any value between 0─20 MHz. In high-speed mode, clock frequency can be any value between 0─52 MHz.

[4] To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.12.3.2 eMMC4.4/4.41 (dual data rate) AC timing

Figure 38 depicts the timing of eMMC4.4/4.41. Table 50 lists the eMMC4.4/4.41 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

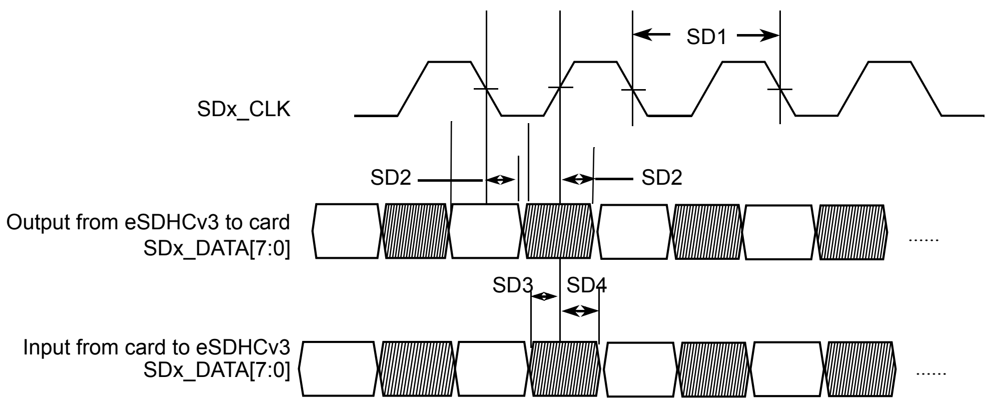

Figure 38. eMMC4.4/4.41 Timing

Table 50. eMMC4.4/4.41 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC4.4/4.41 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.5	7.1	ns
uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	1.7	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

4.12.3.4 HS200 mode timing

Figure 40 depicts the timing of HS200 mode, and Table 52 lists the HS200 timing characteristics.

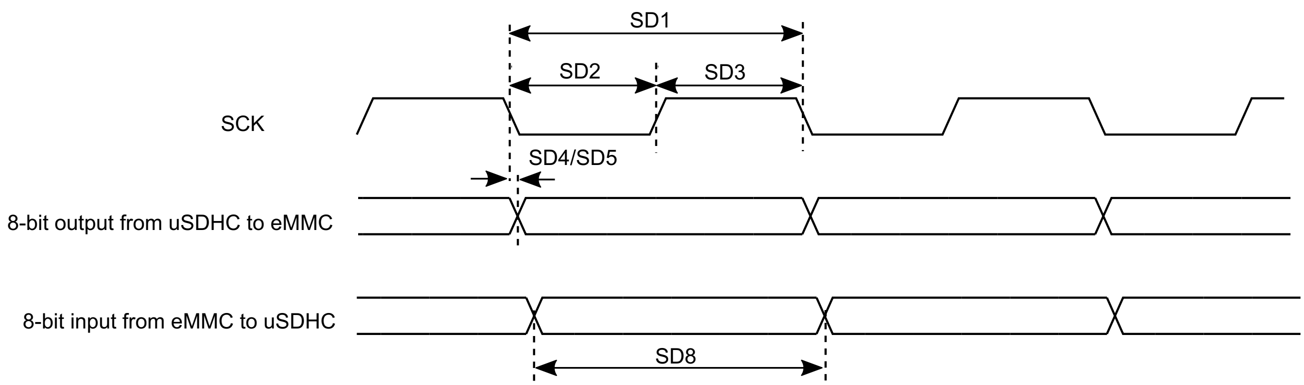

Figure 40. HS200 Mode Timing

Table 52. HS200 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

[1]HS200 is for 8 bits while SDR104 is for 4 bits.

4.12.3.5 Bus operation condition for 3.3 V and 1.8 V signaling

Signaling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1 supply are identical to those shown in Table 24, "Single Voltage GPIO DC Parameters," on page 34.

4.12.4 Ethernet Controller (ENET) AC electrical specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 61. LCD Signal Parameters (continued)

LCD_D12 / ENABLE**	—	R[1]	R[0]	G[4]	—
LCD_D11	—	R[0]	G[5]	G[3]	—
LCD_D10	—	G[5]	G[4]	G[2]	—
LCD_D9	—	G[4]	G[3]	G[1]	—
LCD_D8	—	G[3]	G[2]	G[0]	—
LCD_D8	—	G[3]	G[2]	G[0]	—
LCD_D7	R[2]	G[2]	G[1]	B[7]	Y/C[7]
LCD_D6	R[1]	G[1]	G[0]	B[6]	Y/C[6]
LCD_D5	R[0]	G[0]	B[5]	B[5]	Y/C[5]
LCD_D4	G[2]	B[4]	B[4]	B[4]	Y/C[4]
LCD_D3	G[1]	B[3]	B[3]	B[3]	Y/C[3]
LCD_D2	G[0]	B[2]	B[2]	B[2]	Y/C[2]
LCD_D1	B[1]	B[1]	B[1]	B[1]	Y/C[1]
LCD_D0	B[0]	B[0]	B[0]	B[0]	Y/C[0]
LCD_RESET	LCD_RESET	LCD_RESET	LCD_RESET	LCD_RESET	—
LCD_BUSY / LCD_VSYNC	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	—

4.12.9 QUAD SPI (QSPI) timing parameters

Measurement conditions are with 35 pF load on SCK and SIO pins and input slew rate of 1 V/ns.

4.12.9.1 SDR mode

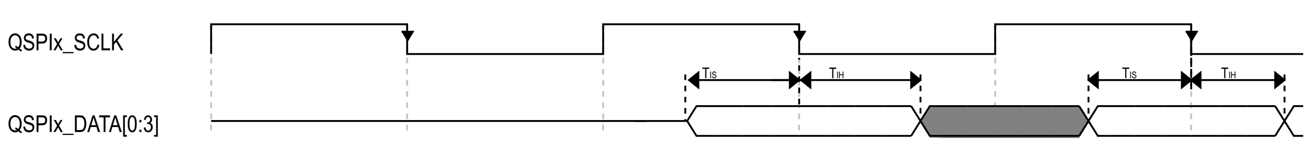

Figure 49. QuadSPI Input/Read Timing (SDR mode with internal sampling)

- Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010
  - Portable device only

4.13 A/D converter

4.13.1 12-bit ADC electrical characteristics

4.13.1.1 12-bit ADC operating conditions

Table 76. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDAD}	3.0	-	3.6	V	—
	Delta to VDD (VDD-VDDAD)[2]	ΔVDDAD	-100	0	100	mV	—
Ground voltage	Delta to VSS (VSS-VSSAD)	ΔVSSAD	-100	0	100	mV	—
Ref Voltage High	—	V_{REFH}	1.13	V_{DDAD}	V_{DDAD}	V	—
Ref Voltage Low	—	V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	—
Input Voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
Input Capacitance	8/10/12 bit modes	C_{ADIN}	—	1.5	2	pF	—
Input Resistance	ADLPC=0, ADHSC=1	R_{ADIN}	—	5	7	kohms	—
	ADLPC=0, ADHSC=0		—	12.5	15	kohms	—
	ADLPC=1, ADHSC=0		—	25	30	kohms	—
Analog Source Resistance	12 bit mode f_{ADCK} = 40MHz ADLSMP=0, ADSTS=10, ADHSC=1	R_{AS}	—	—	1	kohms	T_{samp}=150 ns
R_{AS} depends on Sample Time Setting (ADLSMP, ADSTS) and ADC Power Mode (ADHSC, ADLPC). See charts for Minimum Sample Time vs R_{AS}							
ADC Conversion Clock Frequency	ADLPC=0, ADHSC=1 12 bit mode	f_{ADCK}	4	—	40	MHz	—
	ADLPC=0, ADHSC=0 12 bit mode		4	—	30	MHz	—
	ADLPC=1, ADHSC=0 12 bit mode		4	—	20	MHz	—

[1] Typical values assume VDDAD = 3.0 V, Temp = 25°C, f_{ADCK}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

Table 81. SPI Boot through ECSPI2 (continued)

LCD_VSYNC	ecspi2.SS2	Alt 8				Yes	
LCD_RESET	ecspi2.SS3	Alt 8					Yes

Table 82. SPI Boot through ECSPI3

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG4 [5:4]=00b	BOOT_CFG4[5:4]=01b	BOOT_CFG4[5:4]=10b	BOOT_CFG4 [5:4]=11b
UART2_RTS_B	ecspi3.MISO	Alt 8	Yes				
UART2_CTS_B	ecspi3.MOSI	Alt 8	Yes				
UART2_RX_DATA	ecspi3.SCLK	Alt 8	Yes				
UART2_TX_DATA	ecspi3.SS0	Alt 8		Yes			
NAND_ALE	ecspi3.SS1	Alt 8			Yes		
NAND_RE_B	ecspi3.SS2	Alt 8				Yes	
NAND_WE_B	ecspi3.SS3	Alt 8					Yes

Table 83. SPI Boot through ECSPI4

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG4 [5:4]=00b	BOOT_CFG4 [5:4]=01b	BOOT_CFG4[5:4]=10b	BOOT_CFG 4[5:4]=11b
ENET2_TX_CLK	ecspi4.MISO	Alt 3	Yes				
ENET2_TX_EN	ecspi4.MOSI	Alt 3	Yes				
ENET2_TX_DATA1	ecspi4.SCLK	Alt 3	Yes				
ENET2_RX_ER	ecspi4.SS0	Alt 3		Yes			
NAND_DATA01	ecspi4.SS1	Alt 8			Yes		
NAND_DATA02	ecspi4.SS2	Alt 8				Yes	
NAND_DATA03	ecspi4.SS3	Alt 8					Yes

Table 84. NAND Boot through GPMI

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG1[3:2]= 01b	BOOT_CFG1[3:2]= 10b
NAND_CLE	rawnand.CLE	Alt 0	Yes		
NAND_ALE	rawnand.ALE	Alt 0	Yes		
NAND_WP_B	rawnand.WP_B	Alt 0	Yes		
NAND_READY_B	rawnand.READY_B	Alt 0	Yes		
NAND_CE0_B	rawnand.CE0_B	Alt 0	Yes		
NAND_CE1_B	rawnand.CE1_B	Alt 0		Yes	Yes
NAND_RE_B	rawnand.RE_B	Alt 0	Yes		
NAND_WE_B	rawnand.WE_B	Alt 0	Yes		

Table 91. 14x14 mm Functional Contact Assignments (continued)

JTAG_MOD	P15	NVCC_GPIO	GPIO	ALT5	JTAG_MOD	Input	100 kΩ pull-up
JTAG_TCK	M14	NVCC_GPIO	GPIO	ALT5	JTAG_TCK	Input	47 kΩ pull-up
JTAG_TDI	N16	NVCC_GPIO	GPIO	ALT5	JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	N15	NVCC_GPIO	GPIO	ALT5	JTAG_TDO	Output	Keeper
JTAG_TMS	P14	NVCC_GPIO	GPIO	ALT5	JTAG_TMS	Input	47 kΩ pull-up
JTAG_TRST_B	N14	NVCC_GPIO	GPIO	ALT5	JTAG_TRST_B	Input	47 kΩ pull-up
LCD_CLK	A8	NVCC_LCD	GPIO	ALT5	LCD_CLK	Input	Keeper
LCD_DATA00	B9	NVCC_LCD	GPIO	ALT5	LCD_DATA00	Input	Keeper
LCD_DATA01	A9	NVCC_LCD	GPIO	ALT5	LCD_DATA01	Input	Keeper
LCD_DATA02	E10	NVCC_LCD	GPIO	ALT5	LCD_DATA02	Input	Keeper
LCD_DATA03	D10	NVCC_LCD	GPIO	ALT5	LCD_DATA03	Input	Keeper
LCD_DATA04	C10	NVCC_LCD	GPIO	ALT5	LCD_DATA04	Input	Keeper
LCD_DATA05	B10	NVCC_LCD	GPIO	ALT5	LCD_DATA05	Input	Keeper
LCD_DATA06	A10	NVCC_LCD	GPIO	ALT5	LCD_DATA06	Input	Keeper
LCD_DATA07	D11	NVCC_LCD	GPIO	ALT5	LCD_DATA07	Input	Keeper
LCD_DATA08	B11	NVCC_LCD	GPIO	ALT5	LCD_DATA08	Input	Keeper
LCD_DATA09	A11	NVCC_LCD	GPIO	ALT5	LCD_DATA09	Input	Keeper
LCD_DATA10	E12	NVCC_LCD	GPIO	ALT5	LCD_DATA10	Input	Keeper
LCD_DATA11	D12	NVCC_LCD	GPIO	ALT5	LCD_DATA11	Input	Keeper
LCD_DATA12	C12	NVCC_LCD	GPIO	ALT5	LCD_DATA12	Input	Keeper
LCD_DATA13	B12	NVCC_LCD	GPIO	ALT5	LCD_DATA13	Input	Keeper
LCD_DATA14	A12	NVCC_LCD	GPIO	ALT5	LCD_DATA14	Input	Keeper
LCD_DATA15	D13	NVCC_LCD	GPIO	ALT5	LCD_DATA15	Input	Keeper
LCD_DATA16	C13	NVCC_LCD	GPIO	ALT5	LCD_DATA16	Input	Keeper
LCD_DATA17	B13	NVCC_LCD	GPIO	ALT5	LCD_DATA17	Input	Keeper
LCD_DATA18	A13	NVCC_LCD	GPIO	ALT5	LCD_DATA18	Input	Keeper
LCD_DATA19	D14	NVCC_LCD	GPIO	ALT5	LCD_DATA19	Input	Keeper
LCD_DATA20	C14	NVCC_LCD	GPIO	ALT5	LCD_DATA20	Input	Keeper
LCD_DATA21	B14	NVCC_LCD	GPIO	ALT5	LCD_DATA21	Input	Keeper
LCD_DATA22	A14	NVCC_LCD	GPIO	ALT5	LCD_DATA22	Input	Keeper
LCD_DATA23	B16	NVCC_LCD	GPIO	ALT5	LCD_DATA23	Input	Keeper

Table 94. 9x9 mm Functional Contact Assignments (continued)

DRAM_SDQS0_P	P5	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_P	Input	100 kΩ pull-down
DRAM_SDQS1_N	N4	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_P	Input	100 kΩ pull-down
DRAM_SDQS1_P	N3	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_N	Input	100 kΩ pull-down
DRAM_SDWE_B	F4	NVCC_DRAM	DDR	ALT0	DRAM_SDWE_B	Output	100 kΩ pull-up
DRAM_ZQPAD	T2	NVCC_DRAM	GPIO	—	DRAM_ZQPAD	Input	Keeper
ENET1_RX_DATA0	G17	NVCC_ENET	GPIO	ALT5	ENET1_RX_DATA0	Input	Keeper
ENET1_RX_DATA1	F16	NVCC_ENET	GPIO	ALT5	ENET1_RX_DATA1	Input	Keeper
ENET1_RX_EN	G16	NVCC_ENET	GPIO	ALT5	ENET1_RX_EN	Input	Keeper
ENET1_RX_ER	G14	NVCC_ENET	GPIO	ALT5	ENET1_RX_ER	Input	Keeper
ENET1_TX_CLK	G15	NVCC_ENET	GPIO	ALT5	ENET1_TX_CLK	Input	Keeper
ENET1_TX_DATA0	E16	NVCC_ENET	GPIO	ALT5	ENET1_TX_DATA0	Input	Keeper
ENET1_TX_DATA1	F13	NVCC_ENET	GPIO	ALT5	ENET1_TX_DATA1	Input	Keeper
ENET1_TX_EN	F15	NVCC_ENET	GPIO	ALT5	ENET1_TX_EN	Input	Keeper
ENET2_RX_DATA0	E17	NVCC_ENET	GPIO	ALT5	ENET2_RX_DATA0	Input	Keeper
ENET2_RX_DATA1	D17	NVCC_ENET	GPIO	ALT5	ENET2_RX_DATA1	Input	Keeper
ENET2_RX_EN	D16	NVCC_ENET	GPIO	ALT5	ENET2_RX_EN	Input	Keeper
ENET2_RX_ER	H13	NVCC_ENET	GPIO	ALT5	ENET2_RX_ER	Input	Keeper
ENET2_TX_CLK	H14	NVCC_ENET	GPIO	ALT5	ENET2_TX_CLK	Input	Keeper
ENET2_TX_DATA0	E14	NVCC_ENET	GPIO	ALT5	ENET2_TX_DATA0	Input	Keeper
ENET2_TX_DATA1	F14	NVCC_ENET	GPIO	ALT5	ENET2_TX_DATA1	Input	Keeper
ENET2_TX_EN	E15	NVCC_ENET	GPIO	ALT5	ENET2_TX_EN	Input	Keeper
GPIO1_IO00	M14	NVCC_GPIO	GPIO	ALT5	GPIO1_IO00	Input	Keeper
GPIO1_IO01	M15	NVCC_GPIO	GPIO	ALT5	GPIO1_IO01	Input	Keeper
GPIO1_IO02	M16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO02	Input	Keeper
GPIO1_IO03	N16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO03	Input	Keeper
GPIO1_IO04	N17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO04	Input	Keeper
GPIO1_IO05	P15	NVCC_GPIO	GPIO	ALT5	GPIO1_IO05	Input	Keeper
GPIO1_IO06	N15	NVCC_GPIO	GPIO	ALT5	GPIO1_IO06	Input	Keeper
GPIO1_IO07	N14	NVCC_GPIO	GPIO	ALT5	GPIO1_IO07	Input	Keeper
GPIO1_IO08	P14	NVCC_GPIO	GPIO	ALT5	GPIO1_IO08	Input	Keeper
GPIO1_IO09	P16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO09	Input	Keeper

6.2.3 9x9 mm, 0.5 mm pitch, ball map

Table 95 shows the 9x9 mm, 0.5 mm pitch ball map for the i.MX 6UltraLite.

Table 95. 9x9 mm, 0.5 mm Pitch, Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A		VSS	CSI_DATA06	SD1_DATA1	SD1_DATA0	NAND_DATA05	VSS	NAND_WEB	NAND_DATA01	LCD_ENABLE	LCD_DATA04	VSS	LCD_DATA09	LCD_DATA13	LCD_DATA16	LCD_DATA15	VSS	A
B	VSS	CSI_DATA02	CSI_DATA05	SD1_DATA3	SD1_DATA2	NAND_CE1_B	NAND_CLE	NAND_DATA07	NAND_DATA06	LCD_HSYNC	LCD_DATA03	LCD_DATA01	LCD_DATA08	LCD_DATA14	LCD_DATA18	LCD_DATA22	LCD_DATA20	B
C	CSI_MCLK	CSI_DATA07	CSI_DATA00	CSI_DATA04	SD1_CLK	SD1_CMD	NAND_DATA03	NAND_DATA04	NAND_DATA02	LCD_VSYNC	LCD_CLK	LCD_DATA07	LCD_DATA11	LCD_DATA12	VSS	LCD_DATA21	LCD_DATA23	C
D	CSI_DATA03	CSI_HSYNC	CSI_VSYNC	CSI_DATA01	CSI_PIXCLK	NAND_WP_B	NAND_DATA00	NAND_ALE	NAND_RE_B	LCD_DATA02	LCD_DATA00	LCD_DATA05	LCD_DATA06	LCD_DATA10	LCD_DATA17	ENET2_RX_EN	ENET2_RX_DATA1	D
E	DRAM_ODT1	DRAM_ADDR15	DRAM_ADDR14	DRAM_ADDR06	NVCC_CSI	NAND_DQS	NVCC_SD1	NAND_CE0_B	NAND_READY_B	LCD_RESET	NVCC_NAND	LCD_DATA19	NVCC_LCD	ENET2_TX_DATA0	ENET2_TX_EN	ENET1_TX_DATA0	ENET2_RX_DATA0	E
F	VSS	DRAM_RESET	VSS	DRAM_SDWE_B	DRAM_SDBA1			VSS		VSS			ENET1_TX_DATA1	ENET2_TX_DATA1	ENET1_TX_EN	ENET1_RX_DATA1	VSS	F
G	DRAM_ADDR00	DRAM_ADDR01	DRAM_SDBA2	DRAM_CAS_B	NVCC_DRAM		VDD_SOC_CAP	VDD_SOC_CAP	VDD_ARM_CAP	VDD_ARM_CAP	VDD_ARM_CAP		NVCC_ENET	ENET1_RX_ER	ENET1_TX_CLK	ENET1_RX_EN	ENET1_RX_DATA0	G