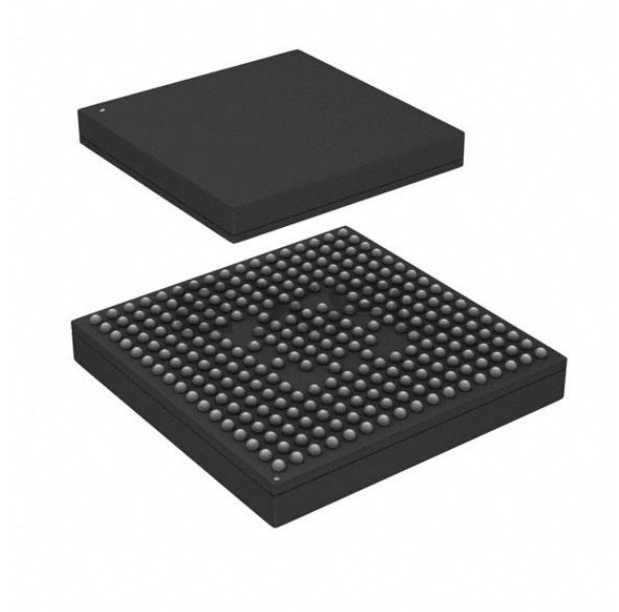

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	528MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	LCD, LVDS
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	272-LFBGA
Supplier Device Package	272-MAPBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6g3cvk05aa

- Four I^2C
- Two 10/100M Ethernet Controller (IEEE1588 compliant)
- Eight Pulse Width Modulators (PWM)
- System JTAG Controller (SJC)
- GPIO with interrupt capabilities
- 8x8 Key Pad Port (KPP)
- One Quad SPI
- Two Flexible Controller Area Network (FlexCAN)
- Three Watchdog timers (WDOG)
- Two 12-bit Analog to Digital Converters (ADC) with up to 10 input channels in total
- Touch Screen Controller (TSC)

The i.MX 6UltraLite processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Use Voltage Sensor for monitoring the die voltage
- Support DVFS techniques for low power modes
- Use SW State Retention and Power Gating for ARM and NEON
- Support various levels of system power modes
- Use flexible clock gating control scheme
- Two smart card interfaces compatible with EVM Standard 4.3

The i.MX 6UltraLite processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption, while having the CPU core relatively free for performing other tasks.

The i.MX 6UltraLite processors incorporate the following hardware accelerators:

- PXP—Pixel Processing Pipeline for imagine resize, rotation, overlay and CSC[1]. Off loading key pixel processing operations are required to support the LCD display applications.
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing cryptographic and hash engines, 32 KB secure RAM, and True and Pseudo Random Number Generator (NIST certified).
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock.
- CSU—Central Security Unit. CSU is configured during boot and by eFUSEs and determine the security level operation mode as well as the TZ policy.

1. G2 and G3 only

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPMI	General Purpose Memory Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices and 40-bit ECC for NAND Flash Controller (GPMI2). GPMI supports separate DMA channels for each NAND device.
GPT1 GPT2	General Purpose Timer	Timer peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
LCDIF	LCD interface	Connectivity peripherals	The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability. The LCDIF is designed to support dumb (synchronous 24-bit Parallel RGB interface) and smart (asynchronous parallel MPU interface) LCD devices.
MQS	Medium Quality Sound	Multimedia Peripherals	MQS is used to generate 2-channel medium quality PWM-like audio via two standard digital GPIO pins.
PWM1 PWM2 PWM3 PWM4 PWM5 PWM6 PWM7 PWM8	Pulse Width Modulation	Connectivity peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
PXP	Pixel Processing Pipeline	Display peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated EPD.

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
QSPI	Quad SPI	Connectivity peripherals	Quad SPI module act as an interface to external serial flash devices. This module contains the following features: • Flexible sequence engine to support various flash vendor devices • Single pad/Dual pad/Quad pad mode of operation • Single Data Rate/Double Data Rate mode of operation • Parallel Flash mode • DMA support • Memory mapped read access to connected flash devices • Multi-master access with priority and flexible and configurable buffer for each master
SAI1 SAI2 SAI3	—	—	The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast context-switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Support of byte-swapping • Library of Scripts and API is available
2x SIMv2	Smart Card	Connectivity peripherals	Smart card interface compliant with ISO7816.

3.1 Special signal considerations

Table 4 lists special signal considerations for the i.MX 6UltraLite processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, "Package information and contact assignments"." Signal descriptions are provided in the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

Table 4. Special Signal Considerations

Signal Name	Remarks
CCM_CLK1_P/ CCM_CLK1_N	One general purpose differential high speed clock Input/output is provided. It can be used: • To feed external reference clock to the PLLs and further to the modules inside SoC. • To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals. See the *i.MX 6UltraLite Reference Manual* (IMX6ULRM) for details on the respective clock trees. Alternatively one may use single ended signal to drive CLK1_P input. In this case corresponding CLK1_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. After initialization, the CLK1 input/output can be disabled (if not used). If unused either or both of the CLK1_N/P pairs may remain unconnected.
RTC_XTALI/RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal, (≤100 kΩ ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI, the RTC_XTALO pin must remain unconnected or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be <100 kHz under typical conditions. In case when high accuracy real time clock are not required system may use internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and keep RTC_XTALO unconnected.
XTALI/XTALO	A 24.0 MHz crystal should be connected between XTALI and XTALO. The crystal must be rated for a maximum drive level of 250 μW. An ESR (equivalent series resistance) of typical 80 Ω is recommended. NXP BSP (board support package) software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALO must be directly driven by the external oscillator and XTALI mounted with 18 pF capacitor. Please refer to the EVK board reference design for details. The logic level of this forcing clock cannot exceed NVCC_PLL level. If this clock is used as a reference for USB, then there are strict frequency tolerance and jitter requirements. See OSC24M chapter and relevant interface specifications chapters for details.

Table 8. Absolute Maximum Ratings (continued)

Supply Input Voltage to Secure Non-Volatile Storage and Real Time Clock	VDD_SNVS_IN	-0.3	3.6	
USB VBUS Supply	USB_OTG_VBUS	—	5.5	V
IO Supply for DDR Interface	NVCC_DRAM	-0.4	1.975 (see note1)	V
Supply for DDR pre-drivers	NVCC_DRAM_2P5	-0.3	2.85	V
IO Supply for GPIO Type Pins	NVCC_CSI NVCC_ENET NVCC_GPIO NVCC_LCD NVCC_NAND NVCC_SD1	-0.5	3.7	V
Supply for ADC 3P3V	VDDA_ADC_3P3	—	3.7	V
Input/Output Voltage range (Non-DDR Pins)	V_{in}/V_{out}	-0.5	OVDD + 0.3 (see note1)	V
Input/Output Voltage range (DDR Pins)	V_{in}/V_{out}	-0.5	OVDD + 0.4 (see note1, 2)	V
ESD damage Immunity: Human Body Model (HBM) Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	 V
Storage Temperature range	$T_{STORAGE}$	-40	150	°C

1 The absolute maximum voltage includes an allowance for 400 mV of overshoot on the IO pins. Per JEDEC standards, the allowed signal overshoot must be derated if NVCC_DRAM exceeds 1.575 V.

2 OVDD is the I/O supply voltage.

4.1.2 Thermal resistance

4.1.2.1 14x14 MM (VM) package thermal resistance

Table 9 displays the 14x14 MM (VM) package thermal resistance data.

Table 9. 14x14 MM (VM) Thermal Resistance Data[1]

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Ambient Natural convection	Single-layer board (1s)	$R_{\theta JA}$	58.4	°C/W	2,3
Junction to Ambient Natural convection	Four-layer board (2s2p)	$R_{\theta JA}$	37.6	°C/W	2,3,4
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	48.6	°C/W	2,4
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	32.9	°C/W	2,4
Junction to Board	—	$R_{\theta JB}$	21.8	°C/W	5

Table 25. LPDDR2 I/O DC Electrical Parameters[1] (continued)

Parameters	Symbol	Test Conditions	Min	Max	Unit
DC High-Level input voltage	Vih_DC	—	Vref+0.13	OVDD	V
DC Low-Level input voltage	Vil_DC	—	OVSS	Vref-0.13	V
Differential Input Logic High	Vih_diff	—	0.26	Note[2]	—
Differential Input Logic Low	Vil_diff	—	Note[2]	-0.26	—
Pull-up/Pull-down Impedance Mismatch	Mmpupd	—	-15	15	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper Circuit Resistance	Rkeep	—	110	175	kΩ
Input current (no pull-up/down)	Iin	VI = 0, VI = OVDD	-2.5	2.5	μA

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4.6.3.2 DDR3/DDR3L mode I/O DC parameters

The parameters in Table 27 are guaranteed per the operating ranges in Table 11, unless otherwise noted.

Table 27. DDR3/DDR3L I/O DC Electrical Characteristics

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -0.1mA Voh (for ipp_dse=001)	0.8*OVDD[1]	—	V
Low-level output voltage	VOL	Iol= 0.1mA Vol (for ipp_dse=001)	0.2*OVDD	—	V
High-level output voltage	VOH	Ioh= -1mA Voh (for all except ipp_dse=001)	0.8*OVDD	—	V
Low-level output voltage	VOL	Iol= 1mA Vol (for all except ipp_dse=001)	0.2*OVDD	—	V
Input Reference Voltage	Vref	—	0.49*ovdd	0.51*ovdd	V
DC High-Level input voltage	Vih_DC	—	Vref[2]+0.1	OVDD	V
DC Low-Level input voltage	Vil_DC	—	OVSS	Vref-0.1	V
Differential Input Logic High	Vih_diff	—	0.2	—	V
Differential Input Logic Low	Vil_diff	—	—	-0.2	V
Termination Voltage	Vtt	Vtt tracking OVDD/2	0.49*OVDD	0.51*OVDD	V
Pull-up/Pull-down Impedance Mismatch	Mmpupd	—	-10	10	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper Circuit Resistance	Rkeep	—	105	165	kΩ
Input current (no pull-up/down)	Iin	VI = 0,VI = OVDD	-2.9	2.9	μA

1 OVDD – I/O power supply (1.425 V–1.575 V for DDR3 and 1.283 V–1.45 V for DDR3L)

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM. Maximum operating frequency for EIM data transfer is 104 MHz. Timing parameters in this section that are given as a function of register settings or clock periods are valid for the entire range of allowed frequencies (0–104 MHz).

4.9.3.1 EIM interface pads allocation

EIM supports 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. Table 38 provides EIM interface pads allocation in different modes.

Table 38. EIM Internal Module Multiplexing[1]

Setup	Non Multiplexed Address/Data Mode						Multiplexed Address/Data mode
	8 Bit				16 Bit		16 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 110	MUM = 0, DSZ = 111	MUM = 0, DSZ = 001	MUM = 0, DSZ = 010	MUM = 1, DSZ = 001
EIM_ADDR [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]
EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]
EIM_DATA [07:00], EIM_EB0_B	EIM_DATA [07:00]	—	Reserved	Reserved	EIM_DATA [07:00]	Reserved	EIM_AD [07:00]
EIM_DATA [15:08], EIM_EB1_B	—	EIM_DATA [15:08]	Reserved	Reserved	EIM_DATA [15:08]	Reserved	EIM_AD [15:08]

[1] For more information on configuration ports mentioned in this table, see the *i.MX 6UltraLite Reference Manual (IMX6ULRM)*.

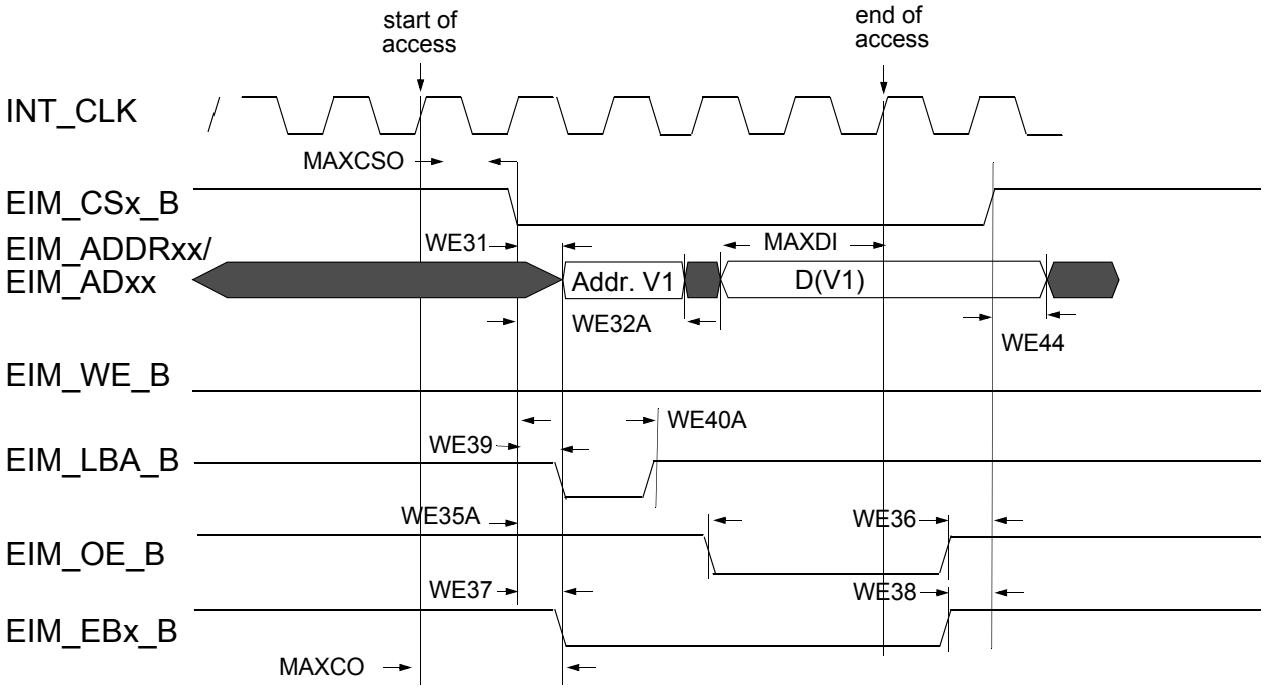

Figure 16. Asynchronous A/D Muxed Read Access (RWSC = 5)

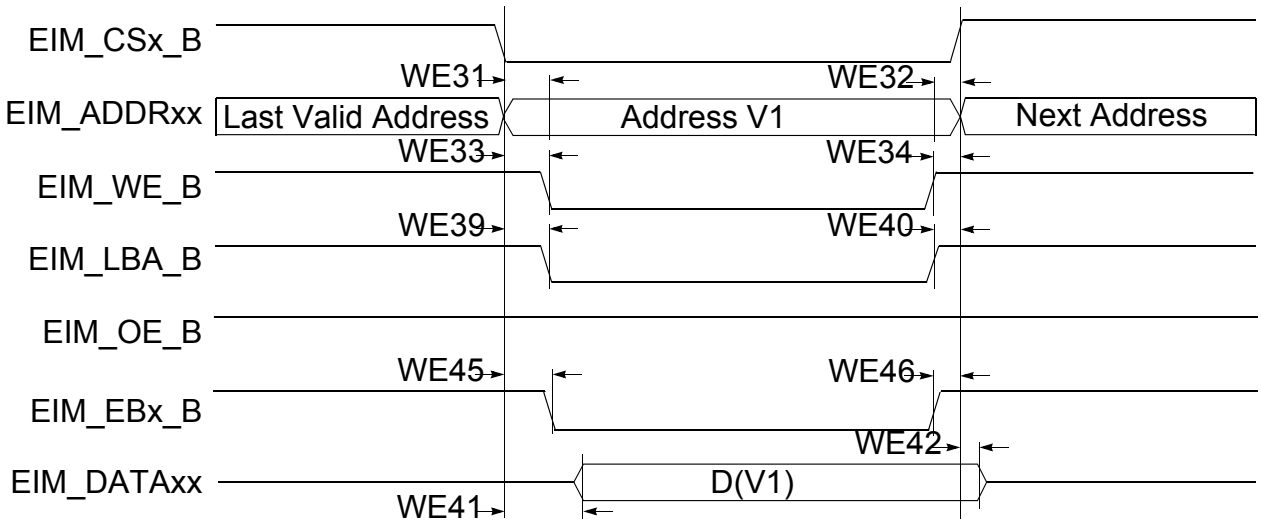

Figure 17. Asynchronous Memory Write Access

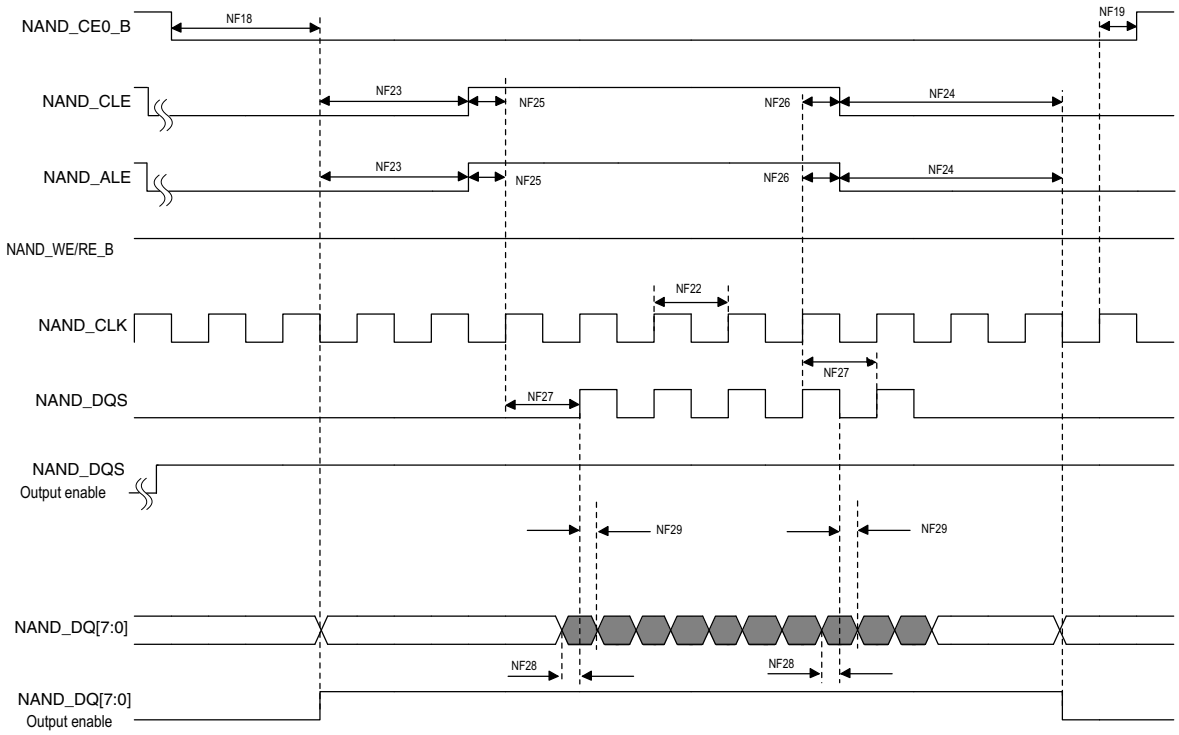

Figure 27. Source Synchronous Mode Data Write Timing Diagram

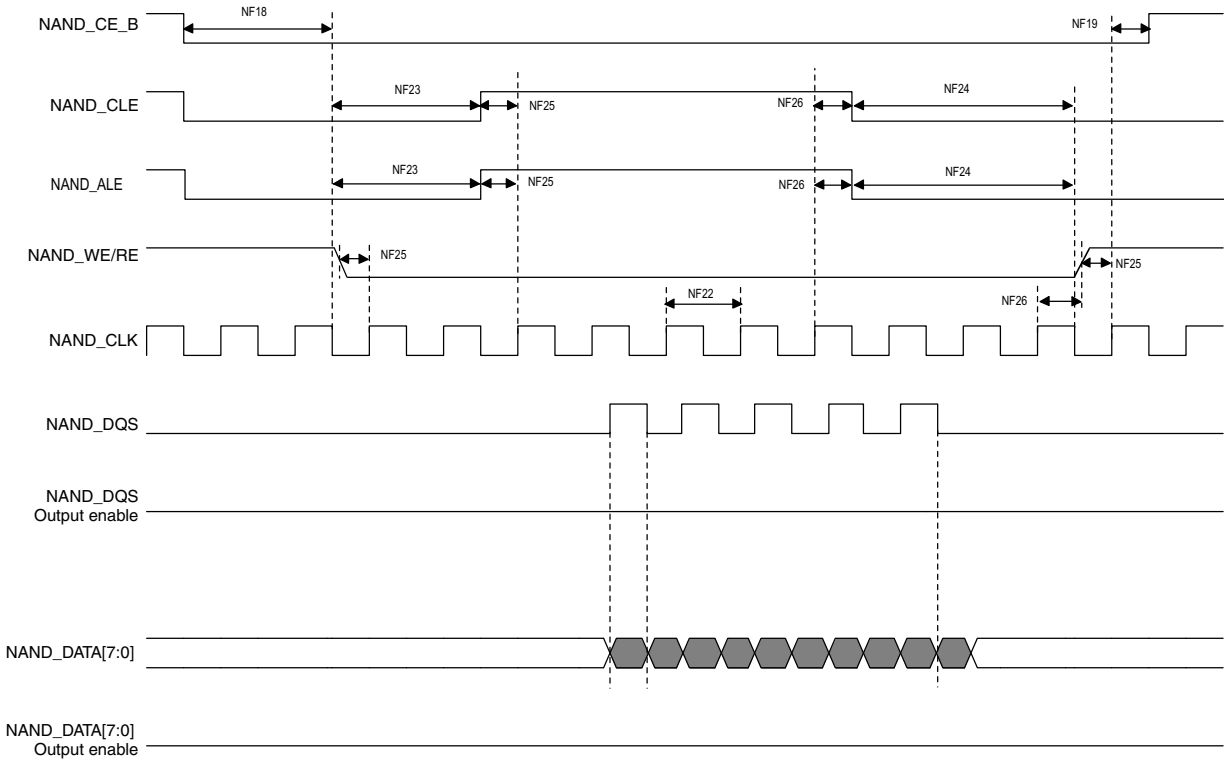

Figure 28. Source Synchronous Mode Data Read Timing Diagram

4.12.3.4 HS200 mode timing

Figure 40 depicts the timing of HS200 mode, and Table 52 lists the HS200 timing characteristics.

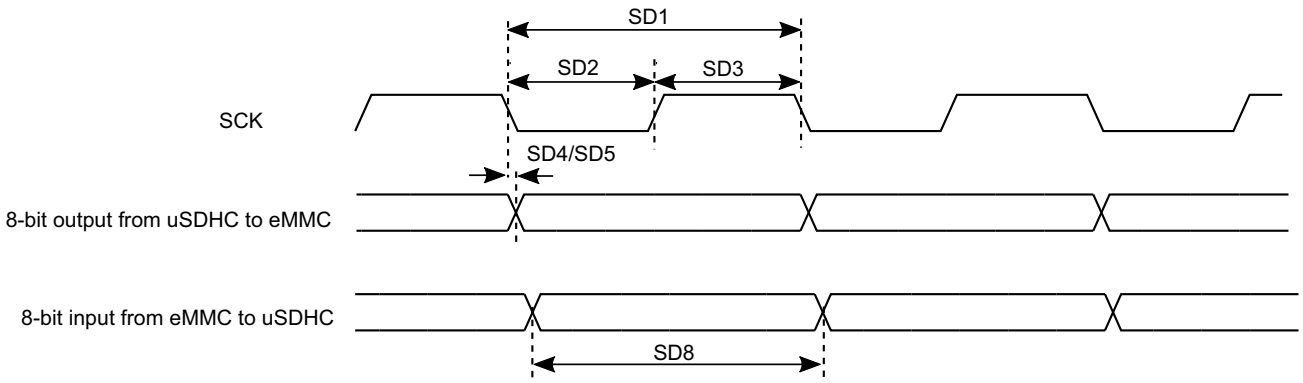

Figure 40. HS200 Mode Timing

Table 52. HS200 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

[1]HS200 is for 8 bits while SDR104 is for 4 bits.

4.12.3.5 Bus operation condition for 3.3 V and 1.8 V signaling

Signaling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1 supply are identical to those shown in Table 24, "Single Voltage GPIO DC Parameters," on page 34.

4.12.4 Ethernet Controller (ENET) AC electrical specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 64. QuadSPI Output/Write Timing (SDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{DVO}	Output data valid time	—	2	ns
T_{DHO}	Output data hold time	0	—	ns
T_{CK}	SCK clock period	10	—	ns
T_{CSS}	Chip select output setup time	3	—	SCK cycle(s)
T_{CSH}	Chip select output hold time	3	—	SCK cycle(s)

NOTE

T_{css} and T_{csh} are configured by the QuadSPIx_FLSHCR register, the default value of 3 are shown on the timing. Please refer to the *i.MX 6UltraLite Reference Manual (IMX6ULRM)* for more details.

4.12.9.2 DDR mode

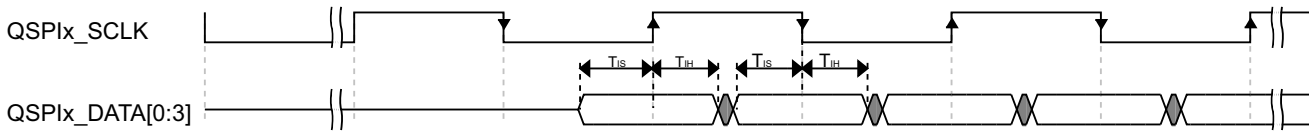

Figure 52. QuadSPI Input/Read Timing (DDR mode with internal sampling)

Table 65. QuadSPI Input/Read Timing (DDR mode with internal sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time requirement for incoming data	0	—	ns

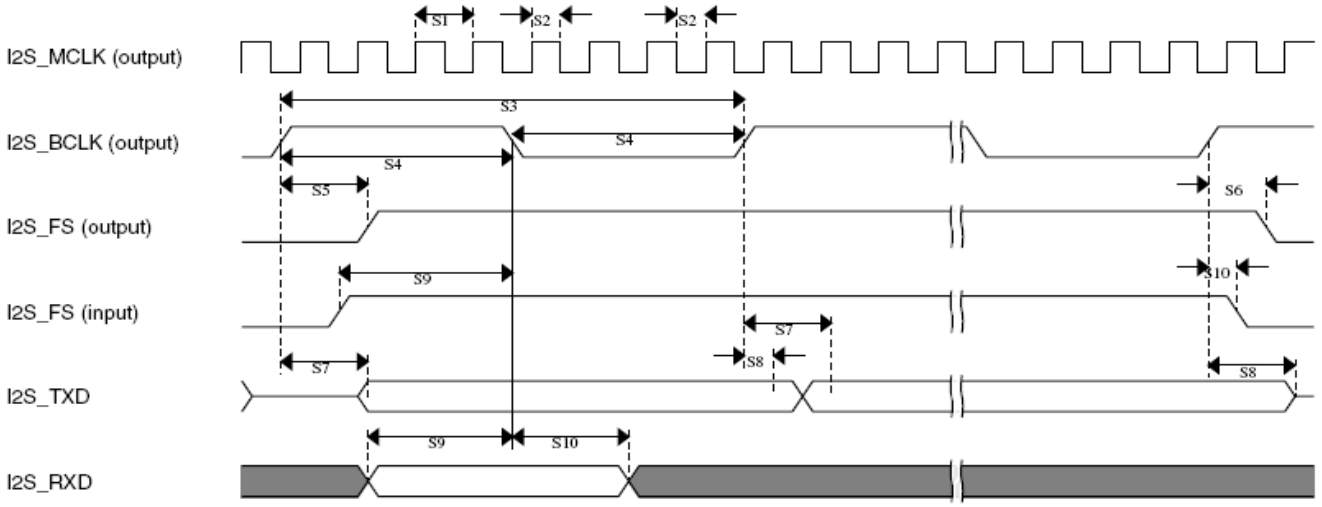

Figure 55. SAI Timing — Master Modes

Table 69. Master Mode SAI Timing

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	4 x t_{sys}	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	—	ns
S14	SAI_FA input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	20	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	ns
S17	SAI_RXD setup before SAI_BCLK	10	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

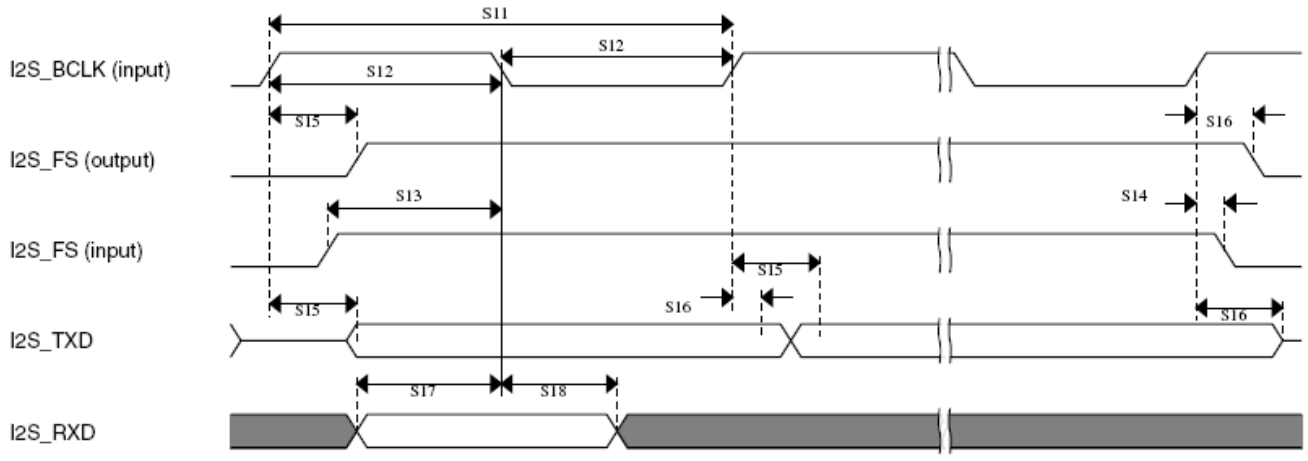

Figure 56. SAI Timing — Slave Modes

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART IrDA mode receiver

Figure 66 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 75 lists the receive timing characteristics.

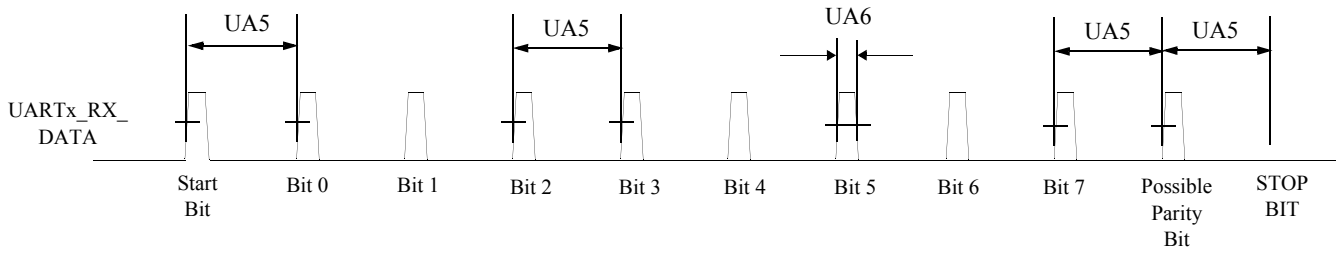

Figure 66. UART IrDA Mode Receive Timing Diagram

Table 75. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] - $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.12.14 USB PHY parameters

This section describes the USB-OTG PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG with the following amendments.

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs

Table 77. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	Comment
Sample Cycles	ADLSMP=0, ADSTS=00	Csamp	—	2	—	cycles	—
	ADLSMP=0, ADSTS=01			4			
	ADLSMP=0, ADSTS=10			6			
	ADLSMP=0, ADSTS=11			8			
	ADLSMP=1, ADSTS=00			12			
	ADLSMP=1, ADSTS=01			16			
	ADLSMP=1, ADSTS=10			20			
	ADLSMP=1, ADSTS=11			24			
Conversion Cycles	ADLSMP=0 ADSTS=00	Cconv	—	28	—	cycles	—
	ADLSMP=0 ADSTS=01			30			
	ADLSMP=0 ADSTS=10			32			
	ADLSMP=0 ADSTS=11			34			
	ADLSMP=1 ADSTS=00			38			
	ADLSMP=1 ADSTS=01			42			
	ADLSMP=1 ADSTS=10			46			
	ADLSMP=1, ADSTS=11			50			

Table 87. NOR/OneNAND Boot through EIM (continued)

Ball Name	Signal Name	Mux Mode	Common	ADL16 Non-Mux	AD16 Mux
NAND_ALE	weim.ADDR[17]	Alt 4		Yes	Yes
NAND_CE1_B	weim.ADDR[18]	Alt 4		Yes	Yes
SD1_CMD	weim.ADDR[19]	Alt 4		Yes	Yes
SD1_CLK	weim.ADDR[20]	Alt 4		Yes	Yes
SD1_DATA0	weim.ADDR[21]	Alt 4		Yes	Yes
SD1_DATA1	weim.ADDR[22]	Alt 4		Yes	Yes
SD1_DATA2	weim.ADDR[23]	Alt 4		Yes	Yes
SD1_DATA3	weim.ADDR[24]	Alt 4		Yes	Yes
ENET2_RXER	weim.ADDR[25]	Alt 4		Yes	Yes
ENET2_CRS_DV	weim.ADDR[26]	Alt 4		Yes	Yes
CSI_MCLK	weim.CS0_B	Alt 4	Yes		
LCD_DATA08	weim.DATA[0]	Alt 4		Yes	
LCD_DATA09	weim.DATA[1]	Alt 4		Yes	
LCD_DATA10	weim.DATA[2]	Alt 4		Yes	
LCD_DATA11	weim.DATA[3]	Alt 4		Yes	
LCD_DATA12	weim.DATA[4]	Alt 4		Yes	
LCD_DATA13	weim.DATA[5]	Alt 4		Yes	
LCD_DATA14	weim.DATA[6]	Alt 4		Yes	
LCD_DATA15	weim.DATA[7]	Alt 4		Yes	
LCD_DATA16	weim.DATA[8]	Alt 4		Yes	
LCD_DATA17	weim.DATA[9]	Alt 4		Yes	
LCD_DATA18	weim.DATA[10]	Alt 4		Yes	
LCD_DATA19	weim.DATA[11]	Alt 4		Yes	
LCD_DATA20	weim.DATA[12]	Alt 4		Yes	
LCD_DATA21	weim.DATA[13]	Alt 4		Yes	
LCD_DATA22	weim.DATA[14]	Alt 4		Yes	
LCD_DATA23	weim.DATA[15]	Alt 4		Yes	
NAND_RE_B	weim.EB_B[0]	Alt 4		Yes	Yes
NAND_WE_B	weim.EB_B[1]	Alt 4		Yes	Yes
CSI_HSYNC	weim.LBA_B	Alt 4	Yes		
CSI_PIXCLK	weim.OE	Alt 4	Yes		
CSI_VSYNC	weim.RW	Alt 4	Yes		

Table 91. 14x14 mm Functional Contact Assignments (continued)

DRAM_DATA09	U3	NVCC_DRAM	DDR	ALT0	DRAM_DATA09	Input	100 kΩ pull-up
DRAM_DATA10	U5	NVCC_DRAM	DDR	ALT0	DRAM_DATA10	Input	100 kΩ pull-up
DRAM_DATA11	R4	NVCC_DRAM	DDR	ALT0	DRAM_DATA11	Input	100 kΩ pull-up
DRAM_DATA12	P5	NVCC_DRAM	DDR	ALT0	DRAM_DATA12	Input	100 kΩ pull-up
DRAM_DATA13	P3	NVCC_DRAM	DDR	ALT0	DRAM_DATA13	Input	100 kΩ pull-up
DRAM_DATA14	R2	NVCC_DRAM	DDR	ALT0	DRAM_DATA14	Input	100 kΩ pull-up
DRAM_DATA15	R1	NVCC_DRAM	DDR	ALT0	DRAM_DATA15	Input	100 kΩ pull-up
DRAM_DQM0	T7	NVCC_DRAM	DDR	ALT0	DRAM_DQM0	Output	100 kΩ pull-up
DRAM_DQM1	T3	NVCC_DRAM	DDR	ALT0	DRAM_DQM1	Output	100 kΩ pull-up
DRAM_ODT0	N1	NVCC_DRAM	DDR	ALT0	DRAM_ODT0	Output	100 kΩ pull-down
DRAM_ODT1	F1	NVCC_DRAM	DDR	ALT0	DRAM_ODT1	Output	100 kΩ pull-down
DRAM_RAS_B	M5	NVCC_DRAM	DDR	ALT0	DRAM_RAS_B	Output	100 kΩ pull-up
DRAM_RESET	G4	NVCC_DRAM	DDR	ALT0	DRAM_RESET	Output	100 kΩ pull-down
DRAM_SDBA0	M1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA0	Output	100 kΩ pull-up
DRAM_SDBA1	H1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA1	Output	100 kΩ pull-up
DRAM_SDBA2	K2	NVCC_DRAM	DDR	ALT0	DRAM_SDBA2	Output	100 kΩ pull-up
DRAM_SDCKE0	M3	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE0	Output	100 kΩ pull-down
DRAM_SDCKE1	J3	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE1	Output	100 kΩ pull-down
DRAM_SDCLK0_N	P2	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_N	Input	100 kΩ pull-up
DRAM_SDCLK0_P	P1	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_P	Input	100 kΩ pull-up
DRAM_SDQS0_N	P7	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_N	Input	100 kΩ pull-down

Table 91. 14x14 mm Functional Contact Assignments (continued)

SNVS_TAMPER0	R10	VDD_SNVS_IN	GPIO	—	GPIO5_IO00/SNVS_TAMPER0[1]	Input	Keeper[1]
SNVS_TAMPER1	R9	VDD_SNVS_IN	GPIO	—	GPIO5_IO01/SNVS_TAMPER1[1]	Input	Keeper[1]
SNVS_TAMPER2	P11	VDD_SNVS_IN	GPIO	—	GPIO5_IO02/SNVS_TAMPER2[1]	Input	Keeper[1]
SNVS_TAMPER3	P10	VDD_SNVS_IN	GPIO	—	GPIO5_IO03/SNVS_TAMPER3[1]	Input	Keeper[1]
SNVS_TAMPER4	P9	VDD_SNVS_IN	GPIO	—	GPIO5_IO04/SNVS_TAMPER4[1]	Input	Keeper[1]
SNVS_TAMPER5	N8	VDD_SNVS_IN	GPIO	—	GPIO5_IO05/SNVS_TAMPER5[1]	Input	Keeper[1]
SNVS_TAMPER6	N11	VDD_SNVS_IN	GPIO	—	GPIO5_IO06/SNVS_TAMPER6[1]	Input	Keeper[1]
SNVS_TAMPER7	N10	VDD_SNVS_IN	GPIO	—	GPIO5_IO07/SNVS_TAMPER7[1]	Input	Keeper[1]
SNVS_TAMPER8	N9	VDD_SNVS_IN	GPIO	—	GPIO5_IO08/SNVS_TAMPER8[1]	Input	Keeper[1]
SNVS_TAMPER9	R6	VDD_SNVS_IN	GPIO	—	GPIO5_IO09/SNVS_TAMPER9[1]	Input	Keeper[1]
TEST_MODE	N7	VDD_SNVS_IN	GPIO	ALT0	TEST_MODE	Input	Keeper
UART1_CTS_B	K15	NVCC_UART	GPIO	ALT5	UART1_CTS_B	Input	Keeper
UART1_RTS_B	J14	NVCC_UART	GPIO	ALT5	UART1_RTS_B	Input	Keeper
UART1_RX_DATA	K16	NVCC_UART	GPIO	ALT5	UART1_RX_DATA	Input	Keeper
UART1_TX_DATA	K14	NVCC_UART	GPIO	ALT5	UART1_TX_DATA	Input	Keeper
UART2_CTS_B	J15	NVCC_UART	GPIO	ALT5	UART2_CTS_B	Input	Keeper
UART2_RTS_B	H14	NVCC_UART	GPIO	ALT5	UART2_RTS_B	Input	Keeper
UART2_RX_DATA	J16	NVCC_UART	GPIO	ALT5	UART2_RX_DATA	Input	Keeper
UART2_TX_DATA	J17	NVCC_UART	GPIO	ALT5	UART2_TX_DATA	Input	Keeper
UART3_CTS_B	H15	NVCC_UART	GPIO	ALT5	UART3_CTS_B	Input	Keeper
UART3_RTS_B	G14	NVCC_UART	GPIO	ALT5	UART3_RTS_B	Input	Keeper
UART3_RX_DATA	H16	NVCC_UART	GPIO	ALT5	UART3_RX_DATA	Input	Keeper
UART3_TX_DATA	H17	NVCC_UART	GPIO	ALT5	UART3_TX_DATA	Input	Keeper
UART4_RX_DATA	G16	NVCC_UART	GPIO	ALT5	UART4_RX_DATA	Input	Keeper
UART4_TX_DATA	G17	NVCC_UART	GPIO	ALT5	UART4_TX_DATA	Input	Keeper
UART5_RX_DATA	G13	NVCC_UART	GPIO	ALT5	UART5_RX_DATA	Input	Keeper
UART5_TX_DATA	F17	NVCC_UART	GPIO	ALT5	UART5_TX_DATA	Input	Keeper
USB_OTG1_CHD_B	U16	OPEN DRAIN	GPIO	—	USB_OTG1_CHD_B	—	—

Table 92. 14x14 mm, 0.8 mm Pitch, Ball Map (continued)

	U	T	R	P
1	VSS	DRAM_SDQS1_P	DRAM_DATA15	DRAM_SDCLK0_P
2	DRAM_DATA08	DRAM_SDQS1_N	DRAM_DATA14	DRAM_SDCLK0_N
3	DRAM_DATA09	DRAM_DQM1	VSS	DRAM_DATA13
4	DRAM_DATA07	DRAM_DATA00	DRAM_DATA11	DRAM_VREF
5	DRAM_DATA10	DRAM_DATA06	VSS	DRAM_DATA12
6	DRAM_DATA01	DRAM_DATA02	SNVS_TAMPER9	DRAM_SDQS0_P
7	DRAM_DATA03	DRAM_DQM0	VSS	DRAM_SDQS0_N
8	DRAM_DATA04	DRAM_DATA05	ONOFF	POR_B
9	CCM_PMIC_STBY_REQ	SNVS_PMIC_ON_REQ	SNVS_TAMPER1	SNVS_TAMPER4
10	BOOT_MODE1	BOOT_MODE0	SNVS_TAMPER0	SNVS_TAMPER3
11	RTC_XTALO	RTC_XTALI	VSS	SNVS_TAMPER2
12	USB_OTG2_VBUS	USB_OTG1_VBUS	VDD_USB_CAP	VDD_SNVS_IN
13	USB_OTG2_DP	USB_OTG2_DN	GPANAIO	NVCC_PLL
14	VSS	VSS	VDD_HIGH_CAP	JTAG_TMS
15	USB_OTG1_DP	USB_OTG1_DN	VDD_HIGH_CAP	JTAG_MOD
16	USB_OTG1_CHD_B	XTALI	VSS	CCM_CLK1_N
17	VSS	XTALO	VSS	CCM_CLK1_P
	U	T	R	P

6.2 9x9 mm package information

6.2.1 9x9 mm, 0.5 mm pitch, ball matrix

Figure 69 shows the top, bottom, and side views of the 9x9 mm BGA package.

Table 94. 9x9 mm Functional Contact Assignments (continued)

DRAM_ADDR07	J4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR07	Output	100 kΩ pull-up
DRAM_ADDR08	J5	NVCC_DRAM	DDR	ALT0	DRAM_ADDR08	Output	100 kΩ pull-up
DRAM_ADDR09	J1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR09	Output	100 kΩ pull-up
DRAM_ADDR10	M2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR10	Output	100 kΩ pull-up
DRAM_ADDR11	K5	NVCC_DRAM	DDR	ALT0	DRAM_ADDR11	Output	100 kΩ pull-up
DRAM_ADDR12	L3	NVCC_DRAM	DDR	ALT0	DRAM_ADDR12	Output	100 kΩ pull-up
DRAM_ADDR13	H4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR13	Output	100 kΩ pull-up
DRAM_ADDR14	E3	NVCC_DRAM	DDR	ALT0	DRAM_ADDR14	Output	100 kΩ pull-up
DRAM_ADDR15	E2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR15	Output	100 kΩ pull-up
DRAM_CAS_B	G4	NVCC_DRAM	DDR	ALT0	DRAM_CAS_B	Output	100 kΩ pull-up
DRAM_CS0_B	L1	NVCC_DRAM	DDR	ALT0	DRAM_CS0_B	Output	100 kΩ pull-up
DRAM_CS1_B	H5	NVCC_DRAM	DDR	ALT0	DRAM_CS1_B	Output	100 kΩ pull-up
DRAM_DATA00	T3	NVCC_DRAM	DDR	ALT0	DRAM_DATA00	Input	100 kΩ pull-up
DRAM_DATA01	N5	NVCC_DRAM	DDR	ALT0	DRAM_DATA01	Input	100 kΩ pull-up
DRAM_DATA02	T4	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	100 kΩ pull-up
DRAM_DATA03	T5	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	100 kΩ pull-up
DRAM_DATA04	U5	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	100 kΩ pull-up
DRAM_DATA05	T6	NVCC_DRAM	DDR	ALT0	DRAM_DATA05	Input	100 kΩ pull-up
DRAM_DATA06	R4	NVCC_DRAM	DDR	ALT0	DRAM_DATA06	Input	100 kΩ pull-up
DRAM_DATA07	U3	NVCC_DRAM	DDR	ALT0	DRAM_DATA07	Input	100 kΩ pull-up
DRAM_DATA08	P1	NVCC_DRAM	DDR	ALT0	DRAM_DATA08	Input	100 kΩ pull-up

Table 94. 9x9 mm Functional Contact Assignments (continued)

SNVS_TAMPER0	R8	VDD_SNVS_IN	GPIO	—	GPIO5_IO00/SNVS_TAMPER0[1]	Input	Keeper/non-connected[1,2]
SNVS_TAMPER1	P6	VDD_SNVS_IN	GPIO	—	GPIO5_IO01/SNVS_TAMPER1[1]	Input	Keeper/non-connected[1,2]
SNVS_TAMPER2	N10	VDD_SNVS_IN	GPIO	—	GPIO5_IO02/SNVS_TAMPER2[1]	Input	Keeper/non-connected[1,2]
SNVS_TAMPER3	P10	VDD_SNVS_IN	GPIO	—	GPIO5_IO03/SNVS_TAMPER3[1]	Input	Keeper/non-connected[1,2]
SNVS_TAMPER4	P7	VDD_SNVS_IN	GPIO	—	GPIO5_IO04/SNVS_TAMPER4[1]	Input	Keeper/non-connected[1,2]
SNVS_TAMPER5	P8	VDD_SNVS_IN	GPIO	—	GPIO5_IO05/SNVS_TAMPER5[1]	Input	Keeper/non-connected[1,2]
SNVS_TAMPER6	R7	VDD_SNVS_IN	GPIO	—	GPIO5_IO06/SNVS_TAMPER6[1]	Input	Keeper/non-connected[1,2]
SNVS_TAMPER7	N9	VDD_SNVS_IN	GPIO	—	GPIO5_IO07/SNVS_TAMPER7[1]	Input	Keeper/non-connected[1,2]
SNVS_TAMPER8	N8	VDD_SNVS_IN	GPIO	—	GPIO5_IO08/SNVS_TAMPER8[1]	Input	Keeper/non-connected[1,2]
SNVS_TAMPER9	P9	VDD_SNVS_IN	GPIO	—	GPIO5_IO09/SNVS_TAMPER9[1]	Input	Keeper/non-connected[1,2]
TEST_MODE	N7	VDD_SNVS_IN	GPIO	ALT0	TEST_MODE	Input	Keeper
UART1_CTS_B	L14	NVCC_UART	GPIO	ALT5	UART1_CTS_B	Input	Keeper
UART1_RTS_B	K14	NVCC_UART	GPIO	ALT5	UART1_RTS_B	Input	Keeper
UART1_RX_DATA	L17	NVCC_UART	GPIO	ALT5	UART1_RX_DATA	Input	Keeper
UART1_TX_DATA	L15	NVCC_UART	GPIO	ALT5	UART1_TX_DATA	Input	Keeper
UART2_CTS_B	J17	NVCC_UART	GPIO	ALT5	UART2_CTS_B	Input	Keeper
UART2_RTS_B	J14	NVCC_UART	GPIO	ALT5	UART2_RTS_B	Input	Keeper
UART2_RX_DATA	K16	NVCC_UART	GPIO	ALT5	UART2_RX_DATA	Input	Keeper
UART2_TX_DATA	L16	NVCC_UART	GPIO	ALT5	UART2_TX_DATA	Input	Keeper
UART3_CTS_B	H16	NVCC_UART	GPIO	ALT5	UART3_CTS_B	Input	Keeper
UART3_RTS_B	H15	NVCC_UART	GPIO	ALT5	UART3_RTS_B	Input	Keeper
UART3_RX_DATA	K15	NVCC_UART	GPIO	ALT5	UART3_RX_DATA	Input	Keeper