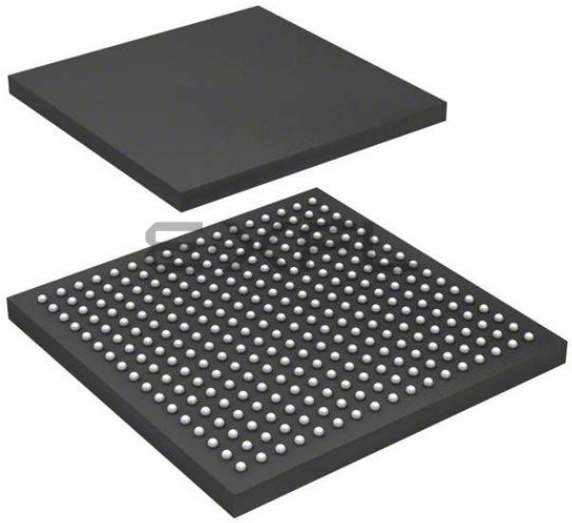

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	528MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	LCD, LVDS
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6g3cvm05aa

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC1 uSDHC2	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6UltraLite specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.5/4.2/4.3/4.4/4.41/ including high-capacity (size > 2 GB) cards HC MMC. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDXC cards up to 2 TB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v3.0 Two ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) • 4-bit or 8-bit transfer mode specifications for eMMC chips up to 200 MHz in HS200 mode (200 MB/s max)
USB	Universal Serial Bus 2.0	Connectivity Peripherals	USBO2 (USB OTG1 and USB OTG2) contains: • Two high-speed OTG 2.0 modules with integrated HS USB PHYs • Support eight Transmit (TX) and eight Receive (Rx) endpoints, including endpoint 0
WDOG1 WDOG3	Watch Dog	Timer Peripherals	The Watch Dog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG2 (TZ)	Watch Dog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW.

Table 5. JTAG Controller Interface Summary (continued)

JTAG	I/O Type	On-chip Termination
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

3.2 Recommended connections for unused analog interfaces

Table 6 shows the recommended connections for unused analog interfaces.

Table 6. Recommended Connections for Unused Analog Interfaces

Module	Pad Name	Recommendations if Unused
CCM	CCM_CLK1_N, CCM_CLK1_P	Float
USB	USB_OTG1_CHD_B, USB_OTG1_DN, USB_OTG1_DP, USB_OTG1_VBUS, USB_OTG2_CHD_B, USB_OTG2_DN, USB_OTG2_DP, USB_OTG2_VBUS	Float
ADC	ADC_VREFH	Tie to VDDA_ADC_3P3
	VDDA_ADC_3P3	VDDA_ADC_3P3 must be powered even if the ADC is not used.

4.4.3 Ethernet PLL

Table 19. Ethernet PLL's Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.4 480 MHz PLL

Table 20. 480 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles

4.4.5 ARM PLL

Table 21. ARM PLL's Electrical Parameters

Parameter	Value
Clock output range	648 MHz ~ 1296 MHz
Reference clock	24 MHz
Lock time	<2250 reference cycles

4.5 On-Chip oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implement an oscillator. The oscillator is powered from NVCC_PLL.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implement a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDD_HIGH_IN such as the oscillator consumes

Table 24. Single Voltage GPIO DC Parameters (continued)

Parameter	Symbol	Test Conditions	Min	Max	Units
Input Hysteresis (OVDD= 1.8V)	VHYS_LowVDD	OVDD=1.8V	250	—	mV
Input Hysteresis (OVDD=3.3V)	VHYS_HighVDD	OVDD=3.3V	250	—	mV
Schmitt trigger VT+[2,3]	VTH+	—	0.5*OVDD	—	mV
Schmitt trigger VT-[2,3]	VTH-	—	—	0.5*OVDD	mV
Pull-up resistor (22_kΩ PU)	RPU_22K	Vin=0V	—	212	μA
Pull-up resistor (22_kΩ PU)	RPU_22K	Vin=OVDD	—	1	μA
Pull-up resistor (47_kΩ PU)	RPU_47K	Vin=0V	—	100	μA
Pull-up resistor (47_kΩ PU)	RPU_47K	Vin=OVDD	—	1	μA
Pull-up resistor (100_kΩ PU)	RPU_100K	Vin=0V	—	48	μA
Pull-up resistor (100_kΩ PU)	RPU_100K	Vin=OVDD	—	1	μA
Pull-down resistor (100_kΩ PD)	RPD_100K	Vin=OVDD	—	48	μA
Pull-down resistor (100_kΩ PD)	RPD_100K	Vin=0V	—	1	μA
Input current (no PU/PD)	IIN	VI = 0, VI = OVDD	-1	1	μA
Keeper Circuit Resistance	R_Keeper	VI =0.3*OVDD, VI = 0.7* OVDD	105	175	kΩ

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

3 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.3 DDR I/O DC parameters

The DDR I/O pads support LPDDR2 and DDR3/DDR3L operational modes. For details on supported DDR memory configurations, see Section 4.10, “Multi-Mode DDR Controller (MMDC)".

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for the i.MX 6UltraLite Applications Processor* (IMX6ULHDG).

4.6.3.1 LPDDR2 mode I/O DC parameters

Table 25. LPDDR2 I/O DC Electrical Parameters[1]

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -0.1mA	0.9*OVDD	—	V
Low-level output voltage	VOL	Iol= 0.1mA	—	0.1*OVDD	V
Input Reference Voltage	Vref	—	0.49*OVDD	0.51*OVDD	V

Table 29. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 30. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	ns
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.7.2 DDR I/O AC parameters

The Multi-mode DDR Controller (MMDC) is compatible with JEDEC-compliant SDRAMs. For details on supported DDR memory configurations, see Section 4.10, "Multi-Mode DDR Controller (MMDC)".

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for the i.MX 6UltraLite Applications Processor* (IMX6ULHDG).

Table 31 shows the AC parameters for DDR I/O operating in LPDDR2 mode.

Table 31. DDR I/O LPDDR2 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	OVDD	V
AC input logic low	Vil(ac)	—	0	Vref - 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	V

Table 31. DDR I/O LPDDR2 Mode AC Parameters[1] (continued)

Parameter	Symbol	Test Condition	Min	Max	Unit
AC differential input low voltage	Vidl(ac)	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	-0.12	0.12	V
Over/undershoot peak	Vpeak	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	0.3	V-ns
Single output slew rate, measured between Vol (ac) and Voh (ac)	tsr	50 Ω to Vref. 5 pF load. Drive impedance = 40 Ω ± 30%	1.5	3.5	V/ns
		50 Ω to Vref. 5pF load.Drive impedance = 60 Ω ± 30%	1	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	0.1	ns

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage | Vtr - Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 32 shows the AC parameters for DDR I/O operating in DDR3/DDR3L mode.

Table 32. DDR I/O DDR3/DDR3L Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref - 0.175	V
AC differential input voltage[2]	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	Vref - 0.15	—	Vref + 0.15	V
Over/undershoot peak	Vpeak	—	—	—	0.4	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.5	V-ns
Single output slew rate, measured between Vol (ac) and Voh (ac)	tsr	Driver impedance = 34 Ω	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC JESD79_3D specification supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage | Vtr-Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 39. EIM Bus Timing Parameters (continued)

ID	Parameter	Min[1]	Max[1]	Unit
WE5	Clock rise to address invalid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE6	Clock rise to EIM_CSx_B valid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE7	Clock rise to EIM_CSx_B invalid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE8	Clock rise to EIM_WE_B Valid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE9	Clock rise to EIM_WE_B Invalid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE10	Clock rise to EIM_OE_B Valid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE11	Clock rise to EIM_OE_B Invalid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE12	Clock rise to EIM_EBx_B Valid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE13	Clock rise to EIM_EBx_B Invalid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE14	Clock rise to EIM_LBA_B Valid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE15	Clock rise to EIM_LBA_B Invalid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE16	Clock rise to Output Data Valid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE17	Clock rise to Output Data Invalid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE18	Input Data setup time to Clock rise	2.3	—	ns
WE19	Input Data hold time from Clock rise	2	—	ns
WE20	EIM_WAIT_B setup time to Clock rise	2	—	ns
WE21	EIM_WAIT_B hold time from Clock rise	2	—	ns

1 k represents register setting BCD value.

2 t is clock period (1/Freq.) For 104 MHz, t = 9.165 ns.

Figure 11 to Figure 14 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

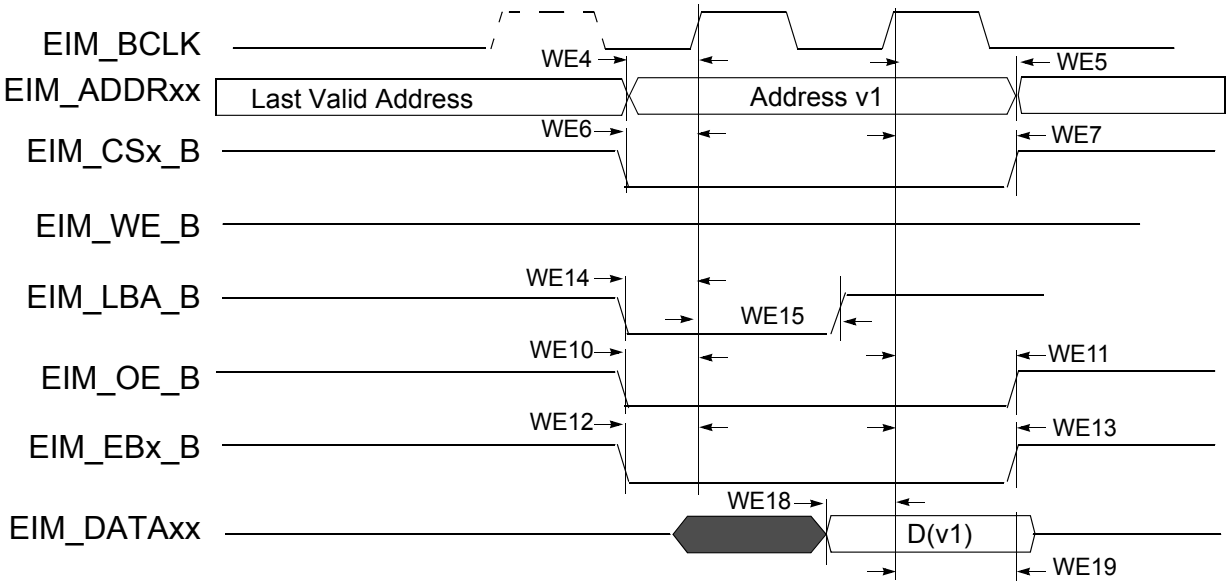

Figure 11. Synchronous Memory Read Access, WSC=1

Table 40. EIM Asynchronous Timing Parameters Table Relative Chip to Select[1,2]

Ref No.	Parameter	Determination by Synchronous measured parameters	Min	Max	Unit
WE45	EIM_CSx_B Valid to EIM_EBx_B Valid (Write access)	WE12 - WE6 + (WBEA - WCSA) x t	-3.5 + (WBEA - WCSA) x t	3.5 + (WBEA - WCSA) x t	ns
WE46	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - WCSN) x t	-3.5 + (WBEN - WCSN) x t	3.5 + (WBEN - WCSN) x t	ns
MAXDTI	MAXIMUM delay from EIM_DTACK_B to its internal flip-flop + 2 cycles for synchronization	10	—	10	—
WE47	EIM_DTACK_B Active to EIM_CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	EIM_CSx_B Invalid to EIM_DTACK_B Invalid	0	0	—	ns

1 For more information on configuration parameters mentioned in this table, see the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

2 In this table, CSA means WCSA when write operation or RCSA when read operation
— t means clock period from axi_clk frequency.
—CSA means register setting for WCSA when in write operations or RCSA when in read operations.
—CSN means register setting for WCSN when in write operations or RCSN when in read operations.
—ADVN means register setting for WADVN when in write operations or RADVN when in read operations.
—ADVA means register setting for WADVA when in write operations or RADVA when in read operations.

4.10 Multi-Mode DDR Controller (MMDC)

The Multi-Mode DDR Controller is a dedicated interface to DDR3/DDR3L/LPDDR2 SDRAM.

4.10.1 MMDC compatibility with JEDEC-compliant SDRAMs

The i.MX 6UltraLite MMDC supports the following memory types:

- LPDDR2 SDRAM compliant with JESD209-2B LPDDR2 JEDEC standard release June, 2009
- DDR3/DDR3L SDRAM compliant with JESD79-3D DDR3 JEDEC standard release April, 2008

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for the i.MX 6UltraLite Applications Processor (IMX6ULHDG)*.

Table 44. Samsung Toggle Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF28	Data write setup	tDS[6]	0.25 × tCK - 0.32	—	ns
NF29	Data write hold	tDH[6]	0.25 × tCK - 0.79	—	ns
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ[7]	—	3.18	—
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS[7]	—	3.27	—

1 The GPMI toggle mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = tCK (GPMI clock period) -0.075ns (half of maximum p-p jitter).

4 CE_DELAY represents HW_GPMI_TIMING2[CE_DELAY]. NF18 is guaranteed by the design. Read/Write operation is started with enough time of ALE/CLE assertion to low level.

5 PRE_DELAY+1) ≥ (AS+DS)

6 Shown in Figure 30.

7 Shown in Figure 31.

For DDR Toggle mode, Figure 29 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 1.4 ns (max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of an delayed NAND_DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the *i.MX 6UltraLite Reference Manual*). Generally, the typical delay value is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.12 External peripheral interface parameters

The following subsections provide information on external peripheral interfaces.

4.12.1 CMOS Sensor Interface (CSI) timing parameters

4.12.1.0.1 Gated clock mode timing

Figure 32 and Figure 33 shows the gated clock mode timings for CSI, and Table 45 describes the timing parameters (P1–P7) shown in the figures. A frame starts with a rising/falling edge on CSI_VSYNC

[2] SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.12.2.2 ECSPI slave mode timing

Figure 36 depicts the timing of ECSPI in slave mode. Table 48 lists the ECSPI slave mode timing characteristics.

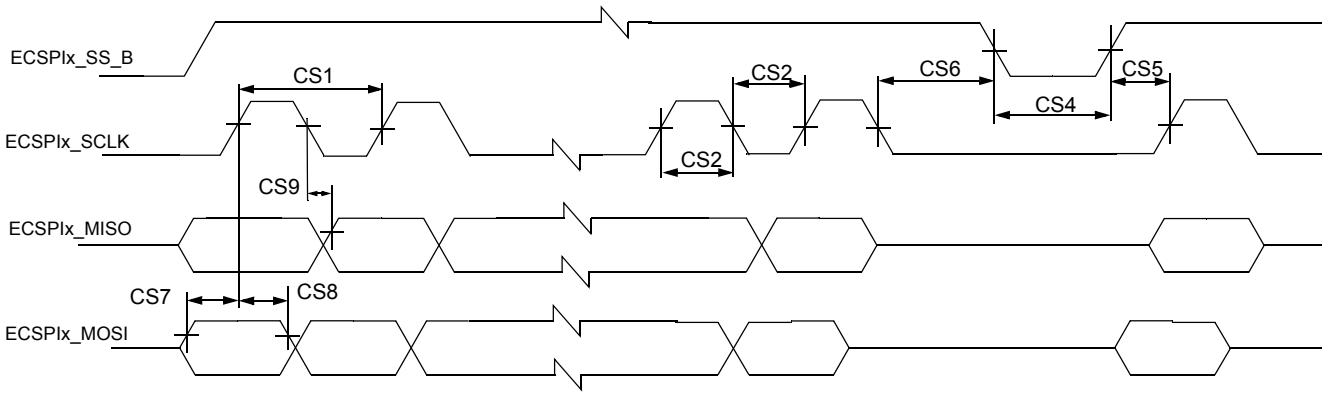

Figure 36. ECSPI Slave Mode Timing Diagram

Table 48. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPI_SCLK Cycle Time–Write	t_{clk}	15 43	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	7 21.5	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPIx_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPIx_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPIx_MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	19	ns

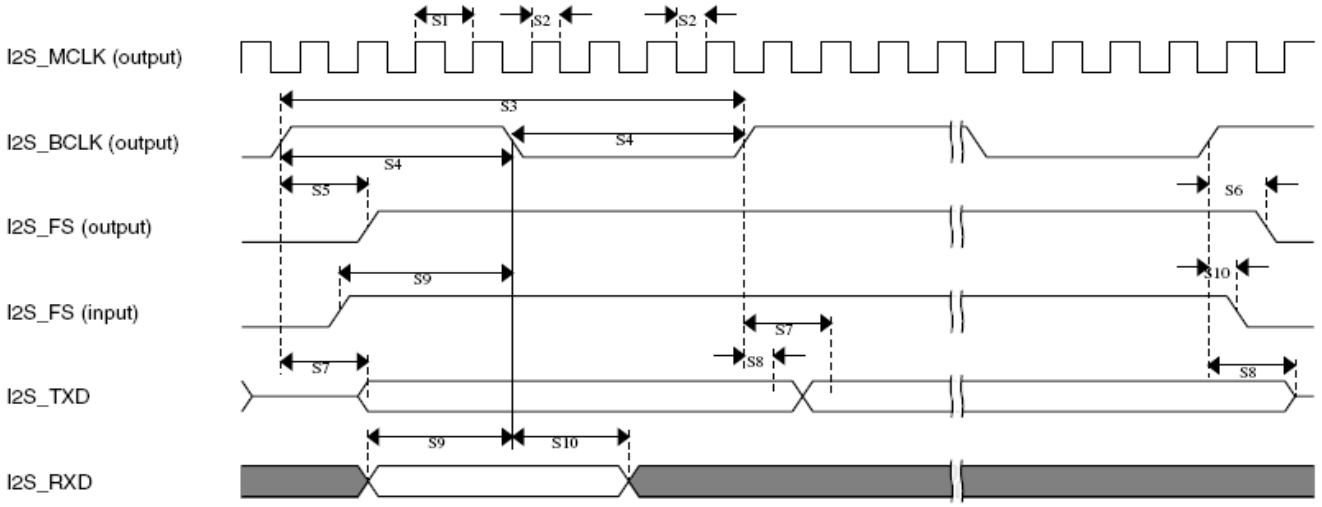

Figure 55. SAI Timing — Master Modes

Table 69. Master Mode SAI Timing

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	4 x t_{sys}	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	—	ns
S14	SAI_FA input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	20	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	ns
S17	SAI_RXD setup before SAI_BCLK	10	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

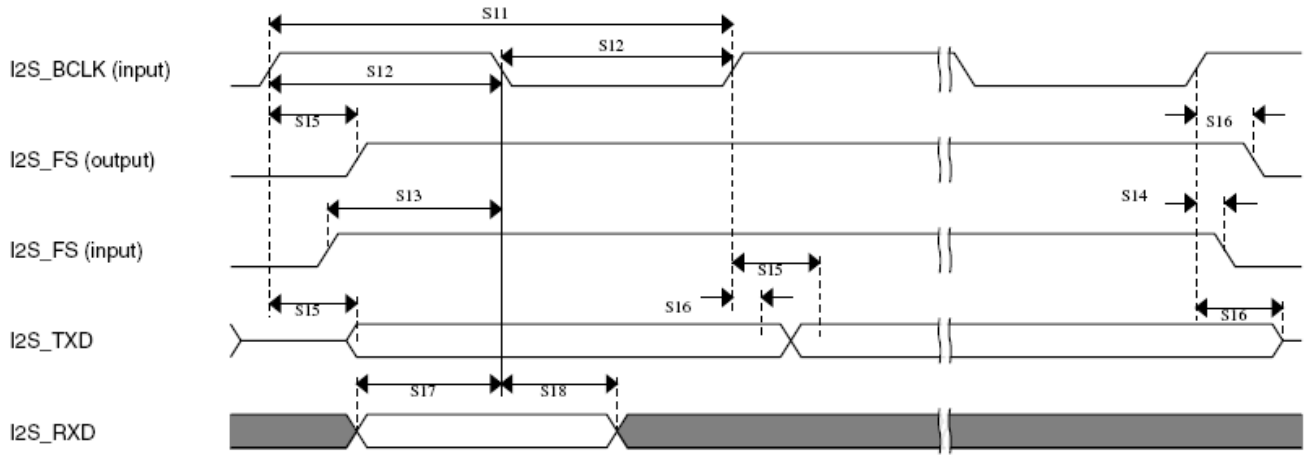

Figure 56. SAI Timing — Slave Modes

[2] Typical values assume V_{DDAD} = 3.0 V, Temp = 25°C, F_{adck}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

NOTE

The ADC electrical spec would be met with the calibration enabled configuration.

Table 78. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at reset	eFuse name	Details
LCD_DATA00	Input with 100 K pull-down	BT_CFG1[0]	Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
LCD_DATA01	Input with 100 K pull-down	BT_CFG1[1]	
LCD_DATA02	Input with 100 K pull-down	BT_CFG1[2]	
LCD_DATA03	Input with 100 K pull-down	BT_CFG1[3]	
LCD_DATA04	Input with 100 K pull-down	BT_CFG1[4]	
LCD_DATA05	Input with 100 K pull-down	BT_CFG1[5]	
LCD_DATA06	Input with 100 K pull-down	BT_CFG1[6]	
LCD_DATA07	Input with 100 K pull-down	BT_CFG1[7]	
LCD_DATA08	Input with 100 K pull-down	BT_CFG2[0]	
LCD_DATA09	Input with 100 K pull-down	BT_CFG2[1]	
LCD_DATA10	Input with 100 K pull-down	BT_CFG2[2]	
LCD_DATA11	Input with 100 K pull-down	BT_CFG2[3]	
LCD_DATA12	Input with 100 K pull-down	BT_CFG2[4]	
LCD_DATA13	Input with 100 K pull-down	BT_CFG2[5]	
LCD_DATA14	Input with 100 K pull-down	BT_CFG2[6]	
LCD_DATA15	Input with 100 K pull-down	BT_CFG2[7]	
LCD_DATA16	Input with 100 K pull-down	BT_CFG4[0]	
LCD_DATA17	Input with 100 K pull-down	BT_CFG4[1]	
LCD_DATA18	Input with 100 K pull-down	BT_CFG4[2]	
LCD_DATA19	Input with 100 K pull-down	BT_CFG4[3]	
LCD_DATA20	Input with 100 K pull-down	BT_CFG4[4]	
LCD_DATA21	Input with 100 K pull-down	BT_CFG4[5]	
LCD_DATA22	Input with 100 K pull-down	BT_CFG4[6]	
LCD_DATA23	Input with 100 K pull-down	BT_CFG4[7]	

5.2 Boot device interface allocation

The following tables list the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The tables also describe the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 79. QSPI Boot trough QSPI

Ball Name	Signal Name	Mux Mode	Common	Quad Mode	+ Port A DQS	+ Port A CS1	+ Port B	+ Port B DQS	+ Port B CS1
NAND_WP_B	qspi.A_SCLK	Alt2	Yes	Yes					
NAND_DQS	qspi.A_SS0_B	Alt2	Yes	Yes					

6 Package information and contact assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 14x14 mm package information

6.1.1 14x14 mm, 0.8 mm pitch, ball matrix

Figure 68 shows the top, bottom, and side views of the 14x14 mm BGA package.

Table 91. 14x14 mm Functional Contact Assignments (continued)

DRAM_DATA09	U3	NVCC_DRAM	DDR	ALT0	DRAM_DATA09	Input	100 kΩ pull-up
DRAM_DATA10	U5	NVCC_DRAM	DDR	ALT0	DRAM_DATA10	Input	100 kΩ pull-up
DRAM_DATA11	R4	NVCC_DRAM	DDR	ALT0	DRAM_DATA11	Input	100 kΩ pull-up
DRAM_DATA12	P5	NVCC_DRAM	DDR	ALT0	DRAM_DATA12	Input	100 kΩ pull-up
DRAM_DATA13	P3	NVCC_DRAM	DDR	ALT0	DRAM_DATA13	Input	100 kΩ pull-up
DRAM_DATA14	R2	NVCC_DRAM	DDR	ALT0	DRAM_DATA14	Input	100 kΩ pull-up
DRAM_DATA15	R1	NVCC_DRAM	DDR	ALT0	DRAM_DATA15	Input	100 kΩ pull-up
DRAM_DQM0	T7	NVCC_DRAM	DDR	ALT0	DRAM_DQM0	Output	100 kΩ pull-up
DRAM_DQM1	T3	NVCC_DRAM	DDR	ALT0	DRAM_DQM1	Output	100 kΩ pull-up
DRAM_ODT0	N1	NVCC_DRAM	DDR	ALT0	DRAM_ODT0	Output	100 kΩ pull-down
DRAM_ODT1	F1	NVCC_DRAM	DDR	ALT0	DRAM_ODT1	Output	100 kΩ pull-down
DRAM_RAS_B	M5	NVCC_DRAM	DDR	ALT0	DRAM_RAS_B	Output	100 kΩ pull-up
DRAM_RESET	G4	NVCC_DRAM	DDR	ALT0	DRAM_RESET	Output	100 kΩ pull-down
DRAM_SDBA0	M1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA0	Output	100 kΩ pull-up
DRAM_SDBA1	H1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA1	Output	100 kΩ pull-up
DRAM_SDBA2	K2	NVCC_DRAM	DDR	ALT0	DRAM_SDBA2	Output	100 kΩ pull-up
DRAM_SDCKE0	M3	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE0	Output	100 kΩ pull-down
DRAM_SDCKE1	J3	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE1	Output	100 kΩ pull-down
DRAM_SDCLK0_N	P2	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_N	Input	100 kΩ pull-up
DRAM_SDCLK0_P	P1	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_P	Input	100 kΩ pull-up
DRAM_SDQS0_N	P7	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_N	Input	100 kΩ pull-down

Table 91. 14x14 mm Functional Contact Assignments (continued)

DRAM_SDQS0_P	P6	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_P	Input	100 kΩ pull-down
DRAM_SDQS1_N	T2	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_N	Input	100 kΩ pull-down
DRAM_SDQS1_P	T1	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_P	Input	100 kΩ pull-down
DRAM_SDWE_B	J1	NVCC_DRAM	DDR	ALT0	DRAM_SDWE_B	Output	100 kΩ pull-up
DRAM_ZQPAD	N4	NVCC_DRAM	GPIO	—	DRAM_ZQPAD	Input	Keeper
ENET1_RX_DATA0	F16	NVCC_ENET	GPIO	ALT5	ENET1_RX_DATA0	Input	Keeper
ENET1_RX_DATA1	E17	NVCC_ENET	GPIO	ALT5	ENET1_RX_DATA1	Input	Keeper
ENET1_RX_EN	E16	NVCC_ENET	GPIO	ALT5	ENET1_RX_EN	Input	Keeper
ENET1_RX_ER	D15	NVCC_ENET	GPIO	ALT5	ENET1_RX_ER	Input	Keeper
ENET1_TX_CLK	F14	NVCC_ENET	GPIO	ALT5	ENET1_TX_CLK	Input	Keeper
ENET1_TX_DATA0	E15	NVCC_ENET	GPIO	ALT5	ENET1_TX_DATA0	Input	Keeper
ENET1_TX_DATA1	E14	NVCC_ENET	GPIO	ALT5	ENET1_TX_DATA1	Input	Keeper
ENET1_TX_EN	F15	NVCC_ENET	GPIO	ALT5	ENET1_TX_EN	Input	Keeper
ENET2_RX_DATA0	C17	NVCC_ENET	GPIO	ALT5	ENET2_RX_DATA0	Input	Keeper
ENET2_RX_DATA1	C16	NVCC_ENET	GPIO	ALT5	ENET2_RX_DATA1	Input	Keeper
ENET2_RX_EN	B17	NVCC_ENET	GPIO	ALT5	ENET2_RX_EN	Input	Keeper
ENET2_RX_ER	D16	NVCC_ENET	GPIO	ALT5	ENET2_RX_ER	Input	Keeper
ENET2_TX_CLK	D17	NVCC_ENET	GPIO	ALT5	ENET2_TX_CLK	Input	Keeper
ENET2_TX_DATA0	A15	NVCC_ENET	GPIO	ALT5	ENET2_TX_DATA0	Input	Keeper
ENET2_TX_DATA1	A16	NVCC_ENET	GPIO	ALT5	ENET2_TX_DATA1	Input	Keeper
ENET2_TX_EN	B15	NVCC_ENET	GPIO	ALT5	ENET2_TX_EN	Input	Keeper
GPIO1_IO00	K13	NVCC_GPIO	GPIO	ALT5	GPIO1_IO00	Input	Keeper
GPIO1_IO01	L15	NVCC_GPIO	GPIO	ALT5	GPIO1_IO01	Input	Keeper
GPIO1_IO02	L14	NVCC_GPIO	GPIO	ALT5	GPIO1_IO02	Input	Keeper
GPIO1_IO03	L17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO03	Input	Keeper
GPIO1_IO04	M16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO04	Input	Keeper
GPIO1_IO05	M17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO05	Input	Keeper
GPIO1_IO06	K17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO06	Input	Keeper
GPIO1_IO07	L16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO07	Input	Keeper
GPIO1_IO08	N17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO08	Input	Keeper
GPIO1_IO09	M15	NVCC_GPIO	GPIO	ALT5	GPIO1_IO09	Input	Keeper

Table 91. 14x14 mm Functional Contact Assignments (continued)

JTAG_MOD	P15	NVCC_GPIO	GPIO	ALT5	JTAG_MOD	Input	100 kΩ pull-up
JTAG_TCK	M14	NVCC_GPIO	GPIO	ALT5	JTAG_TCK	Input	47 kΩ pull-up
JTAG_TDI	N16	NVCC_GPIO	GPIO	ALT5	JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	N15	NVCC_GPIO	GPIO	ALT5	JTAG_TDO	Output	Keeper
JTAG_TMS	P14	NVCC_GPIO	GPIO	ALT5	JTAG_TMS	Input	47 kΩ pull-up
JTAG_TRST_B	N14	NVCC_GPIO	GPIO	ALT5	JTAG_TRST_B	Input	47 kΩ pull-up
LCD_CLK	A8	NVCC_LCD	GPIO	ALT5	LCD_CLK	Input	Keeper
LCD_DATA00	B9	NVCC_LCD	GPIO	ALT5	LCD_DATA00	Input	Keeper
LCD_DATA01	A9	NVCC_LCD	GPIO	ALT5	LCD_DATA01	Input	Keeper
LCD_DATA02	E10	NVCC_LCD	GPIO	ALT5	LCD_DATA02	Input	Keeper
LCD_DATA03	D10	NVCC_LCD	GPIO	ALT5	LCD_DATA03	Input	Keeper
LCD_DATA04	C10	NVCC_LCD	GPIO	ALT5	LCD_DATA04	Input	Keeper
LCD_DATA05	B10	NVCC_LCD	GPIO	ALT5	LCD_DATA05	Input	Keeper
LCD_DATA06	A10	NVCC_LCD	GPIO	ALT5	LCD_DATA06	Input	Keeper
LCD_DATA07	D11	NVCC_LCD	GPIO	ALT5	LCD_DATA07	Input	Keeper
LCD_DATA08	B11	NVCC_LCD	GPIO	ALT5	LCD_DATA08	Input	Keeper
LCD_DATA09	A11	NVCC_LCD	GPIO	ALT5	LCD_DATA09	Input	Keeper
LCD_DATA10	E12	NVCC_LCD	GPIO	ALT5	LCD_DATA10	Input	Keeper
LCD_DATA11	D12	NVCC_LCD	GPIO	ALT5	LCD_DATA11	Input	Keeper
LCD_DATA12	C12	NVCC_LCD	GPIO	ALT5	LCD_DATA12	Input	Keeper
LCD_DATA13	B12	NVCC_LCD	GPIO	ALT5	LCD_DATA13	Input	Keeper
LCD_DATA14	A12	NVCC_LCD	GPIO	ALT5	LCD_DATA14	Input	Keeper
LCD_DATA15	D13	NVCC_LCD	GPIO	ALT5	LCD_DATA15	Input	Keeper
LCD_DATA16	C13	NVCC_LCD	GPIO	ALT5	LCD_DATA16	Input	Keeper
LCD_DATA17	B13	NVCC_LCD	GPIO	ALT5	LCD_DATA17	Input	Keeper
LCD_DATA18	A13	NVCC_LCD	GPIO	ALT5	LCD_DATA18	Input	Keeper
LCD_DATA19	D14	NVCC_LCD	GPIO	ALT5	LCD_DATA19	Input	Keeper
LCD_DATA20	C14	NVCC_LCD	GPIO	ALT5	LCD_DATA20	Input	Keeper
LCD_DATA21	B14	NVCC_LCD	GPIO	ALT5	LCD_DATA21	Input	Keeper
LCD_DATA22	A14	NVCC_LCD	GPIO	ALT5	LCD_DATA22	Input	Keeper
LCD_DATA23	B16	NVCC_LCD	GPIO	ALT5	LCD_DATA23	Input	Keeper

Table 94. 9x9 mm Functional Contact Assignments (continued)

DRAM_ADDR07	J4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR07	Output	100 kΩ pull-up
DRAM_ADDR08	J5	NVCC_DRAM	DDR	ALT0	DRAM_ADDR08	Output	100 kΩ pull-up
DRAM_ADDR09	J1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR09	Output	100 kΩ pull-up
DRAM_ADDR10	M2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR10	Output	100 kΩ pull-up
DRAM_ADDR11	K5	NVCC_DRAM	DDR	ALT0	DRAM_ADDR11	Output	100 kΩ pull-up
DRAM_ADDR12	L3	NVCC_DRAM	DDR	ALT0	DRAM_ADDR12	Output	100 kΩ pull-up
DRAM_ADDR13	H4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR13	Output	100 kΩ pull-up
DRAM_ADDR14	E3	NVCC_DRAM	DDR	ALT0	DRAM_ADDR14	Output	100 kΩ pull-up
DRAM_ADDR15	E2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR15	Output	100 kΩ pull-up
DRAM_CAS_B	G4	NVCC_DRAM	DDR	ALT0	DRAM_CAS_B	Output	100 kΩ pull-up
DRAM_CS0_B	L1	NVCC_DRAM	DDR	ALT0	DRAM_CS0_B	Output	100 kΩ pull-up
DRAM_CS1_B	H5	NVCC_DRAM	DDR	ALT0	DRAM_CS1_B	Output	100 kΩ pull-up
DRAM_DATA00	T3	NVCC_DRAM	DDR	ALT0	DRAM_DATA00	Input	100 kΩ pull-up
DRAM_DATA01	N5	NVCC_DRAM	DDR	ALT0	DRAM_DATA01	Input	100 kΩ pull-up
DRAM_DATA02	T4	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	100 kΩ pull-up
DRAM_DATA03	T5	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	100 kΩ pull-up
DRAM_DATA04	U5	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	100 kΩ pull-up
DRAM_DATA05	T6	NVCC_DRAM	DDR	ALT0	DRAM_DATA05	Input	100 kΩ pull-up
DRAM_DATA06	R4	NVCC_DRAM	DDR	ALT0	DRAM_DATA06	Input	100 kΩ pull-up
DRAM_DATA07	U3	NVCC_DRAM	DDR	ALT0	DRAM_DATA07	Input	100 kΩ pull-up
DRAM_DATA08	P1	NVCC_DRAM	DDR	ALT0	DRAM_DATA08	Input	100 kΩ pull-up

Table 94. 9x9 mm Functional Contact Assignments (continued)

DRAM_DATA09	U2	NVCC_DRAM	DDR	ALT0	DRAM_DATA09	Input	100 kΩ pull-up
DRAM_DATA10	P3	NVCC_DRAM	DDR	ALT0	DRAM_DATA10	Input	100 kΩ pull-up
DRAM_DATA11	R2	NVCC_DRAM	DDR	ALT0	DRAM_DATA11	Input	100 kΩ pull-up
DRAM_DATA12	P4	NVCC_DRAM	DDR	ALT0	DRAM_DATA12	Input	100 kΩ pull-up
DRAM_DATA13	N2	NVCC_DRAM	DDR	ALT0	DRAM_DATA13	Input	100 kΩ pull-up
DRAM_DATA14	N1	NVCC_DRAM	DDR	ALT0	DRAM_DATA14	Input	100 kΩ pull-up
DRAM_DATA15	P2	NVCC_DRAM	DDR	ALT0	DRAM_DATA15	Input	100 kΩ pull-up
DRAM_DQM0	U4	NVCC_DRAM	DDR	ALT0	DRAM_DQM0	Output	100 kΩ pull-up
DRAM_DQM1	R1	NVCC_DRAM	DDR	ALT0	DRAM_DQM1	Output	100 kΩ pull-up
DRAM_ODT0	K2	NVCC_DRAM	DDR	ALT0	DRAM_ODT0	Output	100 kΩ pull-down
DRAM_ODT1	E1	NVCC_DRAM	DDR	ALT0	DRAM_ODT1	Output	100 kΩ pull-down
DRAM_RAS_B	L4	NVCC_DRAM	DDR	ALT0	DRAM_RAS_B	Output	100 kΩ pull-up
DRAM_RESET	F2	NVCC_DRAM	DDR	ALT0	DRAM_RESET	Output	100 kΩ pull-down
DRAM_SDBA0	H3	NVCC_DRAM	DDR	ALT0	DRAM_SDBA0	Output	100 kΩ pull-up
DRAM_SDBA1	F5	NVCC_DRAM	DDR	ALT0	DRAM_SDBA1	Output	100 kΩ pull-up
DRAM_SDBA2	G3	NVCC_DRAM	DDR	ALT0	DRAM_SDBA2	Output	100 kΩ pull-up
DRAM_SDCKE0	L2	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE0	Output	100 kΩ pull-down
DRAM_SDCKE1	K1	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE1	Output	100 kΩ pull-down
DRAM_SDCLK0_N	K4	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_N	Input	100 kΩ pull-up
DRAM_SDCLK0_P	K3	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_P	Input	100 kΩ pull-up
DRAM_SDQS0_N	R5	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_N	Input	100 kΩ pull-down

Table 94. 9x9 mm Functional Contact Assignments (continued)

JTAG_MOD	R13	NVCC_GPIO	GPIO	ALT5	JTAG_MOD	Input	100 kΩ pull-up
JTAG_TCK	R17	NVCC_GPIO	GPIO	ALT5	JTAG_TCK	Input	47 kΩ pull-up
JTAG_TDI	P17	NVCC_GPIO	GPIO	ALT5	JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	R16	NVCC_GPIO	GPIO	ALT5	JTAG_TDO	Output	Keeper
JTAG_TMS	R14	NVCC_GPIO	GPIO	ALT5	JTAG_TMS	Input	47 kΩ pull-up
JTAG_TRST_B	P13	NVCC_GPIO	GPIO	ALT5	JTAG_TRST_B	Input	47 kΩ pull-up
LCD_CLK	C11	NVCC_LCD	GPIO	ALT5	LCD_CLK	Input	Keeper
LCD_DATA00	D11	NVCC_LCD	GPIO	ALT5	LCD_DATA00	Input	Keeper
LCD_DATA01	B12	NVCC_LCD	GPIO	ALT5	LCD_DATA01	Input	Keeper
LCD_DATA02	D10	NVCC_LCD	GPIO	ALT5	LCD_DATA02	Input	Keeper
LCD_DATA03	B11	NVCC_LCD	GPIO	ALT5	LCD_DATA03	Input	Keeper
LCD_DATA04	A11	NVCC_LCD	GPIO	ALT5	LCD_DATA04	Input	Keeper
LCD_DATA05	D12	NVCC_LCD	GPIO	ALT5	LCD_DATA05	Input	Keeper
LCD_DATA06	D13	NVCC_LCD	GPIO	ALT5	LCD_DATA06	Input	Keeper
LCD_DATA07	C12	NVCC_LCD	GPIO	ALT5	LCD_DATA07	Input	Keeper
LCD_DATA08	B13	NVCC_LCD	GPIO	ALT5	LCD_DATA08	Input	Keeper
LCD_DATA09	A13	NVCC_LCD	GPIO	ALT5	LCD_DATA09	Input	Keeper
LCD_DATA10	D14	NVCC_LCD	GPIO	ALT5	LCD_DATA10	Input	Keeper
LCD_DATA11	C13	NVCC_LCD	GPIO	ALT5	LCD_DATA11	Input	Keeper
LCD_DATA12	C14	NVCC_LCD	GPIO	ALT5	LCD_DATA12	Input	Keeper
LCD_DATA13	A14	NVCC_LCD	GPIO	ALT5	LCD_DATA13	Input	Keeper
LCD_DATA14	B14	NVCC_LCD	GPIO	ALT5	LCD_DATA14	Input	Keeper
LCD_DATA15	A16	NVCC_LCD	GPIO	ALT5	LCD_DATA15	Input	Keeper
LCD_DATA16	A15	NVCC_LCD	GPIO	ALT5	LCD_DATA16	Input	Keeper
LCD_DATA17	D15	NVCC_LCD	GPIO	ALT5	LCD_DATA17	Input	Keeper
LCD_DATA18	B15	NVCC_LCD	GPIO	ALT5	LCD_DATA18	Input	Keeper
LCD_DATA19	E12	NVCC_LCD	GPIO	ALT5	LCD_DATA19	Input	Keeper
LCD_DATA20	B17	NVCC_LCD	GPIO	ALT5	LCD_DATA20	Input	Keeper
LCD_DATA21	C16	NVCC_LCD	GPIO	ALT5	LCD_DATA21	Input	Keeper
LCD_DATA22	B16	NVCC_LCD	GPIO	ALT5	LCD_DATA22	Input	Keeper
LCD_DATA23	C17	NVCC_LCD	GPIO	ALT5	LCD_DATA23	Input	Keeper