Infineon Technologies - TC1728N192F133HRACKXUMA2 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	133MHz
Connectivity	ASC, CANbus, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	127
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	152K x 8
Voltage - Supply (Vcc/Vdd)	1.17V ~ 3.63V
Data Converters	A/D 4x10b, 32x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	PG-LQFP-176-6
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1728n192f133hrackxuma2

Table of Contents

3 Pinning

Figure 3-1 shows the TC1728 Logic Symbol.

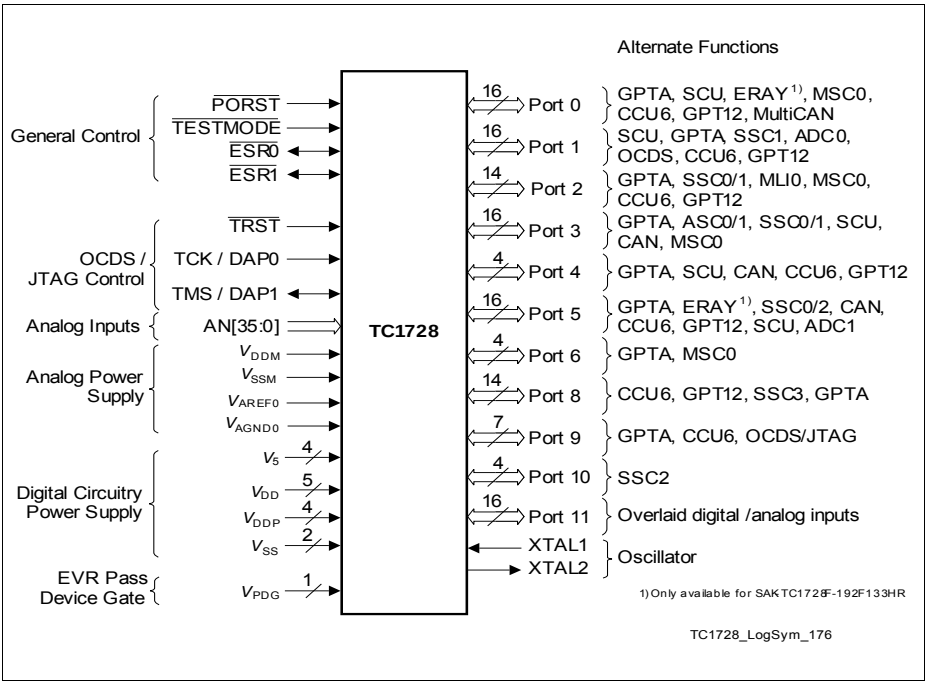

Figure 3-1 TC1728 Logic Symbol

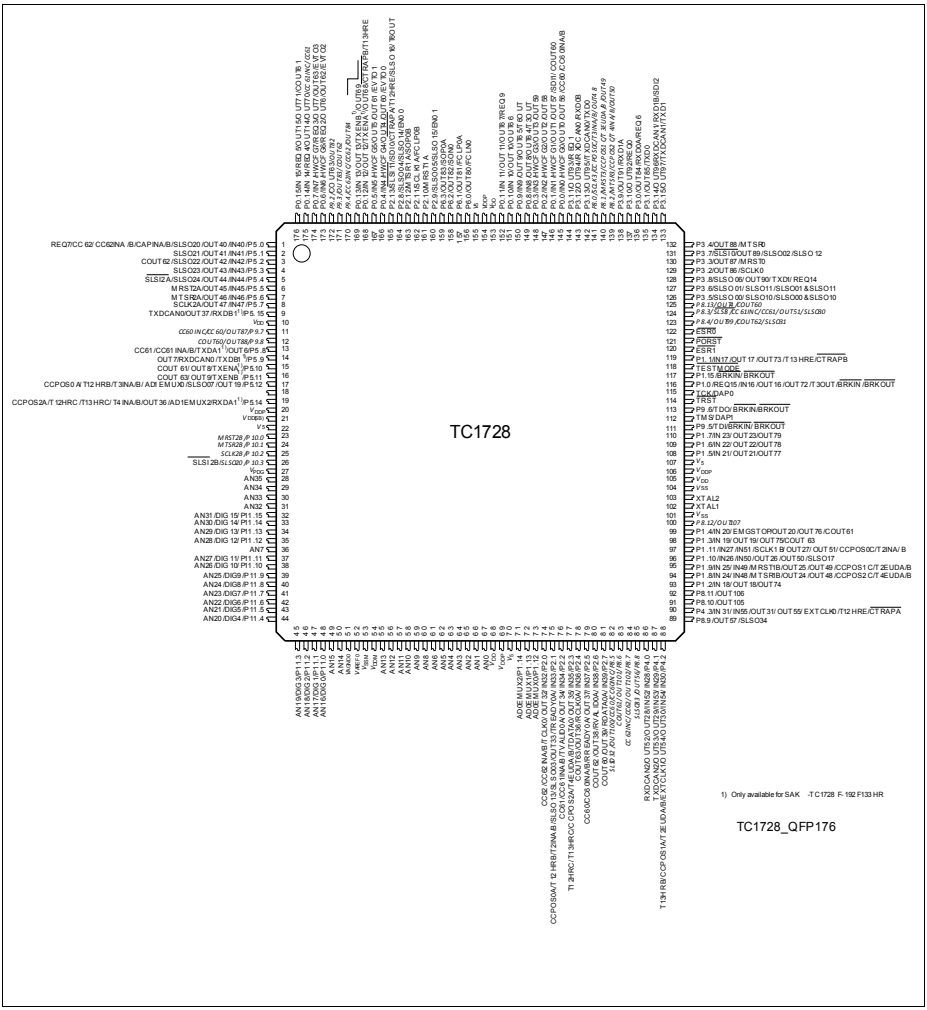

Figure 3-2 SAK-TC1728N-192F133HL / SAK-TC1728N-192F133HR / SAK-TC1728F-192F133HR Pinning

Table 3-1 Pin Definitions and Functions (PG-LQFP-176-6 **Package**)

Pin	Symbol	Ctrl.	Type	Function
Port 0				

Table 3-1 Pin Definitions and Functions (PG-LQFP-176-6 **Package**) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
149	P0.8	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 8**
	IN8	I		**GPTA0 Input 8**
	OUT8	O1		**GPTA0 Output 8**
	OUT64	O2		**GPTA0 Output 64**
	GPT121	O3		**T3OUT**
150	P0.9	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 9**
	IN9	I		**GPTA0 Input 9**
	OUT9	O1		**GPTA0 Output 9**
	OUT65	O2		**GPTA0 Output 65**
	GPT121	O3		**T6OUT**
151	P0.10	I/O0	A2/ PU	**Port 0 General Purpose I/O Line 10**
	IN10	I		**GPTA0 Input 10**
	OUT10	O1		**GPTA0 Output 10**
	OUT66	O2		**GPTA0 Output 66**
	Reserved	O3		**-**
152	P0.11	I/O0	A2/ PU	**Port 0 General Purpose I/O Line 11**
	IN11	I		**GPTA0 Input 11**
	REQ9	I		**External Request Input 9**
	OUT11	O1		**GPTA0 Output 11**
	OUT67	O2		**GPTA0 Output 67**
	Reserved	O3		**-**
168	P0.12	I/O0	A2/ PU	**Port 0 General Purpose I/O Line 12**
	IN12	I		**GPTA0 Input 12**
	CCU60	I		**$\overline{\text{CTRAPB}}$**
	CCU61	I		**T13HRE**
	OUT12	O1		**GPTA0 Output 12**
	OUT68	O2		**GPTA0 Output 68**
	TXENA	O3		**E-Ray Channel A transmit Data Output enable**[1)]

Table 3-1 Pin Definitions and Functions (PG-LQFP-176-6 **Package**) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
169	P0.13	I/O0	A2/ PU	**Port 0 General Purpose I/O Line 13**
	IN13	I		**GPTA0 Input 13**
	OUT13	O1		**GPTA0 Output 13**
	OUT69	O2		**GPTA0 Output 69**
	TXENB	O3		**E-Ray Channel B transmit Data Output enable**[1)]
175	P0.14	I/O0	A1+/ PU	**Port 0 General Purpose I/O Line 14**
	IN14	I		**GPTA0 Input 14**
	REQ4	I		**External Request Input 4**
	CCU61	I		**CC61INC**
	OUT14	O1		**GPTA0 Output 14**
	OUT70	O2		**GPTA0 Output 70**
	CCU60	O3		**CC61**
176	P0.15	I/O0	A1+/ PU	**Port 0 General Purpose I/O Line 15**
	IN15	I		**GPTA0 Input 15**
	REQ5	I		**External Request Input 5**
	OUT15	O1		**GPTA0 Output 15**
	OUT71	O2		**GPTA0 Output 71**
	CCU60	O3		**COUT61**
Port 1				
116	P1.0	I/O0	A2/ PU	**Port 1 General Purpose I/O Line 0**
	REQ15	I		**External Request Input 15**
	IN16	I		**GPTA0 Input 16**
	$\overline{\text{BRKIN}}$	I		**Break Input**
	OUT16	O1		**GPTA0 Output 16**
	OUT72	O2		**GPTA0 Output 72**
	GPT120	O3		**T3OUT**
	$\overline{\text{BRKOUT}}$	O		**Break Output (controlled by OCDS module)**

Table 3-1 Pin Definitions and Functions (PG-LQFP-176-6 **Package**) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
117	P1.15	I/O0	A2/ PU	**Port 1 General Purpose I/O Line 15**
	$\overline{\text{BRKIN}}$	I		**Break Input**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	$\overline{\text{BRKOUT}}$	O		**Break Output (controlled by OCDS module)**
Port 2				
74	P2.0	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 0**
	IN32	I		**GPTA0 Input 32**
	CCU60	I		**CC62INB**
	CCU61	I		**CC62INA**
	OUT32	O1		**GPTA0 Output 32**
	TCLK0	O2		**MLI0 Transmitter Clock Output 0**
	CCU61	O3		**CC62**
75	P2.1	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 1**
	IN33	I		**GPTA0 Input 33**
	TREADY0A	I		**MLI0 Transmitter Ready Input A**
	CCU61	I		**CCPOS0A**
	CCU60	I		**T12HRB**
	GPT120	I		**T2INA**
	GPT121	I		**T2INB**
	OUT33	O1		**GPTA0 Output 33**
	SLSO03	O2		**SSC0 Slave Select Output Line 3**
	SLSO13	O3		**SSC1 Slave Select Output Line 3**

Table 3-1 Pin Definitions and Functions (PG-LQFP-176-6 **Package**) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
2	P5.1	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 1**
	IN41	I		**GPTA0 Input 41**
	OUT41	O1		**GPTA0 Output 41**
	Reserved	O2		**-**
	SLSO21	O3		**SSC2 Slave Select Output 1**
3	P5.2	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 2**
	IN42	I		**GPTA0 Input 42**
	OUT42	O1		**GPTA0 Output 42**
	CCU60	O2		**COUT62**
	SLSO22	O3		**SSC2 Slave Select Output 2**
4	P5.3	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 3**
	IN43	I		**GPTA0 Input 43**
	OUT43	O1		**GPTA0 Output 43**
	Reserved	O2		**-**
	SLSO23	O3		**SSC2 Slave Select Output 3**
5	P5.4	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 4**
	IN44	I		**GPTA0 Input 44**
	SLSI2A	I		**SSC2 Slave Select Input A**
	OUT44	O1		**GPTA0 Output 44**
	Reserved	O2		**-**
	SLSO24	O3		**SSC2 Slave Select Output 4**
6	P5.5	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 5**
	IN45	I		**GPTA0 Input 45**
	MRST2A	I		**SSC2 Master Receive Input A (Master Mode)**
	OUT45	O1		**GPTA0 Output 45**
	Reserved	O2		**-**
	MRST2	O3		**SSC2 Slave Transmit Output (Slave Mode)**

Table 3-1 Pin Definitions and Functions (PG-LQFP-176-6 **Package**) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
34	P11.13	I	D / S	**Port 11 General Purpose I/O Line 13**[2]
	Dig13	I		**Digital Input 13**
	AN29	I		**Analog Input : ADC1.CH13** [3]
33	P11.14	I	D / S	**Port 11 General Purpose I/O Line 14**[2]
	Dig14	I		**Digital Input 14**
	AN30	I		**Analog Input : ADC1.CH14** [3]
32	P11.15	I	D / S	**Port 11 General Purpose I/O Line 15**[2]
	Dig15	I		**Digital Input 15**
	AN31	I		**Analog Input : ADC1.CH15** [3]
Analog Input Port				
67	AN0	I	D	**Analog Input 0: ADC0.CH0** [3]
66	AN1	I	D	**Analog Input 1: ADC0.CH1** [3]
65	AN2	I	D	**Analog Input 2: ADC0.CH2** [3]
64	AN3	I	D	**Analog Input 3: ADC0.CH3** [3]
63	AN4	I	D	**Analog Input 4: ADC0.CH4** [3]
62	AN5	I	D	**Analog Input 5: ADC0.CH5** [3]
61	AN6	I	D	**Analog Input 6: ADC0.CH6** [3]
36	AN7	I	D	**Analog Input 7: ADC0.CH7** [3]
60	AN8	I	D	**Analog Input 8: ADC0.CH8** [3]
59	AN9	I	D	**Analog Input 9: ADC0.CH9** [3]
58	AN10	I	D	**Analog Input 10: ADC0.CH10** [3]
57	AN11	I	D	**Analog Input 11: ADC0.CH11** [3]
56	AN12	I	D	**Analog Input 12: ADC0.CH12** [3]
55	AN13	I	D	**Analog Input 13: ADC0.CH13** [3]
50	AN14	I	D	**Analog Input 14: ADC0.CH14** [3]
49	AN15	I	D	**Analog Input 15: ADC0.CH15** [3]
48	AN16	I	D / S	**Analog Input 16: ADC1.CH0, Dig0** [3]
47	AN17	I	D / S	**Analog Input 17: ADC1.CH1, Dig1** [3]
46	AN18	I	D / S	**Analog Input 18: ADC1.CH2, Dig2** [3]
45	AN19	I	D / S	**Analog Input 19: ADC1.CH3, Dig3** [3]

Table 3-1 Pin Definitions and Functions (PG-LQFP-176-6 **Package**) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
44	AN20	I	D / S	**Analog Input 20: ADC1.CH4, Dig4** [3]
43	AN21	I	D / S	**Analog Input 21: ADC1.CH5, Dig5** [3]
42	AN22	I	D / S	**Analog Input 22: ADC1.CH6, Dig6** [3]
41	AN23	I	D / S	**Analog Input 23: ADC1.CH7, Dig7** [3]
40	AN24	I	D / S	**Analog Input 24: ADC1.CH8, Dig8** [3]
39	AN25	I	D / S	**Analog Input 25: ADC1.CH9, Dig9** [3]
38	AN26	I	D / S	**Analog Input 26: ADC1.CH10, Dig10** [3]
37	AN27	I	D / S	**Analog Input 27: ADC1.CH11, Dig11** [3]
35	AN28	I	D / S	**Analog Input 28: ADC1.CH12, Dig12** [3]
34	AN29	I	D / S	**Analog Input 29: ADC1.CH13, Dig13** [3]
33	AN30	I	D / S	**Analog Input 30: ADC1.CH14, Dig14** [3]
32	AN31	I	D / S	**Analog Input 31: ADC1.CH15, Dig15** [3]
31	AN32	I	D	**Analog Input 32: FADC_FADIN0P** [4]
30	AN33	I	D	**Analog Input 33: FADC_FADIN0N** [4]
29	AN34	I	D	**Analog Input 34: FADC_FADIN1P** [4]
28	AN35	I	D	**Analog Input 35: FADC_FADIN1N** [4]
54	V_{DDM}	-	-	**ADC Analog Part Power Supply (3.3V - 5V)**
53	V_{SSM}	-	-	**ADC Analog Part Ground**
52	V_{AREF0}	-	-	**ADC0 and ADC1 Reference Voltage**
51	V_{AGND0}	-	-	**ADC Reference Ground**
10, 21[5], 68, 105, 153	V_{DD}	-	-	**Digital Core Power Supply (1.3V)**
20, 69, 106, 154	V_{DDP}	-	-	**Port Power Supply (3.3V)**

5.1.4 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 8 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time (24000 h) is not exceeded
- **Operating Conditions** are met for
  - pad supply levels (V_{DDP} or V_{DDM})
  - temperature

If a pin current is out of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Table 8 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any digital pin during overload condition except LVDS pins	I_{IN}	-5	–	+5	mA	
Input current on LVDS pins	I_{INLVDS}	-3	–	+3	mA	
Absolute sum of all input circuit currents for one port group during overload condition[1)]	I_{ING}	-70	–	+70	mA	
Input current on analog pins	I_{INANA}	-3	–	+3	mA	
Absolute sum of all analog input currents for analog inputs of a single ADC during overload condition	I_{INSAS}	-15	–	+15	mA	
Absolute sum of all input circuit currents during overload condition	ΣI_{INS}	-100	–	100	mA	

1) The port groups are defined in **Table 12**.

Note: FADC input pins count as analog pin as they are overlayed with an ADC pins.

Table 11 Operating Conditions Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Junction temperature	T_J	SR	-40	–	160	°C	
Core Supply Voltage	V_{DD}	SR	1.17	1.3	1.43[2]	V	Only required if externally supplied[5]
ADC analog supply voltage	V_{DDM}	SR	2.97	5.0	5.5[3]	V	
EVR supply voltage	V_5	SR	4.00	5.0	5.5	V	5.0V single supply
			2.97	3.3	3.63	V	3.3V single supply
Digital supply voltage for IO pads	V_{DDP}	SR	2.97	3.3	3.63[4]	V	Only required if externally supplied[5]
VDDP voltage to ensure defined pad states[6]	V_{DDPPA}	CC	0.65	–	–	V	
Digital ground voltage	V_{SS}	SR	0	–	–	V	
Analog ground voltage for V_{DDM}	V_{SSM}	SR	-0.1	0	0.1	V	

1) Applicable for digital outputs.

2) Voltage overshoot to 1.7V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

3) Voltage overshoot to 6.5V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

4) Voltage overshoot to 4.0V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

5) No external inductive load permissable if EVR is used.

6) This parameter is valid under the assumption the $\overline{\text{PORST}}$ signal is constantly at low level during the power-up/power-down of V_{DDP}.

Table 12 Pin Groups for Overload / Short-Circuit Current Sum Parameter

Group	Pins
1	P0.15, P5.[7:0], P5.[15:8], P9.[8:7], P10.[3:0]
2	P0.[14:0], P2.[13:8], P3.[1:0], P3.[4:3], P3.7, P3.[15:9], P6.[3:0], P8.[2:0], P9.[4:2]

Table 15 Standard_Pads Class_A1+

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of the class A1+ pad, weak driver	$R_{DSONWCC}$	–	450	600	Ohm	I_{OH}> -0.5 mA; P_MOS
		–	210	340	Ohm	I_{OL}< 0.5 mA; N_MOS
On-Resistance of the class A1+ pad, medium driver	$R_{DSONMCC}$	–	–	155	Ohm	I_{OH}> -2 mA; P_MOS
		–	–	110	Ohm	I_{OL}< 2 mA; N_MOS
On-Resistance of the class A1+ pad, strong driver	$R_{DSON1+CC}$	–	–	110	Ohm	I_{OH}> -2 mA; P_MOS
		–	–	80	Ohm	I_{OL}< 2 mA; N_MOS
Fall time, pad type A1+	$t_{FA1+CCC}$	–	–	150	ns	C_L= 20 pF; pin out driver= weak
		–	–	28	ns	C_L= 50 pF; edge= slow; pin out driver= strong
		–	–	16	ns	C_L= 50 pF; edge= soft ; pin out driver= strong
		–	–	50	ns	C_L= 50 pF; pin out driver= medium
		–	–	140	ns	C_L= 150 pF; pin out driver= medium
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak

5.3.2 Power Sequencing 5V Supply Only

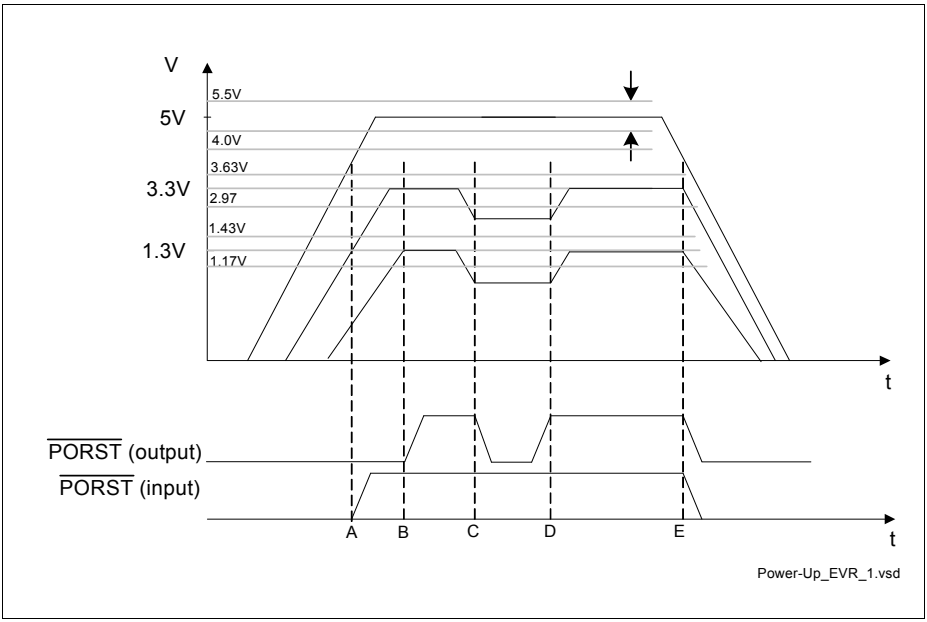

Figure 9 5 V / 3.3 V / 1.3 V Power-Up/Down Sequence

The events for the above points in the power-up/down sequence

- A :external supplied voltage reaches operating level
- B: external supplied and internal generated voltages reaches operating levels
- C: internal generated voltage drops below operating level
- D: internal generated voltage resumes operating level
- E: external supplied voltage leaves operating level

P0.4 and P0.5 should be kept at the selected setting of '0' or '1' until external supplied voltage has reached its operating level.

The following list of rules applies to the power-up/down sequence:

- All ground pins V_{SS} must be externally connected to one single star point in the system. Regarding the DC current component, all ground pins are internally directly connected.
- The latch-up risk is minimized if the I/O currents are limited to:
  - 20 mA for one pin group
  - AND 100 mA for the completed device I/Os

5.3.4 Power Sequencing all Voltages supplied from External

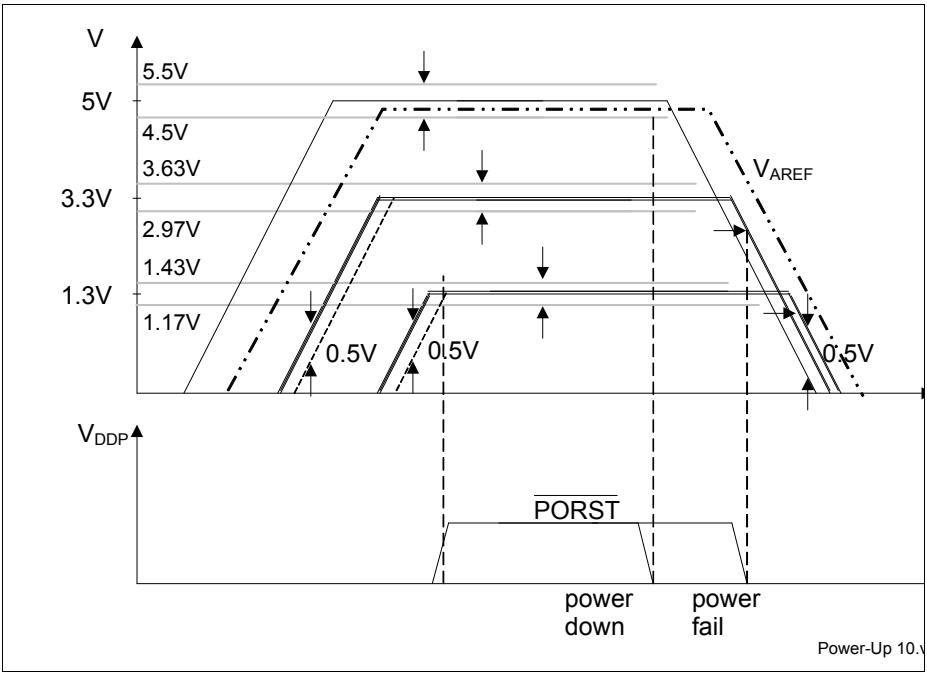

Figure 11 5 V / 3.3 V / 1.3 V Power-Up/Down Sequence

P0.4 and P0.5 should be kept at the selected setting until external supplied voltage has reached its operating level.

The following list of rules applies to the power-up/down sequence:

- All ground pins V_{SS} must be externally connected to one single star point in the system. Regarding the DC current component, all ground pins are internally directly connected.
- At any moment in time to avoid increased latch-up risk,
  each power supply must be higher then any lower_power_supply - 0.5 V, or:
  VDD5 > VDDP - 0.5 V; VDD5 > VDD - 0.5 V;VDDP > VDD - 0.5 V, see **Figure 11**.
  – The latch-up risk is minimized if the I/O currents are limited to:
  – 20 mA for one pin group
  – AND 100 mA for the completed device I/Os
  – AND additionally before power-up / after power-down:
  1 mA for one pin in inactive mode (0 V on all power supplies)

5.3.9 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 32 JTAG Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	25	–	–	ns	
TCK high time	t_2 SR	10	–	–	ns	
TCK low time	t_3 SR	10	–	–	ns	
TCK clock rise time	t_4 SR	–	–	4	ns	
TCK clock fall time	t_5 SR	–	–	4	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6.0	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6.0	–	–	ns	
TDO valid after TCK falling edge[1]	t_8 CC	3.0	–	–	ns	C_L= 20 pF
		–	–	13	ns	C_L=50 pF
TDO high impedance to valid from TCK falling edge[2]	t_9 CC	–	–	14	ns	C_L= 50 pF
TDO valid output to high impedance from TCK falling edge	t_{10} CC	–	–	13.5	ns	C_L= 50 pF
TDO hold after TCK falling edge	t_{18} CC	2	–	–	ns	

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

5.3.10 DAP Interface Timing

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 33 DAP Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period[1]	t_{TCK} SR	12.5	–	–	ns	
DAP0 high time	t_{12} SR	4	–	–	ns	
DAP0 low time[1]	t_{13} SR	4	–	–	ns	
DAP0 clock rise time	t_{14} SR	–	–	2	ns	
DAP0 clock fall time	t_{15} SR	–	–	2	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	6.0	–	–	ns	
DAP1 hold after DAP0 rising edge	t_{17} SR	6.0	–	–	ns	
DAP1 valid per DAP0 clock period[2]	t_{19} CC	8	–	–	ns	C_L= 20 pF; f= 80 MHz
		10	–	–	ns	C_L= 50 pF; f= 40 MHz

1) See the DAP chapter for clock rate restrictions in the Active::IDLE protocol state.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

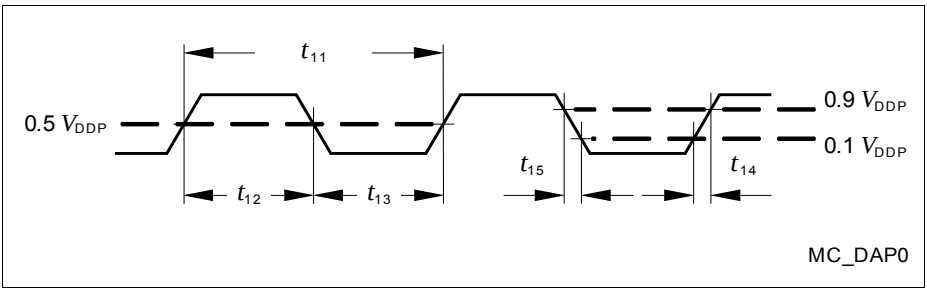

Figure 15 Test Clock Timing (DAP0)

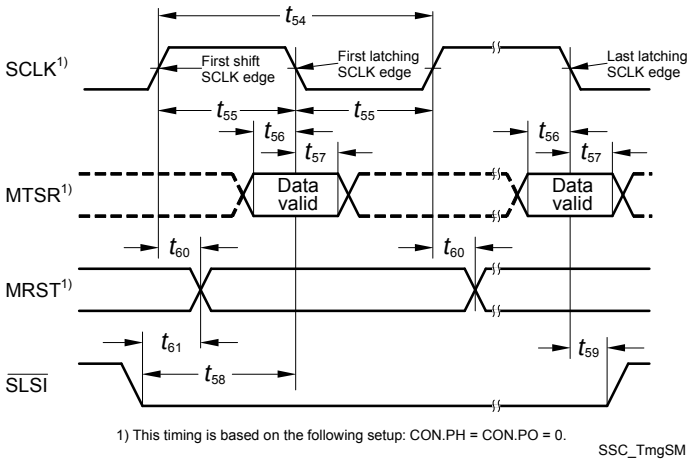

Figure 21 Slave Mode Timing

6 Revision History

Changes from V0.3 to V0.4D1

- Operating Conditions
  - Added footnote 3 and 4
  - Updated K_{OVAN} and K_{OVAP} max values
  - Added f_{CPU}, f_{LMB}, f_{PCP}, f_{FPI}max for SAK-TC1724F-192F133HL, SAK-TC1724F-192F133HR, SAK-TC1724N-192F80HR, SAK-TC1724N-128F80HR.
  - Updated limits for $V_{DD,}$ $V_{DDM,}$ V_{DDP}.
  - Added $I_{IN,}$ ΣI_{IN}
  - Updated ΣI_{SC_PG}
- Standard Pad Class A1
  - Changed R_{DSON1} *to* R_{DSONM}, added new condition “PMOS” for 140ohms, added a new condition for “NMOS” with a max value of 100ohms
  - Added R_{DSONW}
  - Changed min value of V_{IHA1} to 0.6 x V_{DDP}
  - Changed min value of V_{ILA1} / V_{IHA1} to 0.6
- Standard Pad Class A1+
  - Added HYSA1+
  - Added V_{ILA1+} / V_{IHA1+}
  - Added R_{DSONW}, R_{DSONM}
  - R_{DSON1+}, added new condition “PMOS” for 85ohms, added a new condition for “NMOS” with a max value of 70ohms
  - Changed min value of V_{IHA1+} to 0.6 x V_{DDP}
  - Deleted -2000nA to 2000nA limits for I_{OZA1+}
- Standard Pad Class A2
  - Added HYSA2
  - Added R_{DSONW}, R_{DSONM}
  - R_{DSON2}, added new condition “PMOS” for 25ohms, added a new condition for “NMOS” with a max value of 20ohms
  - t_{FA2}, added max 18000ns for CL=20000pF; pinout driver=medium, 65000ns for CL=20000pF;pinout driver=weak
  - t_{RA2}, removed 140ns for CL=150pF;pinout driver=weak
  - t_{RA2}, added 550ns for CL=150pF,pinout driver=weak, 18000ns for CL=20000pF, pinout driver=medium, 65000ns for CL=20000pF, pinoutdriver=weak
- Standard Pad Class F
  - Added HYSF
  - Changed min value of VIHF to 0.6 x VDDP
  - Added min value of V_{ILF} / V_{IHF} as 0.6
  - Added R_{DSONW}, R_{DSONM}
  - Deleted note for t_{FF}, t_{RF}
- Standard Pad Class I
  - Changed min value of V_{IHI} to 0.6 x V_{DDP}

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG