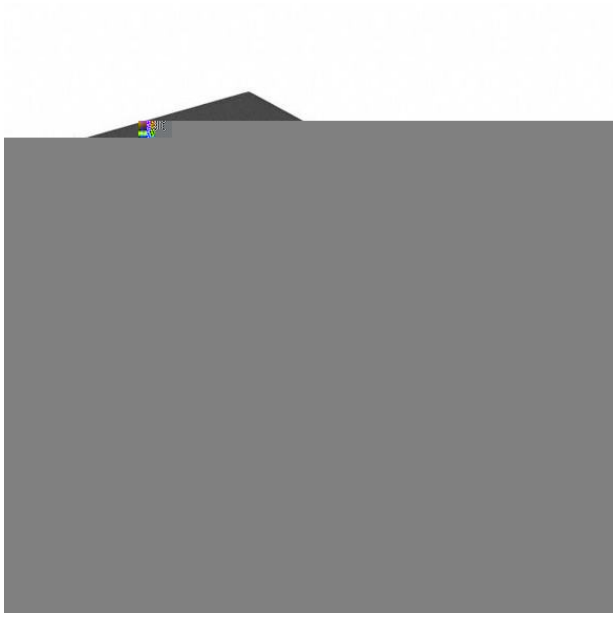


**Welcome to E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

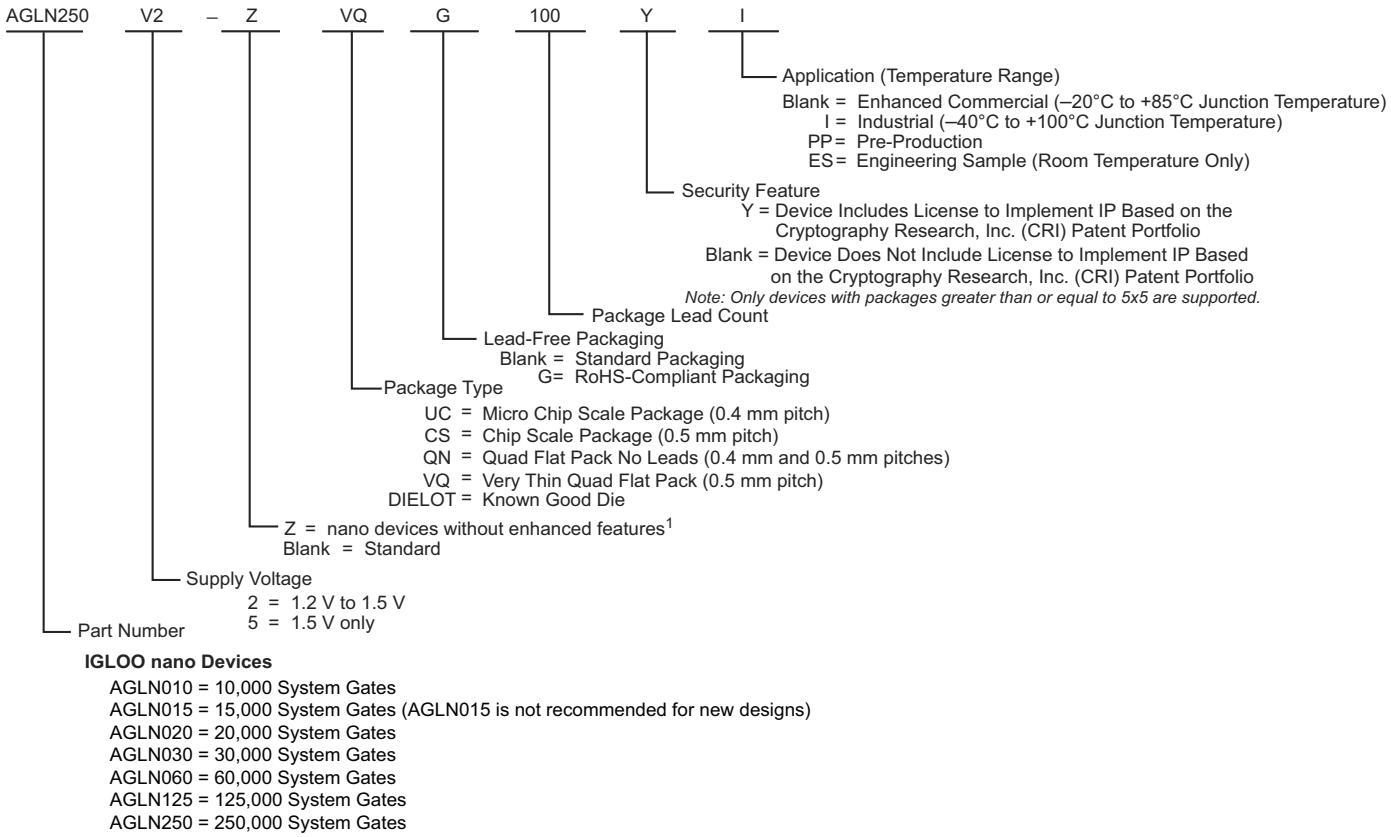
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 520 |
| Total RAM Bits | - |
| Number of I/O | 52 |
| Number of Gates | 20000 |
| Voltage - Supply | 1.14V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 81-WFBGA, CSBGA |
| Supplier Device Package | 81-UCSP (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/agln020v2-ucg81i |

# IGLOO nano Ordering Information




**IGLOO nano Devices**

AGLN010 = 10,000 System Gates
AGLN015 = 15,000 System Gates (AGLN015 is not recommended for new designs)
AGLN020 = 20,000 System Gates
AGLN030 = 30,000 System Gates
AGLN060 = 60,000 System Gates
AGLN125 = 125,000 System Gates
AGLN250 = 250,000 System Gates

*Notes:*

1. *Z-feature grade devices AGLN060Z, AGLN125Z, and AGLN250Z do not support the enhanced nano features of Schmitt Trigger input, bus hold (hold previous I/O state in Flash*Freeze mode), cold-sparing, hot-swap I/O capability and 1.2 V programming. The AGLN030 Z feature grade does not support Schmitt trigger input, bus hold and 1.2 V programming. For the VQ100, CS81, UC81, QN68, and QN48 packages, the Z feature grade and the N part number are not marked on the device. Z feature grade devices are not recommended for new designs.*
2. *AGLN030 is available in the Z feature grade only.*
3. *Marking Information: IGLOO nano V2 devices do not have a V2 marking, but IGLOO nano V5 devices are marked with a V5 designator.*

# Devices Not Recommended For New Designs

AGLN015, AGLN030Z, AGLN060Z, AGLN125Z, and AGLN250Z are not recommended for new designs. For more information on obsoleted devices/packages, refer to the *PDN1503 - IGLOO nano Z and ProASIC3 nano Z Families*.

# 1 – IGLOO nano Device Overview

## General Description

The IGLOO family of flash FPGAs, based on a 130-nm flash process, offers the lowest power FPGA, a single-chip solution, small footprint packages, reprogrammability, and an abundance of advanced features.

The Flash*Freeze technology used in IGLOO nano devices enables entering and exiting an ultra-low power mode that consumes nanoPower while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low power consumption while the IGLOO nano device is completely functional in the system. This allows the IGLOO nano device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOO nano devices the advantage of being a secure, low power, single-chip solution that is Instant On. The IGLOO nano device is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOO nano devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). The AGLN030 and smaller devices have no PLL or RAM support. IGLOO nano devices have up to 250 k system gates, supported with up to 36 kbits of true dual-port SRAM and up to 71 user I/Os.

IGLOO nano devices increase the breadth of the IGLOO product line by adding new features and packages for greater customer value in high volume consumer, portable, and battery-backed markets. Features such as smaller footprint packages designed with two-layer PCBs in mind, power consumption measured in nanoPower, Schmitt trigger, and bus hold (hold previous I/O state in Flash*Freeze mode) functionality make these devices ideal for deployment in applications that require high levels of flexibility and low cost.

### Flash*Freeze Technology

The IGLOO nano device offers unique Flash*Freeze technology, allowing the device to enter and exit ultra-low power Flash*Freeze mode. IGLOO nano devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOO nano V2 devices to support a wide range of core voltage (1.2 V to 1.5 V) allows further reduction in power consumption, thus achieving the lowest total system power.

During Flash*Freeze mode, each I/O can be set to the following configurations: hold previous state, tristate, HIGH, or LOW.

The availability of low power modes, combined with reprogrammability, a single-chip and single-voltage solution, and small-footprint packages make IGLOO nano devices the best fit for portable electronics.

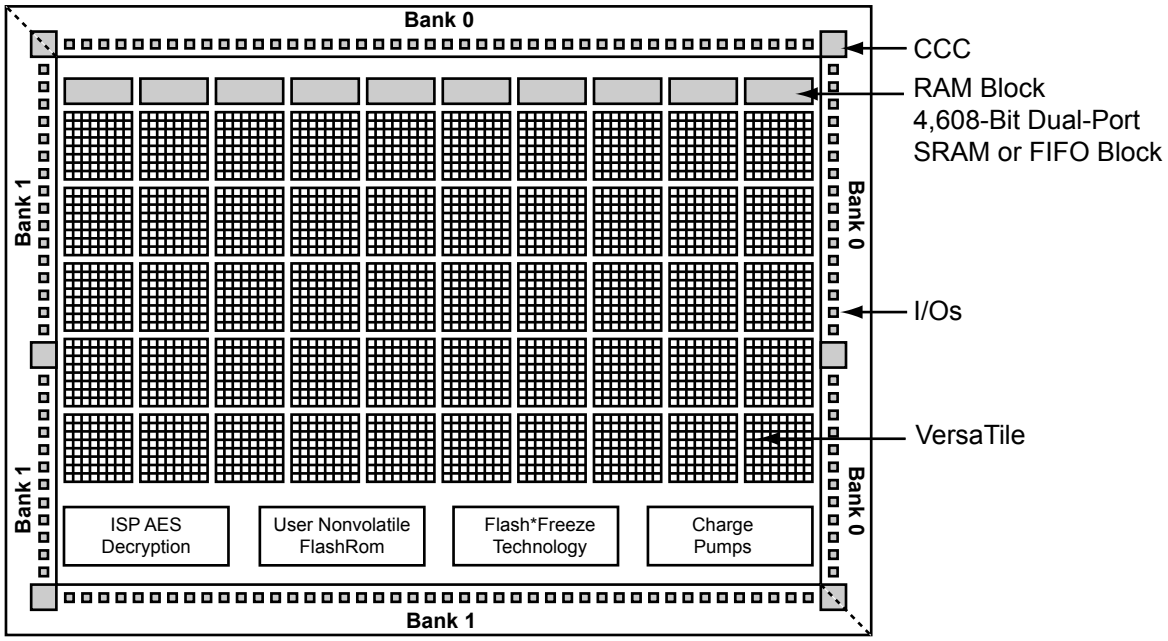



***Figure 1-3 •*** **IGLOO Device Architecture Overview with Two I/O Banks (AGLN060, AGLN125)**

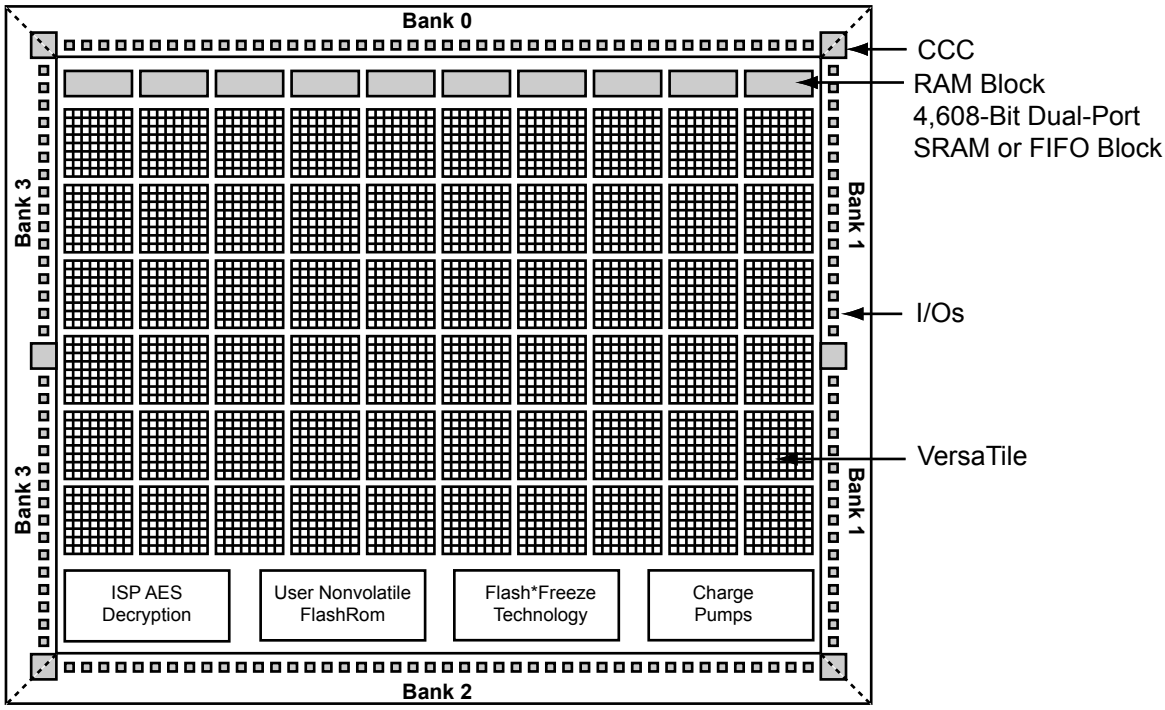



***Figure 1-4 •*** **IGLOO Device Architecture Overview with Four I/O Banks (AGLN250)**

***Table 2-2 •*** **Recommended Operating Conditions [1]**

| Symbol | Parameter | | Extended Commercial | Industrial | Units |
|---|---|---|---|---|---|
| $T_J$ | Junction temperature | | –20 to + 85[2] | –40 to +100[2] | °C |
| VCC | 1.5 V DC core supply voltage[3] | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | 1.2 V–1.5 V wide range core voltage[4,5] | | 1.14 to 1.575 | 1.14 to 1.575 | V |
| VJTAG | JTAG DC voltage | | 1.4 to 3.6 | 1.4 to 3.6 | V |
| VPUMP [6] | Programming voltage | Programming mode | 3.15 to 3.45 | 3.15 to 3.45 | V |
| | | Operation | 0 to 3.6 | 0 to 3.6 | V |
| VCCPLL[7] | Analog power supply (PLL) | 1.5 V DC core supply voltage[3] | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | | 1.2 V–1.5 V wide range core supply voltage[4] | 1.14 to 1.575 | 1.14 to 1.575 | V |
| VCCI and VMV [8,9] | 1.2 V DC supply voltage [4] | | 1.14 to 1.26 | 1.14 to 1.26 | V |
| | 1.2 V DC wide range supply voltage [4] | | 1.14 to 1.575 | 1.14 to 1.575 | V |
| | 1.5 V DC supply voltage | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | 1.8 V DC supply voltage | | 1.7 to 1.9 | 1.7 to 1.9 | V |
| | 2.5 V DC supply voltage | | 2.3 to 2.7 | 2.3 to 2.7 | V |
| | 3.3 V DC supply voltage | | 3.0 to 3.6 | 3.0 to 3.6 | V |
| | 3.3 V DC wide range supply voltage [10] | | 2.7 to 3.6 | 2.7 to 3.6 | V |

*Notes:*

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the Libero Online Help.*
3. *For IGLOO® nano V5 devices*
4. *For IGLOO nano V2 devices only, operating at VCCI ≥ VCC*
5. *IGLOO nano V5 devices can be programmed with the VCC core voltage at 1.5 V only. IGLOO nano V2 devices can be programmed with the VCC core voltage at 1.2 V (with FlashPro4 only) or 1.5 V. If you are using FlashPro3 and want to do in-system programming using 1.2 V, please contact the factory.*
6. *$V_{PUMP}$ can be left floating during operation (not programming mode).*
7. *VCCPLL pins should be tied to VCC pins. See the "Pin Descriptions" chapter for further information.*
8. *VMV pins must be connected to the corresponding VCCI pins. See the Pin Descriptions chapter of the IGLOO nano FPGA Fabric User's Guide for further information.*
9. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-21 on page 2-19. VCCI should be at the same voltage within a given I/O bank.*
10. *3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.*

***Table 2-3 •*** **Flash Programming Limits – Retention, Storage, and Operating Temperature[1]**

| Product Grade | Programming Cycles | Program Retention (biased/unbiased) | Maximum Storage Temperature $T_{STG}$ (°C) [2] | Maximum Operating Junction Temperature $T_J$ (°C) [2] |
|---|---|---|---|---|
| Commercial | 500 | 20 years | 110 | 100 |
| Industrial | 500 | 20 years | 110 | 100 |

*Notes:*

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

## Power per I/O Pin

***Table 2-13 •*** **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to IGLOO nano I/O Banks**

| | VCCI (V) | Dynamic Power PAC9 (µW/MHz) [1] |
|---|---|---|
| **Single-Ended** | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 3.3 | 16.38 |
| 3.3 V LVTTL / 3.3 V LVCMOS – Schmitt Trigger | 3.3 | 18.89 |
| 3.3 V LVCMOS Wide Range[2] | 3.3 | 16.38 |
| 3.3 V LVCMOS Wide Range – Schmitt Trigger | 3.3 | 18.89 |
| 2.5 V LVCMOS | 2.5 | 4.71 |
| 2.5 V LVCMOS – Schmitt Trigger | 2.5 | 6.13 |
| 1.8 V LVCMOS | 1.8 | 1.64 |
| 1.8 V LVCMOS – Schmitt Trigger | 1.8 | 1.79 |
| 1.5 V LVCMOS (JESD8-11) | 1.5 | 0.97 |
| 1.5 V LVCMOS (JESD8-11) – Schmitt Trigger | 1.5 | 0.96 |
| 1.2 V LVCMOS[3] | 1.2 | 0.57 |
| 1.2 V LVCMOS – Schmitt Trigger[3] | 1.2 | 0.52 |
| 1.2 V LVCMOS Wide Range[3] | 1.2 | 0.57 |
| 1.2 V LVCMOS Wide Range – Schmitt Trigger[3] | 1.2 | 0.52 |

*Notes:*

1. *PAC9 is the total dynamic power measured on $V_{CCI}$.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
3. *Applicable to IGLOO nano V2 devices operating at VCCI ≥ VCC.*

***Table 2-14 •*** **Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] Applicable to IGLOO nano I/O Banks**

| | $C_{LOAD}$ (pF) | VCCI (V) | Dynamic Power PAC10 (µW/MHz)[2] |
|---|---|---|---|
| **Single-Ended** | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 5 | 3.3 | 107.98 |
| 3.3 V LVCMOS Wide Range[3] | 5 | 3.3 | 107.98 |
| 2.5 V LVCMOS | 5 | 2.5 | 61.24 |
| 1.8 V LVCMOS | 5 | 1.8 | 31.28 |
| 1.5 V LVCMOS (JESD8-11) | 5 | 1.5 | 21.50 |
| 1.2 V LVCMOS[4] | 5 | 1.2 | 15.22 |

*Notes:*

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PAC10 is the total dynamic power measured on VCCI.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
4. *Applicable for IGLOO nano V2 devices operating at VCCI ≥ VCC.*

### 1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

**Table 2-57 • Minimum and Maximum DC Input and Output Levels**

| 1.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL [1] | IIH [2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA [3] | Max. mA [3] | µA [4] | µA [4] |
| 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 13 | 16 | 10 | 10 |

*Notes:*

1. *$I_{IL}$ is the input leakage current per I/O pin over recommended operating conditions where –0.3 < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

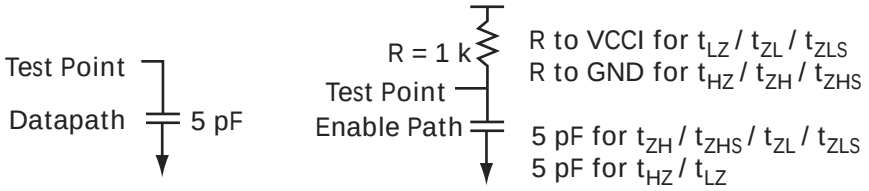



**Figure 2-10 • AC Loading**

**Table 2-58 • 1.5 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads**

| Input LOW (V) | Input HIGH (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 1.5 | 0.75 | 5 |

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.*

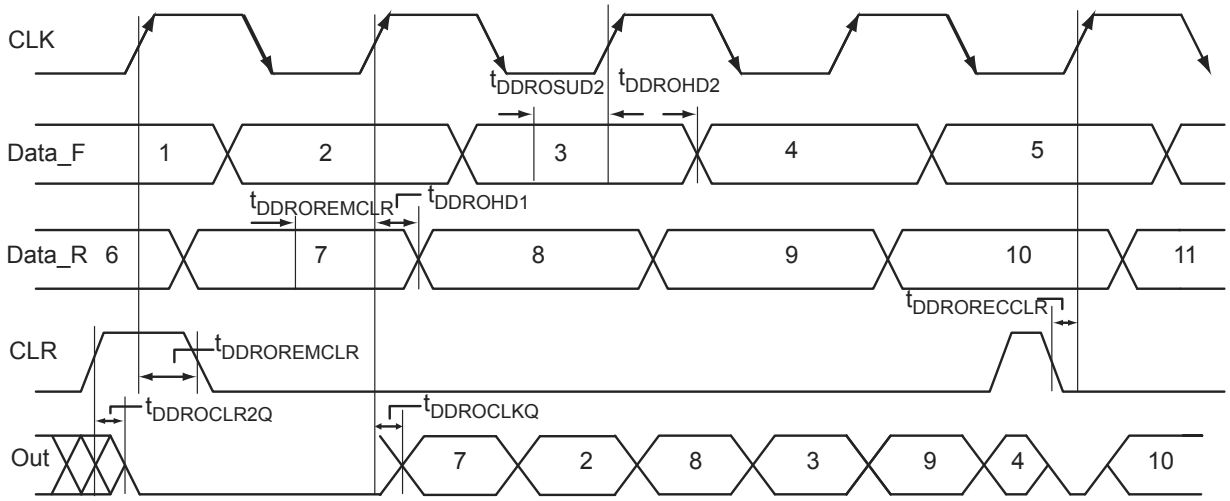



***Figure 2-20 •*** **Output DDR Timing Diagram**

### *Timing Characteristics*

#### *1.5 V DC Core Voltage*

***Table 2-82 •*** **Output DDR Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out of DDR for Output DDR | 1.07 | ns |
| $t_{DDROSUD1}$ | Data_F Data Setup for Output DDR | 0.67 | ns |
| $t_{DDROSUD2}$ | Data_R Data Setup for Output DDR | 0.67 | ns |
| $t_{DDROHD1}$ | Data_F Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROHD2}$ | Data_R Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out for Output DDR | 1.38 | ns |
| $t_{DDROREMCLR}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | ns |
| $t_{DDRORECCLR}$ | Asynchronous Clear Recovery Time for Output DDR | 0.23 | ns |
| $t_{DDROWCLR1}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.19 | ns |
| $t_{DDROCKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output DDR | 0.31 | ns |
| $t_{DDROCKMPWL}$ | Clock Minimum Pulse Width LOW for the Output DDR | 0.28 | ns |
| $F_{DDOMAX}$ | Maximum Frequency for the Output DDR | 250.00 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## VersaTile Specifications as a Sequential Module

The IGLOO nano library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide for Software v10.1*.

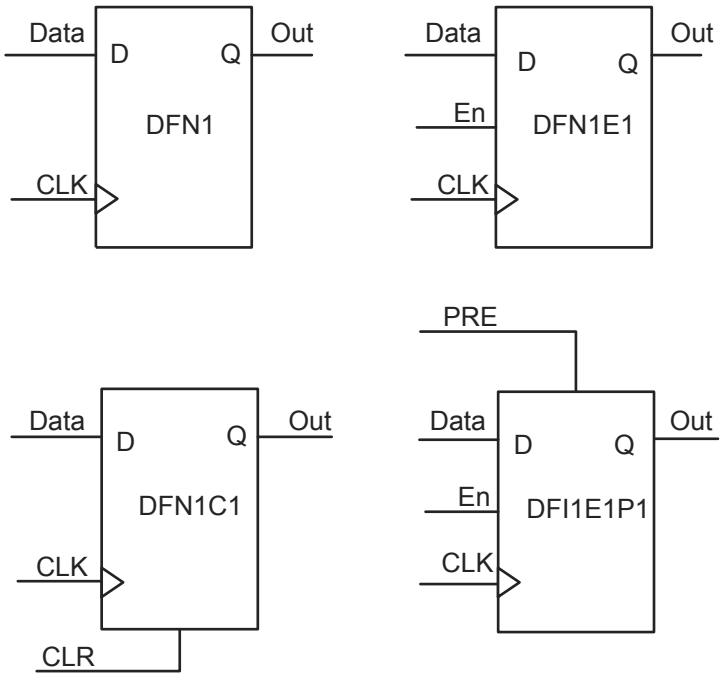



***Figure 2-23 •*** **Sample of Sequential Cells**

# Clock Conditioning Circuits

## CCC Electrical Specifications

### Timing Characteristics

***Table 2-100* • IGLOO nano CCC/PLL Specification**
**For IGLOO nano V2 OR V5 Devices, 1.5 V DC Core Supply Voltage**

| Parameter | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Clock Conditioning Circuitry Input Frequency $f_{IN\_CCC}$ | | 1.5 | | 250 | MHz |
| Clock Conditioning Circuitry Output Frequency $f_{OUT\_CCC}$ | | 0.75 | | 250 | MHz |
| Delay Increments in Programmable Delay Blocks [1, 2] | | | 360[3] | | ps |
| Number of Programmable Values in Each Programmable Delay Block | | | | 32 | |
| Serial Clock (SCLK) for Dynamic PLL [4,9] | | | | 100 | MHz |
| Input Cycle-to-Cycle Jitter (peak magnitude) | | | | 1 | ns |
| Acquisition Time | | | | | |
| | LockControl = 0 | | | 300 | µs |
| | LockControl = 1 | | | 6.0 | ms |
| Tracking Jitter [5] | | | | | |
| | LockControl = 0 | | | 2.5 | ns |
| | LockControl = 1 | | | 1.5 | ns |
| Output Duty Cycle | | 48.5 | | 51.5 | % |
| Delay Range in Block: Programmable Delay 1 [1, 2] | | 1.25 | | 15.65 | ns |
| Delay Range in Block: Programmable Delay 2 [1, 2, | | 0.025 | | 15.65 | ns |
| Delay Range in Block: Fixed Delay [1, 2] | | | 3.5 | | ns |
| VCO Output Peak-to-Peak Period Jitter $F_{CCC\_OUT}$[6] | Max Peak-to-Peak Jitter Data [6,7,8] | | | | |
| | SSO ≤ 2 | SSO ≤ 4 | SSO ≤ 8 | SSO ≤ 16 | |
| 0.75 MHz to 50 MHz | 0.50 | 0.60 | 0.80 | 1.20 | % |
| 50 MHz to 250 MHz | 2.50 | 4.00 | 6.00 | 12.00 | % |

*Notes:*

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for deratings.*
2. *$T_J$ = 25°C, V**CC** = 1.5 V*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
4. *Maximum value obtained for a STD speed grade device in Worst-Case Commercial conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for derating values.*
5. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
6. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT, regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, no matter what the settings are for the output divider.*
7. *Measurements done with LVTTL 3.3 V 8 mA I/O drive strength and high slew rate. VCC/VCCPLL = 1.425 V, VCCI = 3.3 V, VQ/PQ/TQ type of packages, 20 pF load.*
8. *SSOs are outputs that are synchronous to a single clock domain and have their clock-to-out times within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO nano FPGA Fabric User's Guide.*
9. *The AGLN010, AGLN015, and AGLN020 devices do not support PLLs.*

### 1.2 V DC Core Voltage

**Table 2-107 • FIFO**
**Worst Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{ENS}$ | REN, WEN Setup Time | 3.44 | ns |
| $t_{ENH}$ | REN, WEN Hold Time | 0.26 | ns |
| $t_{BKS}$ | BLK Setup Time | 0.30 | ns |
| $t_{BKH}$ | BLK Hold Time | 0.00 | ns |
| $t_{DS}$ | Input Data (DI) Setup Time | 1.30 | ns |
| $t_{DH}$ | Input Data (DI) Hold Time | 0.41 | ns |
| $t_{CKQ1}$ | Clock High to New Data Valid on RD (flow-through) | 5.67 | ns |
| $t_{CKQ2}$ | Clock High to New Data Valid on RD (pipelined) | 3.02 | ns |
| $t_{RCKEF}$ | RCLK High to Empty Flag Valid | 6.02 | ns |
| $t_{WCKFF}$ | WCLK High to Full Flag Valid | 5.71 | ns |
| $t_{CKAF}$ | Clock High to Almost Empty/Full Flag Valid | 22.17 | ns |
| $t_{RSTFG}$ | RESET LOW to Empty/Full Flag Valid | 5.93 | ns |
| $t_{RSTAF}$ | RESET LOW to Almost Empty/Full Flag Valid | 21.94 | ns |
| $t_{RSTBQ}$ | RESET LOW to Data Out Low on RD (flow-through) | 3.41 | ns |
| | RESET LOW to Data Out Low on RD (pipelined) | 4.09 | 3.41 |
| $t_{REMRSTB}$ | RESET Removal | 1.02 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 5.48 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 1.18 | ns |
| $t_{CYC}$ | Clock Cycle Time | 10.90 | ns |
| $F_{MAX}$ | Maximum Frequency for FIFO | 92 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

# Related Documents

## User Guides

*IGLOO nano FPGA Fabric User's Guide*

## Packaging Documents

The following documents provide packaging information and device selection for low power flash devices.

### *Product Catalog*

*FPGA and SoC Product Catalog*

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

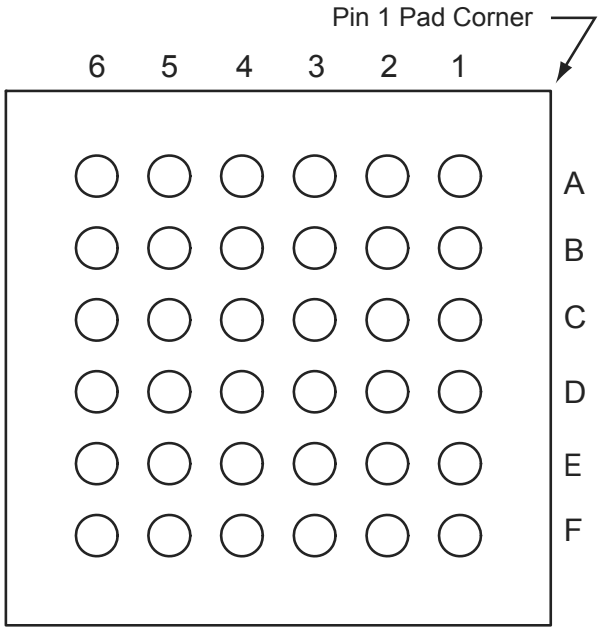
### *Package Mechanical Drawings*

This document contains the package mechanical drawings for all packages currently or previously supplied by Microsemi. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials are on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

# 4 – Package Pin Assignments

## UC36




*Note: This is the bottom view of the package.*

### *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

| UC81 | |
|---|---|
| **Pin Number** | **AGLN020 Function** |
| A1 | IO64RSB2 |
| A2 | IO54RSB2 |
| A3 | IO57RSB2 |
| A4 | IO36RSB1 |
| A5 | IO32RSB1 |
| A6 | IO24RSB1 |
| A7 | IO20RSB1 |
| A8 | IO04RSB0 |
| A9 | IO08RSB0 |
| B1 | IO59RSB2 |
| B2 | IO55RSB2 |
| B3 | IO62RSB2 |
| B4 | IO34RSB1 |
| B5 | IO28RSB1 |
| B6 | IO22RSB1 |
| B7 | IO18RSB1 |
| B8 | IO00RSB0 |
| B9 | IO03RSB0 |
| C1 | IO51RSB2 |
| C2 | IO50RSB2 |
| C3 | NC |
| C4 | NC |
| C5 | NC |
| C6 | NC |
| C7 | NC |
| C8 | IO10RSB0 |
| C9 | IO07RSB0 |
| D1 | IO49RSB2 |
| D2 | IO44RSB2 |
| D3 | NC |
| D4 | VCC |
| D5 | VCCIB2 |
| D6 | GND |
| D7 | NC |
| D8 | IO13RSB0 |
| D9 | IO12RSB0 |

| UC81 | |
|---|---|
| **Pin Number** | **AGLN020 Function** |
| E1 | GEC0/IO48RSB2 |
| E2 | GEA0/IO47RSB2 |
| E3 | NC |
| E4 | VCCIB1 |
| E5 | VCC |
| E6 | VCCIB0 |
| E7 | NC |
| E8 | GDA0/IO15RSB0 |
| E9 | GDC0/IO14RSB0 |
| F1 | IO46RSB2 |
| F2 | IO45RSB2 |
| F3 | NC |
| F4 | GND |
| F5 | VCCIB1 |
| F6 | NC |
| F7 | NC |
| F8 | IO16RSB0 |
| F9 | IO17RSB0 |
| G1 | IO43RSB2 |
| G2 | IO42RSB2 |
| G3 | IO41RSB2 |
| G4 | IO31RSB1 |
| G5 | NC |
| G6 | IO21RSB1 |
| G7 | NC |
| G8 | VJTAG |
| G9 | TRST |
| H1 | IO40RSB2 |
| H2 | FF/IO39RSB1 |
| H3 | IO35RSB1 |
| H4 | IO29RSB1 |
| H5 | IO26RSB1 |
| H6 | IO25RSB1 |
| H7 | IO19RSB1 |
| H8 | TDI |
| H9 | TDO |

| UC81 | |
|---|---|
| **Pin Number** | **AGLN020 Function** |
| J1 | IO38RSB1 |
| J2 | IO37RSB1 |
| J3 | IO33RSB1 |
| J4 | IO30RSB1 |
| J5 | IO27RSB1 |
| J6 | IO23RSB1 |
| J7 | TCK |
| J8 | TMS |
| J9 | VPUMP |

| CS81 | |
|---|---|
| **Pin Number** | **AGLN125 Function** |
| A1 | GAA0/IO00RSB0 |
| A2 | GAA1/IO01RSB0 |
| A3 | GAC0/IO04RSB0 |
| A4 | IO13RSB0 |
| A5 | IO22RSB0 |
| A6 | IO32RSB0 |
| A7 | GBB0/IO37RSB0 |
| A8 | GBA1/IO40RSB0 |
| A9 | GBA2/IO41RSB0 |
| B1 | GAA2/IO132RSB1 |
| B2 | GAB0/IO02RSB0 |
| B3 | GAC1/IO05RSB0 |
| B4 | IO11RSB0 |
| B5 | IO25RSB0 |
| B6 | GBC0/IO35RSB0 |
| B7 | GBB1/IO38RSB0 |
| B8 | IO42RSB0 |
| B9 | GBB2/IO43RSB0 |
| C1 | GAB2/IO130RSB1 |
| C2 | IO131RSB1 |
| C3 | GND |
| C4 | IO15RSB0 |
| C5 | IO28RSB0 |
| C6 | GND |
| C7 | GBA0/IO39RSB0 |
| C8 | GBC2/IO45RSB0 |
| C9 | IO47RSB0 |
| D1 | GAC2/IO128RSB1 |
| D2 | IO129RSB1 |
| D3 | GFA2/IO117RSB1 |
| D4 | VCC |
| D5 | VCCIB0 |
| D6 | GND |
| D7 | GCC2/IO59RSB0 |
| D8 | GCC1/IO51RSB0 |
| D9 | GCC0/IO52RSB0 |

| CS81 | |
|---|---|
| **Pin Number** | **AGLN125 Function** |
| E1 | GFB0/IO120RSB1 |
| E2 | GFB1/IO121RSB1 |
| E3 | GFA1/IO118RSB1 |
| E4 | VCCIB1 |
| E5 | VCC |
| E6 | VCCIB0 |
| E7 | GCA0/IO56RSB0 |
| E8 | GCA1/IO55RSB0 |
| E9 | GCB2/IO58RSB0 |
| F1* | VCCPLF |
| F2* | VCOMPLF |
| F3 | GND |
| F4 | GND |
| F5 | VCCIB1 |
| F6 | GND |
| F7 | GDA1/IO65RSB0 |
| F8 | GDC1/IO61RSB0 |
| F9 | GDC0/IO62RSB0 |
| G1 | GEA0/IO104RSB1 |
| G2 | GEC0/IO108RSB1 |
| G3 | GEB1/IO107RSB1 |
| G4 | IO96RSB1 |
| G5 | IO92RSB1 |
| G6 | IO72RSB1 |
| G7 | GDB2/IO68RSB1 |
| G8 | VJTAG |
| G9 | TRST |
| H1 | GEA1/IO105RSB1 |
| H2 | FF/GEB2/IO102RSB1 |
| H3 | IO99RSB1 |
| H4 | IO94RSB1 |
| H5 | IO91RSB1 |
| H6 | IO81RSB1 |
| H7 | GDA2/IO67RSB1 |
| H8 | TDI |
| H9 | TDO |

| CS81 | |
|---|---|
| **Pin Number** | **AGLN125 Function** |
| J1 | GEA2/IO103RSB1 |
| J2 | GEC2/IO101RSB1 |
| J3 | IO97RSB1 |
| J4 | IO93RSB1 |
| J5 | IO90RSB1 |
| J6 | IO78RSB1 |
| J7 | TCK |
| J8 | TMS |
| J9 | VPUMP |

*Note: * Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN125-CS81.*

| CS81 | |
|---|---|
| **Pin Number** | **AGLN250 Function** |
| A1 | GAA0/IO00RSB0 |
| A2 | GAA1/IO01RSB0 |
| A3 | GAC0/IO04RSB0 |
| A4 | IO07RSB0 |
| A5 | IO09RSB0 |
| A6 | IO12RSB0 |
| A7 | GBB0/IO16RSB0 |
| A8 | GBA1/IO19RSB0 |
| A9 | GBA2/IO20RSB1 |
| B1 | GAA2/IO67RSB3 |
| B2 | GAB0/IO02RSB0 |
| B3 | GAC1/IO05RSB0 |
| B4 | IO06RSB0 |
| B5 | IO10RSB0 |
| B6 | GBC0/IO14RSB0 |
| B7 | GBB1/IO17RSB0 |
| B8 | IO21RSB1 |
| B9 | GBB2/IO22RSB1 |
| C1 | GAB2/IO65RSB3 |
| C2 | IO66RSB3 |
| C3 | GND |
| C4 | IO08RSB0 |
| C5 | IO11RSB0 |
| C6 | GND |
| C7 | GBA0/IO18RSB0 |
| C8 | GBC2/IO23RSB1 |
| C9 | IO24RSB1 |
| D1 | GAC2/IO63RSB3 |
| D2 | IO64RSB3 |
| D3 | GFA2/IO56RSB3 |
| D4 | VCC |
| D5 | VCCIB0 |
| D6 | GND |
| D7 | IO30RSB1 |
| D8 | GCC1/IO25RSB1 |
| D9 | GCC0/IO26RSB1 |

| CS81 | |
|---|---|
| **Pin Number** | **AGLN250 Function** |
| E1 | GFB0/IO59RSB3 |
| E2 | GFB1/IO60RSB3 |
| E3 | GFA1/IO58RSB3 |
| E4 | VCCIB3 |
| E5 | VCC |
| E6 | VCCIB1 |
| E7 | GCA0/IO28RSB1 |
| E8 | GCA1/IO27RSB1 |
| E9 | GCB2/IO29RSB1 |
| F1 | VCCPLF |
| F2 | VCOMPLF |
| F3 | GND |
| F4 | GND |
| F5 | VCCIB2 |
| F6 | GND |
| F7 | GDA1/IO33RSB1 |
| F8 | GDC1/IO31RSB1 |
| F9 | GDC0/IO32RSB1 |
| G1 | GEA0/IO51RSB3 |
| G2 | GEC1/IO54RSB3 |
| G3 | GEC0/IO53RSB3 |
| G4 | IO45RSB2 |
| G5 | IO42RSB2 |
| G6 | IO37RSB2 |
| G7 | GDB2/IO35RSB2 |
| G8 | VJTAG |
| G9 | TRST |
| H1 | GEA1/IO52RSB3 |
| H2 | FF/GEB2/IO49RSB2 |
| H3 | IO47RSB2 |
| H4 | IO44RSB2 |
| H5 | IO41RSB2 |
| H6 | IO39RSB2 |
| H7 | GDA2/IO34RSB2 |
| H8 | TDI |
| H9 | TDO |

| CS81 | |
|---|---|
| **Pin Number** | **AGLN250 Function** |
| J1 | GEA2/IO50RSB2 |
| J2 | GEC2/IO48RSB2 |
| J3 | IO46RSB2 |
| J4 | IO43RSB2 |
| J5 | IO40RSB2 |
| J6 | IO38RSB2 |
| J7 | TCK |
| J8 | TMS |
| J9 | VPUMP |

*Note: * Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN250-CS81.*

# 5 – Datasheet Information

## List of Changes

The following table lists critical changes that were made in each version of the IGLOO nano datasheet.

| Revision | Changes | Page |
|---|---|---|
| Revision 19 (October 2015) | Modified the note to include device/package obsoletion information in "Features and Benefits" section (SAR 69724). | 1-I |
| | Added a note under Security Feature "Y" in "IGLOO nano Ordering Information" section (SAR 70553). | 1-IV |
| | Modified AGLN250 pin assignment table to match with I/O Attribute Editor tool from Libero in "CS81" Package (SAR 59049). | 4-6 |
| | Modified the nominal area to 25 for CS81 Package in Table 1 (SAR 71127). | 1-II |
| | Modified the title of AGLN125Z pin assignment table for "CS81" Package (SAR 71127). | 4-6 |
| Revision 18 (November 2013) | Modified the "Device Marking" section and updated Figure 1 • Example of Device Marking for Small Form Factor Packages to reflect updates suggested per CN1004 published on 5/10/2010 (SAR 52036). | V |
| Revision 17 (May 2013) | Deleted details related to Ambient temperature from "Enhanced Commercial Temperature Range", "IGLOO nano Ordering Information", "Temperature Grade Offerings", and Table 2-2 • Recommended Operating Conditions [1] to remove ambiguities arising due to the same, and modified Note 2 (SAR 47063). | I, IV, VI, and 2-2 |
| Revision 16 (December 2012) | The "IGLOO nano Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43174). | IV |
| | The note in Table 2-100 • IGLOO nano CCC/PLL Specification and Table 2-101 • IGLOO nano CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42565). | 2-70, 2-71 |
| | Live at Power-Up (LAPU) has been replaced with ’Instant On’. | NA |
| Revision 15 (September 2012) | The status of the AGLN125 device has been modified from ’Advance’ to ’Production’ in the "IGLOO nano Device Status" section (SAR 41416). | III |
| | Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40274). | NA |
| Revision 14 (September 2012) | The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data. | 1-2 |
| Revision 13 (June 2012) | Figure Figure 2-34 • FIFO Read and Figure 2-35 • FIFO Write have been added (SAR 34842). | 2-82 |
| | The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions" section: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with “Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks” (SAR 38319). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement. | 3-1 |

| Revision | Changes | Page |
|---|---|---|
| Revision 11 (Jul 2010) | The status of the AGLN060 device has changed from Advance to Production. | III |
| | The values for PAC1, PAC2, PAC3, and PAC4 were updated in Table 2-15 • Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices for 1.5 V core supply voltage (SAR 26404). | 2-10 |
| | The values for PAC1, PAC2, PAC3, and PAC4 were updated in Table 2-17 • Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices for 1.2 V core supply voltage (SAR 26404). | 2-11 |
| July 2010 | The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "IGLOO nano Device Status" table on page III indicates the status for each device in the device family. | N/A |
| Revision 10 (Apr 2010) | References to differential inputs were removed from the datasheet, since IGLOO nano devices do not support differential inputs (SAR 21449). | N/A |
| | A parenthetical note, "hold previous I/O state in Flash*Freeze mode," was added to each occurrence of bus hold in the datasheet (SAR 24079). | N/A |
| | The "In-System Programming (ISP) and Security" section was revised to add 1.2 V programming. | I |
| | The note connected with the "IGLOO nano Ordering Information" table was revised to clarify features not available for Z feature grade devices. | IV |
| | The "IGLOO nano Device Status" table is new. | III |
| | The definition of C in the "Temperature Grade Offerings" table was changed to "extended commercial temperature range". | VI |
| | 1.2 V wide range was added to the list of voltage ranges in the "I/Os with Advanced I/O Standards" section. | 1-8 |
| | A note was added to Table 2-2 • Recommended Operating Conditions [1] regarding switching from 1.2 V to 1.5 V core voltage for in-system programming. The VJTAG voltage was changed from "1.425 to 3.6" to "1.4 to 3.6" (SAR 24052). The note regarding voltage for programming V2 and V5 devices was revised (SAR 25213). The maximum value for VPUMP programming voltage (operation mode) was changed from 3.45 V to 3.6 V (SAR 25220). | 2-2 |
| | Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.425 V) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.14 V) were updated. Table 2-8 • Power Supply State per Mode is new. | 2-6, 2-7 |
| | The tables in the "Quiescent Supply Current" section were updated (SAR 24882 and SAR 24112). | 2-7 |
| | VJTAG was removed from Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO nano Sleep Mode* (SARs 24112, 24882, and 79503). | 2-8 |
| | The note stating what was included in $I_{DD}$ was removed from Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOO nano Shutdown Mode. The note, "per VCCI or VJTAG bank" was removed from Table 2-12 • Quiescent Supply Current (IDD), No IGLOO nano Flash*Freeze Mode[1]. The note giving $I_{DD}$ was changed to "$I_{DD}$ = $N_{BANKS}$ * $I_{CCI}$ + $I_{CCA}$." | 2-8 |
| | The values in Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings and Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] were updated. Wide range support information was added. | 2-9 |

| Revision / Version | Changes | Page |
|---|---|---|
| **Revision 9 (Mar2010)**<br>Product Brief Advance v0.9<br>Packaging Advance v0.8 | All product tables and pin tables were updated to show clearly that AGLN030 is available only in the Z feature grade at this time. The nano-Z feature grade devices are designated with a Z at the end of the part number. | N/A |
| **Revision 8 (Jan 2009)** | The "Reprogrammable Flash Technology" section was revised to add "250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance". | I |
| Product Brief Advance v0.8 | The note for AGLN030 in the "IGLOO nano Devices" table and "I/Os Per Package" table was revised to remove the statement regarding package compatibility with lower density nano devices. | II, II |
| | The "I/Os with Advanced I/O Standards" section was revised to add definitions for hot-swap and cold-sparing. | 1-8 |
| Packaging Advance v0.7 | The "UC81", "CS81", "QN48", and "QN68" pin tables for AGLN030 are new. | 4-5, 4-8, 4-17, 4-21 |
| | The "CS81"pin table for AGLN060 is new. | 4-9 |
| | The "CS81" and "VQ100" pin tables for AGLN060Z are new. | 4-10, 4-25 |
| | The "CS81" and "VQ100" pin tables for AGLN125Z are new. | 4-12, 4-27 |
| | The "CS81" and "VQ100" pin tables for AGLN250Z is new. | 4-14, 4-29 |
| **Revision 7 (Apr 2009)**<br>Product Brief Advance v0.7<br>DC and Switching Characteristics Advance v0.3 | The –F speed grade is no longer offered for IGLOO nano devices and was removed from the datasheet. | N/A |
| **Revision 6 (Mar 2009)**<br>Packaging Advance v0.6 | The "VQ100" pin table for AGLN030 is new. | 4-23 |
| **Revision 5 (Feb 2009)**<br>Packaging Advance v0.5 | The "100-Pin QFN" section was removed. | N/A |
| **Revision 4 (Feb 2009)** | The QN100 package was removed for all devices. | N/A |
| Product Brief Advance v0.6 | "IGLOO nano Devices" table was updated to change the maximum user I/Os for AGLN030 from 81 to 77. | II |
| | The "Device Marking" section is new. | V |
| **Revision 3 (Feb 2009)**<br>Product Brief Advance v0.5 | The following table note was removed from "IGLOO nano Devices" table: "Six chip (main) and three quadrant global networks are available for AGLN060 and above." | II |
| | The CS81 package was added for AGLN250 in the "IGLOO nano Products Available in the Z Feature Grade" table. | VI |
| Packaging Advance v0.4 | The "UC81" and "CS81" pin tables for AGLN020 are new. | 4-4, 4-7 |
| | The "CS81" pin table for AGLN250 is new. | 4-13 |

| Revision / Version | Changes | Page |
|---|---|---|
| **Revision 1 (cont'd)**<br>Packaging Advance v0.2 | The "QN48" pin diagram was revised. | 4-16 |
| | Note 2 for the "QN48", "QN68", and "100-Pin QFN" pin diagrams was changed to "The die attach paddle of the package is tied to ground (GND)." | 4-16, 4-19 |
| | The "VQ100" pin diagram was revised to move the pin IDs to the upper left corner instead of the upper right corner. | 4-23 |
| **Revision 0 (Oct 2008)**<br>Product Brief Advance v0.2 | The following tables and sections were updated to add the UC81 and CS81 packages for AGL030:<br>"IGLOO nano Devices"<br>"I/Os Per Package"<br>"IGLOO nano Products Available in the Z Feature Grade"<br>"Temperature Grade Offerings" | N/A |
| | The "I/Os Per Package" table was updated to add the following information to table note 4: "For nano devices, the VQ100 package is offered in both leaded and RoHS-compliant versions. All other packages are RoHS-compliant only." | II |
| | The "IGLOO nano Products Available in the Z Feature Grade" section was updated to remove QN100 for AGLN250. | VI |
| | The device architecture figures, Figure 1-3 • IGLOO Device Architecture Overview with Two I/O Banks (AGLN060, AGLN125) through Figure 1-4 • IGLOO Device Architecture Overview with Four I/O Banks (AGLN250), were revised. Figure 1-1 • IGLOO Device Architecture Overview with Two I/O Banks and No RAM (AGLN010 and AGLN030) is new. | 1-4 through 1-5 |
| | The "PLL and CCC" section was revised to include information about CCC-GLs in AGLN020 and smaller devices. | 1-7 |
| | The "I/Os with Advanced I/O Standards" section was revised to add information about IGLOO nano devices supporting double-data-rate applications. | 1-8 |

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