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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

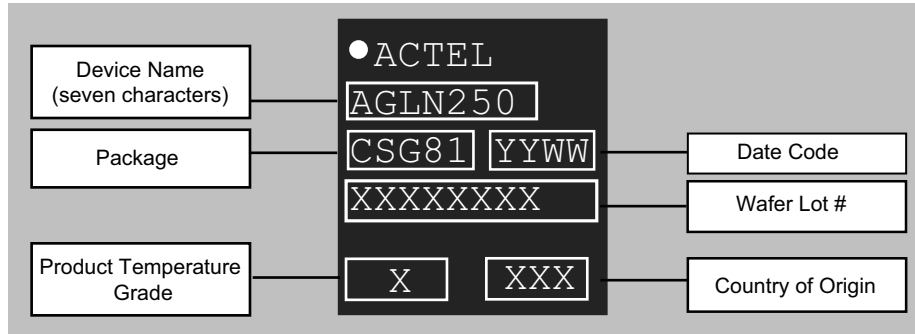
#### Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	768
Total RAM Bits	-
Number of I/O	34
Number of Gates	30000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-20°C ~ 85°C (TJ)
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (6x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microsemi/agln030v2-zqng48">https://www.e-xfl.com/product-detail/microsemi/agln030v2-zqng48</a>

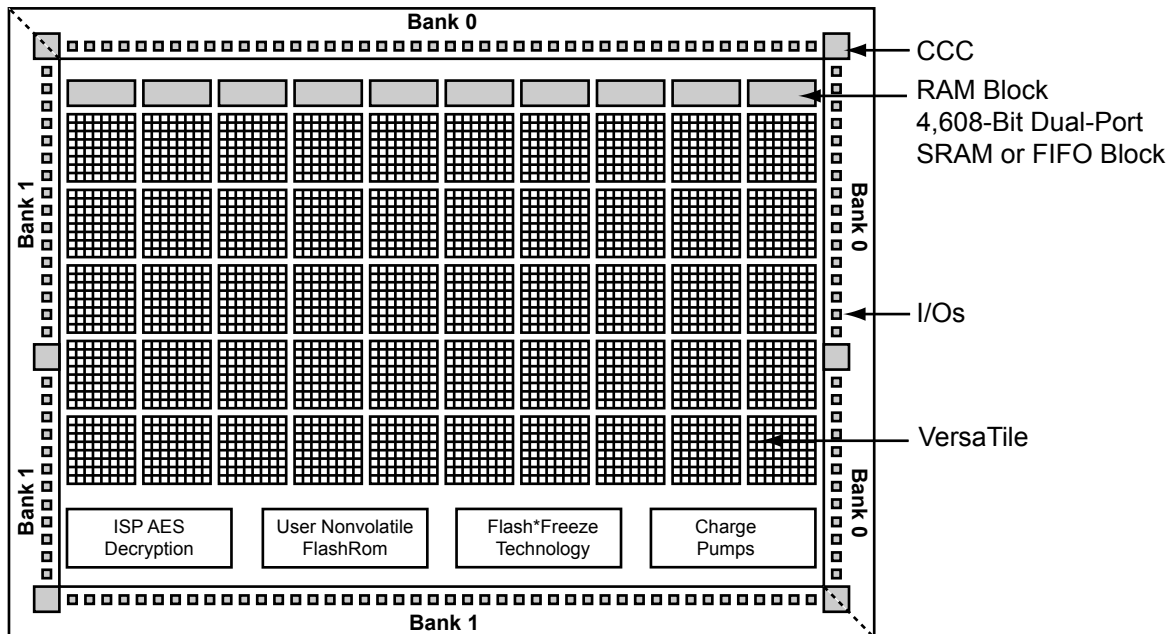
## Device Marking

Microsemi normally topside marks the full ordering part number on each device. There are some exceptions to this, such as some of the Z feature grade nano devices, the V2 designator for IGLOO devices, and packages where space is physically limited. Packages that have limited characters available are UC36, UC81, CS81, QN48, QN68, and QFN132. On these specific packages, a subset of the device marking will be used that includes the required legal information and as much of the part number as allowed by character limitation of the device. In this case, devices will have a truncated device marking and may exclude the applications markings, such as the I designator for Industrial Devices or the ES designator for Engineering Samples.

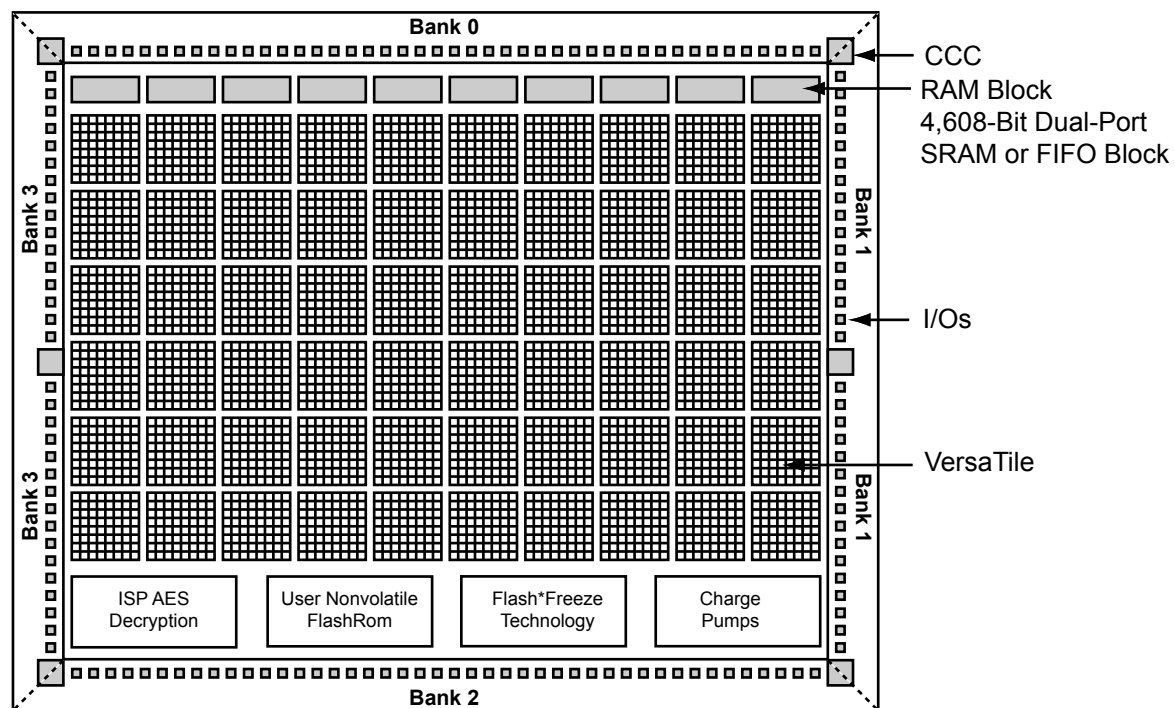
Figure 1 shows an example of device marking based on the AGLN250V2-CSG81. The actual mark will vary by the device/package combination ordered.



**Figure 1 • Example of Device Marking for Small Form Factor Packages**



**Figure 1-3 • IGLOO Device Architecture Overview with Two I/O Banks (AGLN060, AGLN125)**



**Figure 1-4 • IGLOO Device Architecture Overview with Four I/O Banks (AGLN250)**

## Flash\*Freeze Technology

The IGLOO nano device has an ultra-low power static mode, called Flash\*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash\*Freeze technology enables the user to quickly (within 1  $\mu$ s) enter and exit Flash\*Freeze mode by activating the Flash\*Freeze pin while all power supplies are kept at their original values. I/Os, global I/Os, and clocks can still be driven and can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and I/O states. I/Os can be individually configured to either hold their previous state or be tristated during Flash\*Freeze mode.

Alternatively, I/Os can be set to a specific state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 2  $\mu$ W in this mode.

Flash\*Freeze technology allows the user to switch to Active mode on demand, thus simplifying the power management of the device.

The Flash\*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. Refer to Figure 1-5 for an illustration of entering/exiting Flash\*Freeze mode. It is also possible to use the Flash\*Freeze pin as a regular I/O if Flash\*Freeze mode usage is not planned.

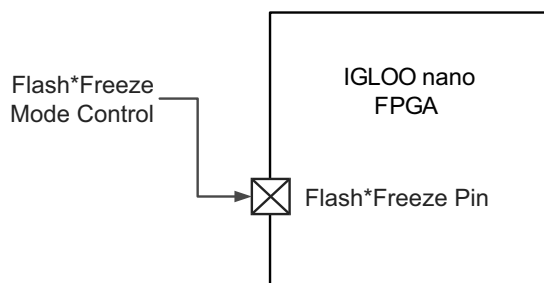


Figure 1-5 • IGLOO nano Flash\*Freeze Mode

## VersaTiles

The IGLOO nano core consists of VersaTiles, which have been enhanced beyond the ProASIC<sup>PLUS</sup>® core tiles. The IGLOO nano VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-6 for VersaTile configurations.

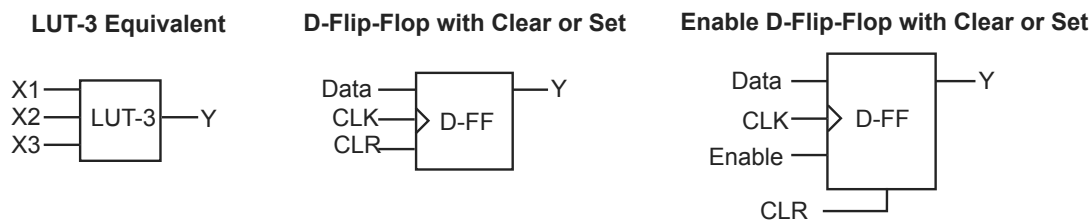


Figure 1-6 • VersaTile Configurations

## **User Nonvolatile FlashROM**

IGLOO nano devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IGLOO nano IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the AGLN030 and smaller devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The IGLOO nano development software solutions, Libero<sup>®</sup> System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature enables the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Microsemi Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

## **SRAM and FIFO**

IGLOO nano devices (except the AGLN030 and smaller devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in the AGLN030 and smaller devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

## **PLL and CCC**

Higher density IGLOO nano devices using either the two I/O bank or four I/O bank architectures provide designers with very flexible clock conditioning capabilities. AGLN060, AGLN125, and AGLN250 contain six CCCs. One CCC (center west side) has a PLL. The AGLN030 and smaller devices use different CCCs in their architecture (CCC-GL). These CCC-GLs contain a global MUX but do not have any PLLs or programmable delays.

For devices using the six CCC block architecture, these are located at the four corners and the centers of the east and west sides. All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

## 2 – IGLOO nano DC and Switching Characteristics

### General Specifications

The Z feature grade does not support the enhanced nano features of Schmitt trigger input, Flash\*Freeze bus hold (hold previous I/O state in Flash\*Freeze mode), cold-sparing, and hot-swap I/O capability. Refer to "IGLOO nano Ordering Information" on page IV for more information.

### Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

**Table 2-1 • Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O buffer supply voltage	–0.3 to 3.75	V
VI <sup>1</sup>	I/O input voltage	–0.3 V to 3.6 V	V
T <sub>STG</sub> <sup>2</sup>	Storage temperature	–65 to +150	°C
T <sub>J</sub> <sup>2</sup>	Junction temperature	+125	°C

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.
2. For flash programming and retention maximum limits, refer to Table 2-3 on page 2-2, and for recommended operating limits, refer to Table 2-2 on page 2-2.

**Table 2-2 • Recommended Operating Conditions <sup>1</sup>**

Symbol	Parameter		Extended Commercial	Industrial	Units
T <sub>J</sub>	Junction temperature		–20 to + 85 <sup>2</sup>	–40 to +100 <sup>2</sup>	°C
VCC	1.5 V DC core supply voltage <sup>3</sup>		1.425 to 1.575	1.425 to 1.575	V
	1.2 V–1.5 V wide range core voltage <sup>4,5</sup>		1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP <sup>6</sup>	Programming voltage	Programming mode	3.15 to 3.45	3.15 to 3.45	V
		Operation	0 to 3.6	0 to 3.6	V
VCCPLL <sup>7</sup>	Analog power supply (PLL)	1.5 V DC core supply voltage <sup>3</sup>	1.425 to 1.575	1.425 to 1.575	V
		1.2 V–1.5 V wide range core supply voltage <sup>4</sup>	1.14 to 1.575	1.14 to 1.575	V
VCCI and VMV <sup>8,9</sup>	1.2 V DC supply voltage <sup>4</sup>		1.14 to 1.26	1.14 to 1.26	V
	1.2 V DC wide range supply voltage <sup>4</sup>		1.14 to 1.575	1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	3.3 V DC wide range supply voltage <sup>10</sup>		2.7 to 3.6	2.7 to 3.6	V

**Notes:**

1. All parameters representing voltages are measured with respect to GND unless otherwise specified.
2. Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the Libero Online Help.
3. For IGLOO® nano V5 devices
4. For IGLOO nano V2 devices only, operating at VCCI ≥ VCC
5. IGLOO nano V5 devices can be programmed with the VCC core voltage at 1.5 V only. IGLOO nano V2 devices can be programmed with the VCC core voltage at 1.2 V (with FlashPro4 only) or 1.5 V. If you are using FlashPro3 and want to do in-system programming using 1.2 V, please contact the factory.
6. V<sub>PUMP</sub> can be left floating during operation (not programming mode).
7. VCCPLL pins should be tied to VCC pins. See the "Pin Descriptions" chapter for further information.
8. VMV pins must be connected to the corresponding VCCI pins. See the Pin Descriptions chapter of the IGLOO nano FPGA Fabric User's Guide for further information.
9. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-21 on page 2-19. VCCI should be at the same voltage within a given I/O bank.
10. 3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.

**Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature<sup>1</sup>**

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T <sub>STG</sub> (°C) <sup>2</sup>	Maximum Operating Junction Temperature T <sub>J</sub> (°C) <sup>2</sup>
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

**Notes:**

1. This is a stress rating only; functional operation at any condition other than those indicated is not implied.
2. These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.

**Applies to IGLOO nano at 1.2 V Core Operating Conditions**

**Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings**  
STD Speed Grade, Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$ ,  
Worst-Case  $V_{CCI} = 3.0\text{ V}$

I/O Standard	Drive Strength (mA)	Equiv. Software Default Drive Strength Option <sup>1</sup>	Slew Rate	Capacitive Load (pF)	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
3.3 V LVTTTL / 3.3 V LVCMOS	8 mA	8 mA	High	5 pF	1.55	2.31	0.26	0.97	1.36	1.10	2.34	1.90	2.43	3.14	ns
3.3 V LVCMOS Wide Range <sup>2</sup>	100 $\mu\text{A}$	8 mA	High	5 pF	1.55	3.25	0.26	1.31	1.91	1.10	3.25	2.61	3.38	4.27	ns
2.5 V LVCMOS	8 mA	8 mA	High	5 pF	1.55	2.30	0.26	1.21	1.39	1.10	2.33	2.04	2.41	2.99	ns
1.8 V LVCMOS	4 mA	4 mA	High	5 pF	1.55	2.49	0.26	1.13	1.59	1.10	2.53	2.34	2.42	2.81	ns
1.5 V LVCMOS	2 mA	2 mA	High	5 pF	1.55	2.78	0.26	1.27	1.77	1.10	2.82	2.62	2.44	2.74	ns
1.2 V LVCMOS	1 mA	1 mA	High	5 pF	1.55	3.50	0.26	1.56	2.27	1.10	3.37	3.10	2.55	2.66	ns
1.2 V LVCMOS Wide Range <sup>3</sup>	100 $\mu\text{A}$	1 mA	High	5 pF	1.55	3.50	0.26	1.56	2.27	1.10	3.37	3.10	2.55	2.66	ns

**Notes:**

1. The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is  $\pm 100\text{ }\mu\text{A}$ . Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range, as specified in the JESD8-B specification.
3. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V side range as specified in the JESD8-12 specification.
4. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



## Timing Characteristics

### Applies to 1.5 V DC Core Voltage

**Table 2-53 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
2 mA	STD	0.97	5.44	0.19	1.03	1.44	0.66	5.25	5.44	1.69	1.35	ns
4 mA	STD	0.97	4.44	0.19	1.03	1.44	0.66	4.37	4.44	1.99	2.11	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

**Table 2-54 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
2 mA	STD	0.97	2.64	0.19	1.03	1.44	0.66	2.59	2.64	1.69	1.40	ns
4 mA	STD	0.97	2.08	0.19	1.03	1.44	0.66	2.12	1.95	1.99	2.19	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

### Applies to 1.2 V DC Core Voltage

**Table 2-55 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
2 mA	STD	1.55	5.92	0.26	1.13	1.59	1.10	5.72	5.92	2.11	1.95	ns
4 mA	STD	1.55	4.91	0.26	1.13	1.59	1.10	4.82	4.91	2.42	2.73	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

**Table 2-56 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
2 mA	STD	1.55	3.05	0.26	1.13	1.59	1.10	3.01	3.05	2.10	2.00	ns
4 mA	STD	1.55	2.49	0.26	1.13	1.59	1.10	2.53	2.34	2.42	2.81	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

## 1.2 V LVCMOS (JESD8-12A)

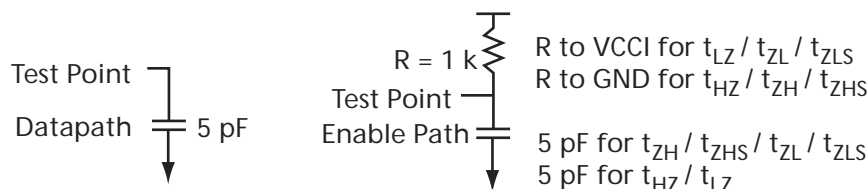
Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

**Table 2-63 • Minimum and Maximum DC Input and Output Levels**

1.2 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
1 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	1	1	10	13	10	10

Notes:

1.  $I_{IL}$  is the input leakage current per I/O pin over recommended operating conditions where  $-0.3 < V_{IN} < V_{IL}$ .
2.  $I_{IH}$  is the input leakage current per I/O pin over recommended operating conditions where  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.



**Figure 2-11 • AC Loading**

**Table 2-64 • 1.2 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C <sub>LOAD</sub> (pF)
0	1.2	0.6	5

Note: \*Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.

## Timing Characteristics

**Applies to 1.2 V DC Core Voltage**

**Table 2-65 • 1.2 V LVCMOS Low Slew**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	Units
1 mA	STD	1.55	8.30	0.26	1.56	2.27	1.10	7.97	7.54	2.56	2.55	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

**Table 2-66 • 1.2 V LVCMOS High Slew**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	Units
1 mA	STD	1.55	3.50	0.26	1.56	2.27	1.10	3.37	3.10	2.55	2.66	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

## 1.2 V LVCMOS Wide Range

**Table 2-67 • Minimum and Maximum DC Input and Output Levels**

1.2 V LVCMOS Wide Range	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
1 mA	-0.3	0.3 * VCCI	0.7 * VCCI	3.6	0.1	VCCI - 0.1	100	100	10	13	10	10

Notes:

1.  $I_{IL}$  is the input leakage current per I/O pin over recommended operating conditions where  $-0.3 < V_{IN} < V_{IL}$ .
2.  $I_{IH}$  is the input leakage current per I/O pin over recommended operating conditions where  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Applicable to IGLOO nano V2 devices operating at  $V_{CCI} \geq V_{CC}$ .
6. Software default selection highlighted in gray.

## Timing Characteristics

**Applies to 1.2 V DC Core Voltage**

**Table 2-68 • 1.2 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	Units
100 μA	1 mA	STD	1.55	8.30	0.26	1.56	2.27	1.10	7.97	7.54	2.56	2.55	ns

Notes:

1. The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is  $\pm 100 \mu\text{A}$ . Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

**Table 2-69 • 1.2 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

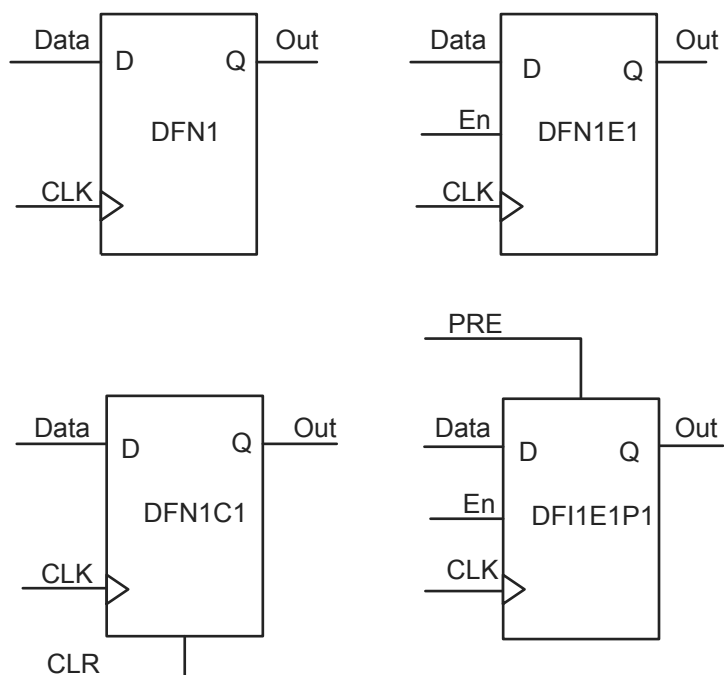
Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	Units
100 μA	1 mA	STD	1.55	3.50	0.26	1.56	2.27	1.10	3.37	3.10	2.55	2.66	ns

Notes:

1. The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is  $\pm 100 \mu\text{A}$ . Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.
3. Software default selection highlighted in gray.

## VersaTile Specifications as a Sequential Module

The IGLOO nano library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide for Software v10.1*.



**Figure 2-23 • Sample of Sequential Cells**

## 1.2 V DC Core Voltage

**Table 2-87 • Register Delays**  
Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
$t_{CLKQ}$	Clock-to-Q of the Core Register	1.61	ns
$t_{SUD}$	Data Setup Time for the Core Register	1.17	ns
$t_{HD}$	Data Hold Time for the Core Register	0.00	ns
$t_{SUE}$	Enable Setup Time for the Core Register	1.29	ns
$t_{HE}$	Enable Hold Time for the Core Register	0.00	ns
$t_{CLR2Q}$	Asynchronous Clear-to-Q of the Core Register	0.87	ns
$t_{PRE2Q}$	Asynchronous Preset-to-Q of the Core Register	0.89	ns
$t_{REMCLR}$	Asynchronous Clear Removal Time for the Core Register	0.00	ns
$t_{RECCLR}$	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
$t_{REMPRE}$	Asynchronous Preset Removal Time for the Core Register	0.00	ns
$t_{RECPRE}$	Asynchronous Preset Recovery Time for the Core Register	0.24	ns
$t_{WCLR}$	Asynchronous Clear Minimum Pulse Width for the Core Register	0.46	ns
$t_{WPRE}$	Asynchronous Preset Minimum Pulse Width for the Core Register	0.46	ns
$t_{CKMPWH}$	Clock Minimum Pulse Width HIGH for the Core Register	0.95	ns
$t_{CKMPWL}$	Clock Minimum Pulse Width LOW for the Core Register	0.95	ns

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

## Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-70. Table 2-88 to Table 2-96 on page 2-68 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

### Timing Characteristics

#### 1.5 V DC Core Voltage

**Table 2-88 • AGLN010 Global Resource**  
Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	1.13	1.42	ns
$t_{RCKH}$	Input High Delay for Global Clock	1.15	1.50	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock	1.65		ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.35	ns

#### Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

**Table 2-89 • AGLN015 Global Resource**  
Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	1.21	1.55	ns
$t_{RCKH}$	Input High Delay for Global Clock	1.23	1.65	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock	1.65		ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.42	ns

#### Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

## Embedded SRAM and FIFO Characteristics

### SRAM

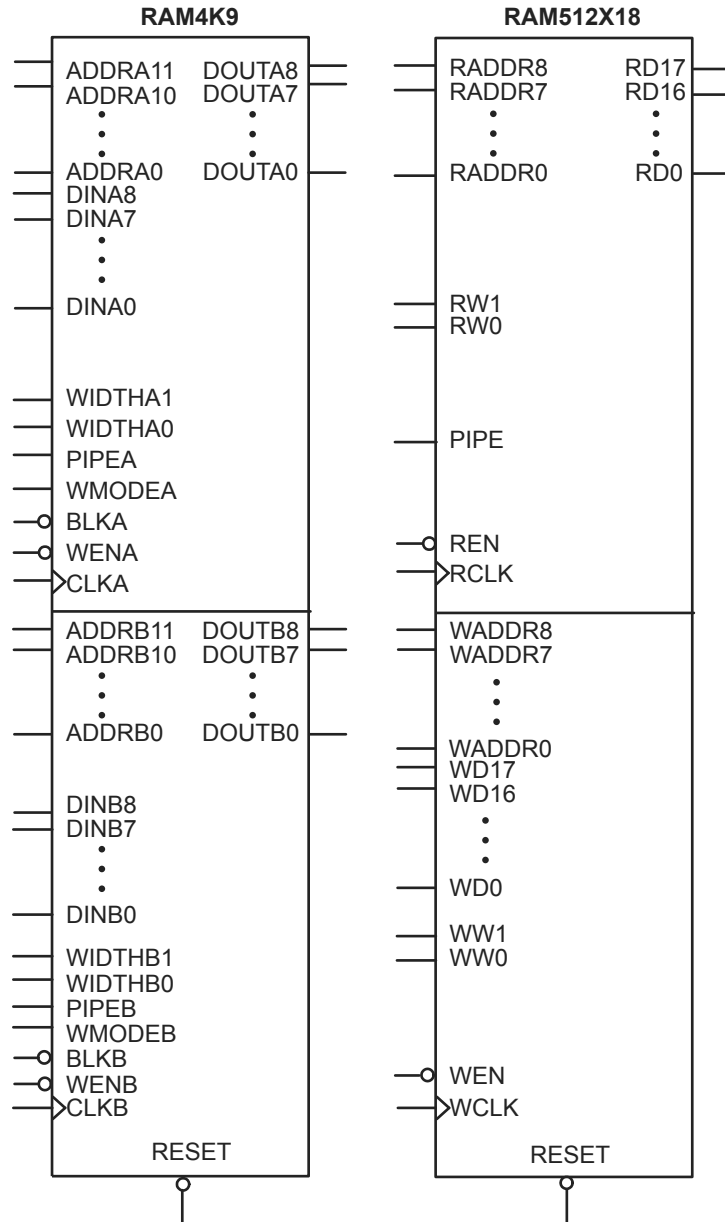
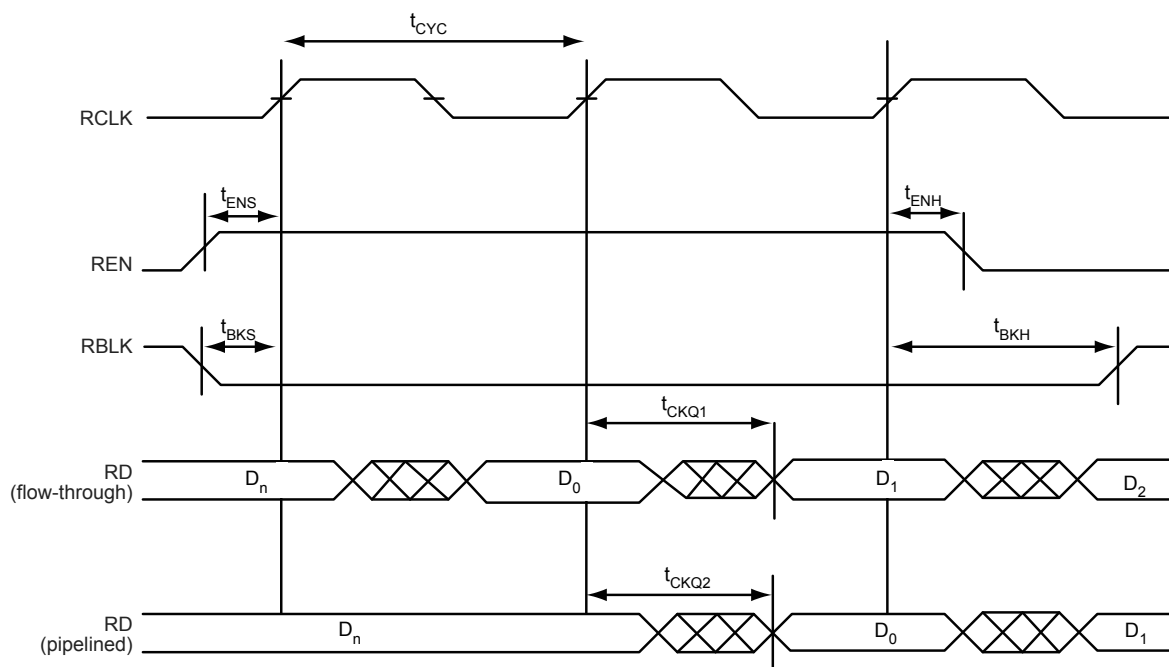
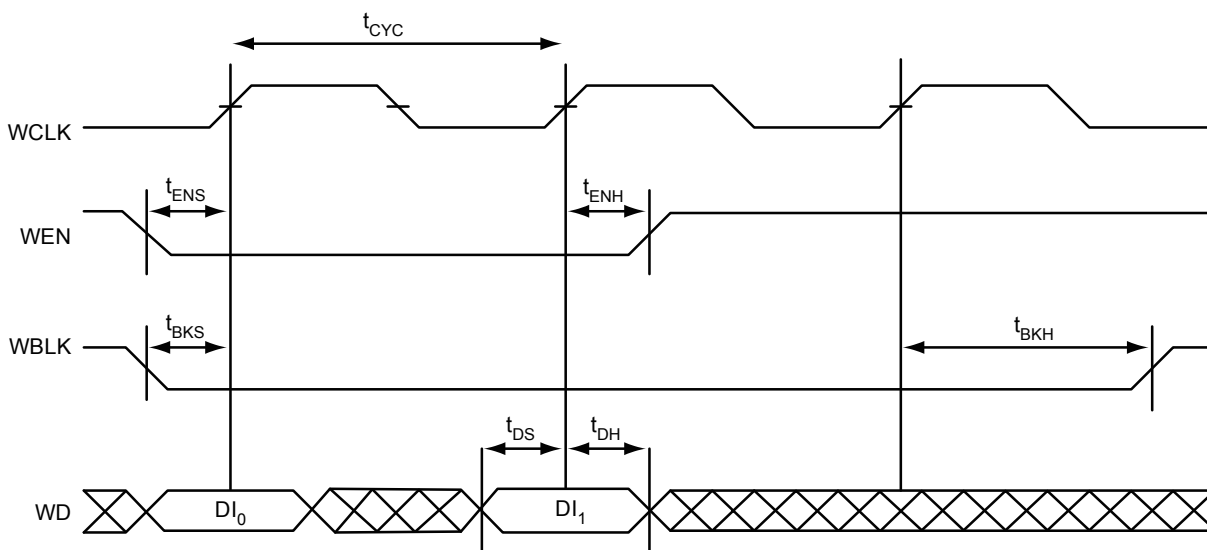


Figure 2-27 • RAM Models

## Timing Waveforms

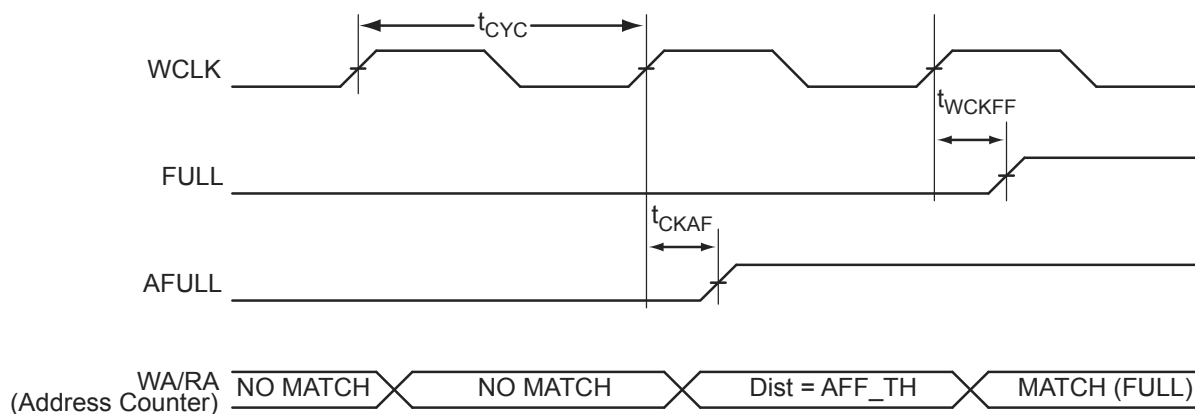


**Figure 2-34 • FIFO Read**

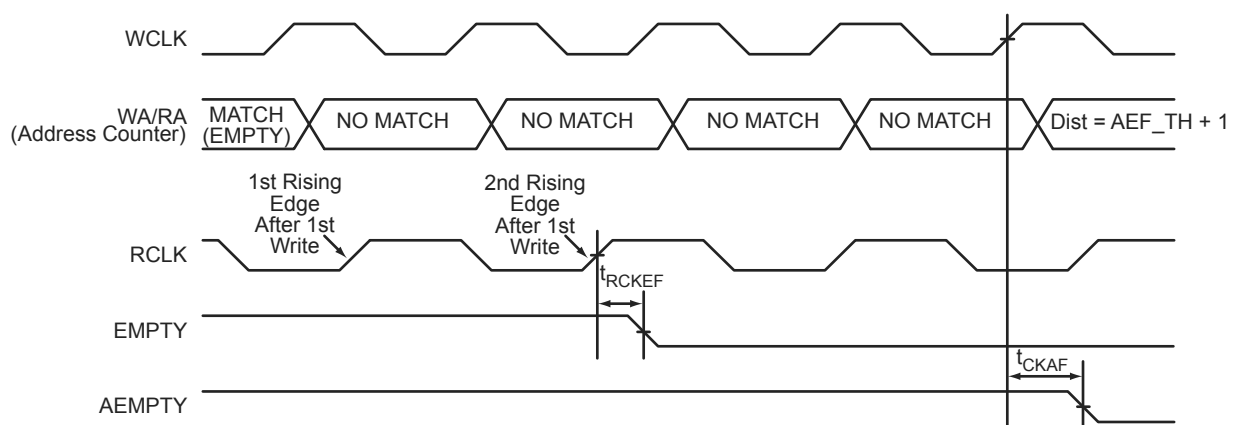


**Figure 2-35 • FIFO Write**

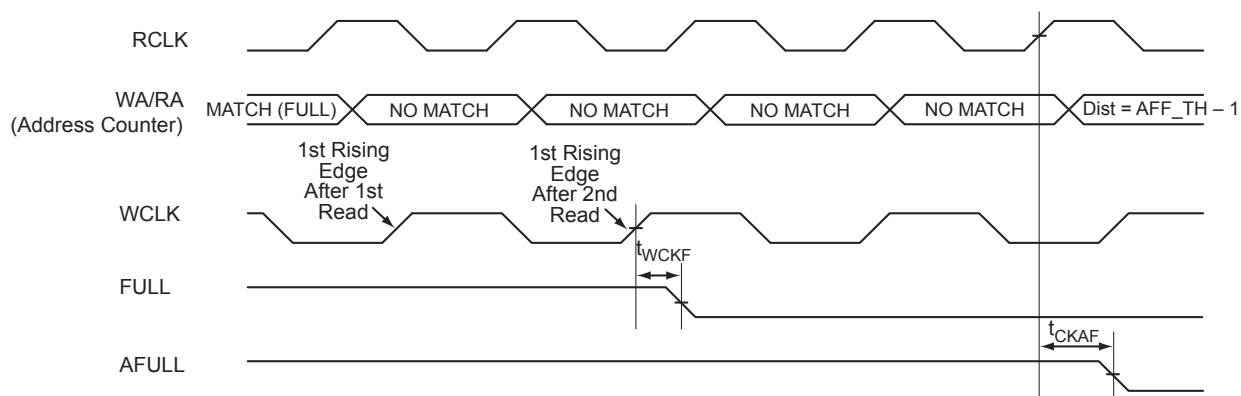




**Figure 2-38 • FIFO FULL Flag and AFULL Flag Assertion**

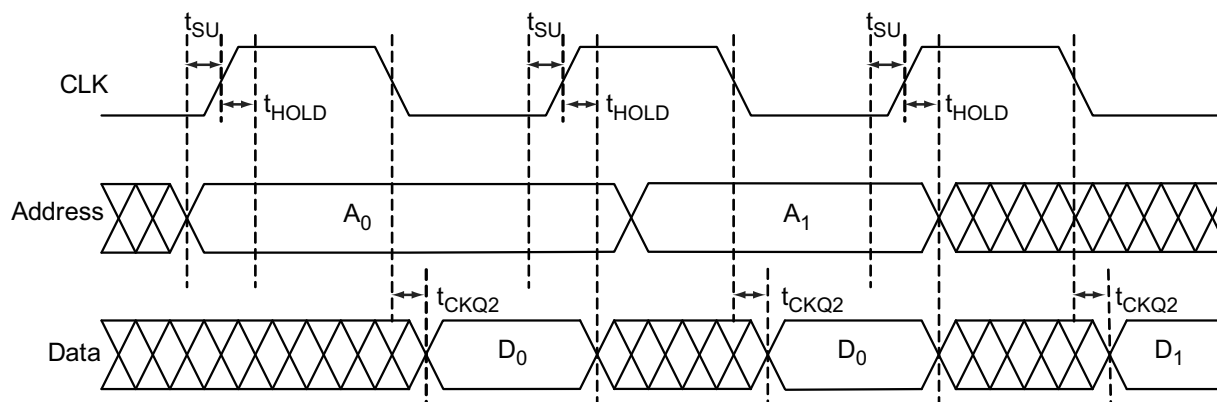


**Figure 2-39 • FIFO EMPTY Flag and AEMPTY Flag Deassertion**



**Figure 2-40 • FIFO FULL Flag and AFULL Flag Deassertion**

## Embedded FlashROM Characteristics



**Figure 2-41 • Timing Diagram**

### **Timing Characteristics**

#### **1.5 V DC Core Voltage**

**Table 2-108 • Embedded FlashROM Access Time**

**Worst Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$**

Parameter	Description	Std.	Units
$t_{SU}$	Address Setup Time	0.57	ns
$t_{HOLD}$	Address Hold Time	0.00	ns
$t_{CK2Q}$	Clock to Out	20.90	ns
$F_{MAX}$	Maximum Clock Frequency	15	MHz

#### **1.2 V DC Core Voltage**

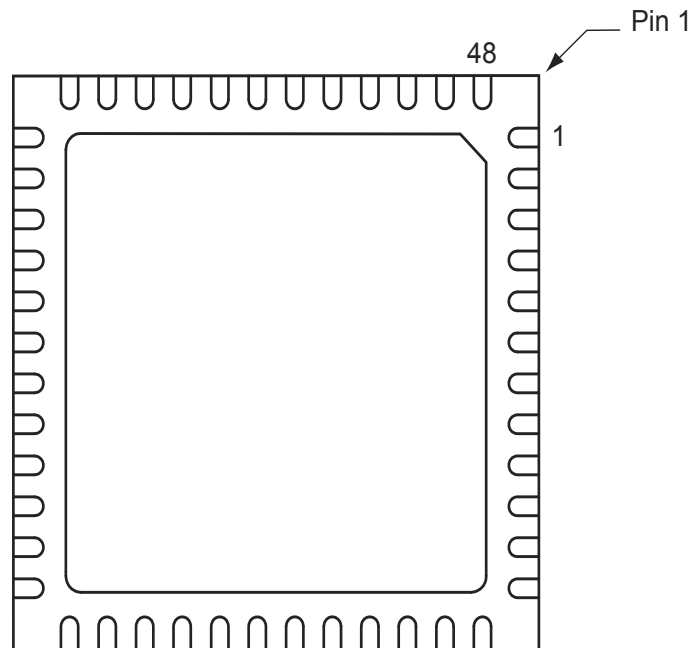
**Table 2-109 • Embedded FlashROM Access Time**

**Worst Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.	Units
$t_{SU}$	Address Setup Time	0.59	ns
$t_{HOLD}$	Address Hold Time	0.00	ns
$t_{CK2Q}$	Clock to Out	35.74	ns
$F_{MAX}$	Maximum Clock Frequency	10	MHz

## QN48

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*Notes:*

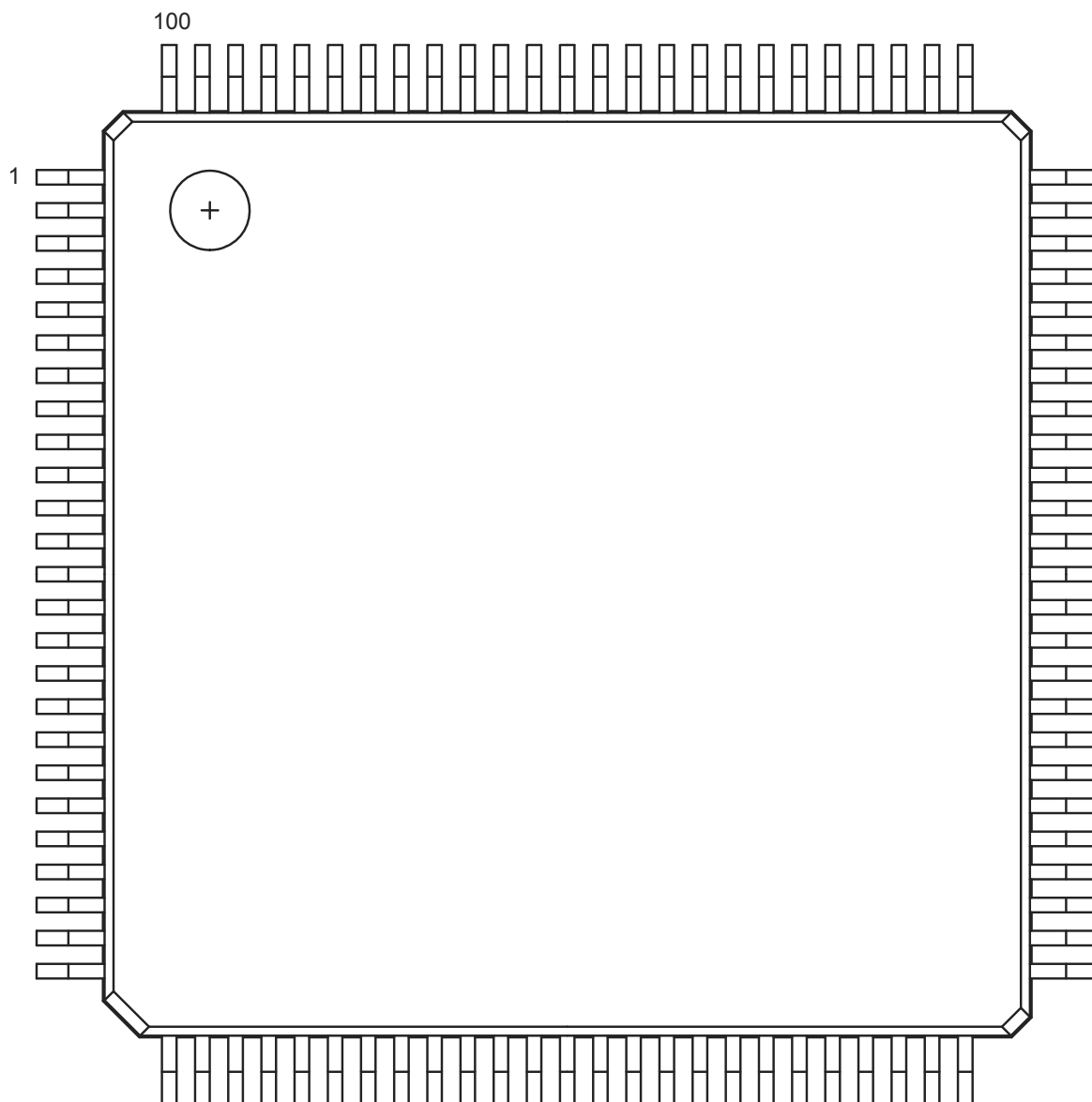
1. *This is the bottom view of the package.*
  2. *The die attach paddle of the package is tied to ground (GND).*
- 

### **Note**

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

## VQ100

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*Note: This is the top view of the package.*

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### **Note**

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

## Datasheet Categories

### **Categories**

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "IGLOO nano Device Status" table on page III, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

#### **Product Brief**

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

#### **Advance**

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

#### **Preliminary**

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

#### **Unmarked (production)**

This version contains information that is considered to be final.

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