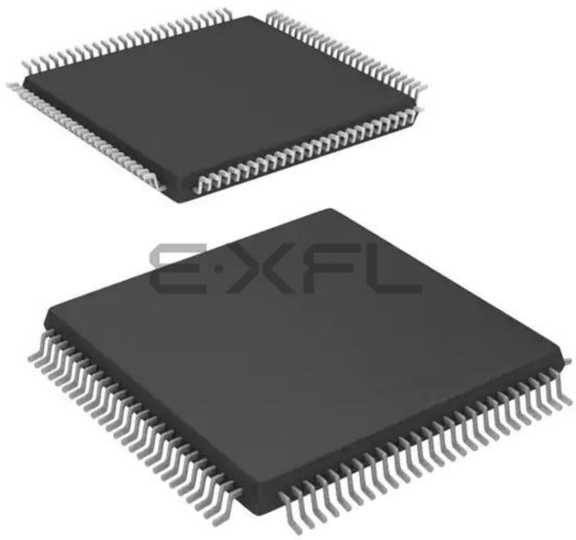

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	768
Total RAM Bits	-
Number of I/O	77
Number of Gates	30000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agln030v2-zvq100i

Device Marking

Microsemi normally topside marks the full ordering part number on each device. There are some exceptions to this, such as some of the Z feature grade nano devices, the V2 designator for IGLOO devices, and packages where space is physically limited. Packages that have limited characters available are UC36, UC81, CS81, QN48, QN68, and QFN132. On these specific packages, a subset of the device marking will be used that includes the required legal information and as much of the part number as allowed by character limitation of the device. In this case, devices will have a truncated device marking and may exclude the applications markings, such as the I designator for Industrial Devices or the ES designator for Engineering Samples.

Figure 1 shows an example of device marking based on the AGLN250V2-CSG81. The actual mark will vary by the device/package combination ordered.

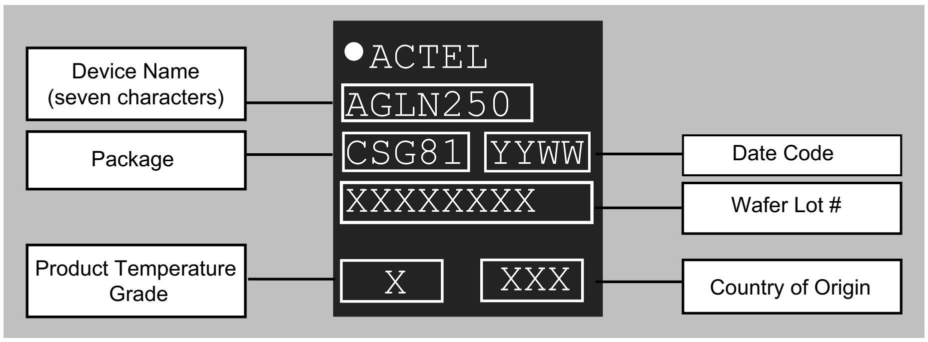

Figure 1 • **Example of Device Marking for Small Form Factor Packages**

IGLOO nano Products Available in the Z Feature Grade

IGLOO nano-Z Devices	AGLN030Z*	AGLN060Z*	AGLN125Z*	AGLN250Z*
	QN48	–	–	–
	QN68	–	–	–
	UC81	–	–	–
	CS81	CS81	CS81	CS81
Packages	VQ100	VQ100	VQ100	VQ100

*Note: *Not recommended for new designs.*

Temperature Grade Offerings

Package	AGLN010	AGLN015*	AGLN020		AGLN060	AGLN125	AGLN250
				AGLN030Z*	AGLN060Z*	AGLN125Z*	AGLN250Z*
UC36	C, I	–	–	–	–	–	–
QN48	C, I	–	–	C, I	–	–	–
QN68	–	C, I	C, I	C, I	–	–	–
UC81	–	–	C, I	C, I	–	–	–
CS81	–	–	C, I	C, I	C, I	C, I	C, I
VQ100	–	–	–	C, I	C, I	C, I	C, I

*Note: * Not recommended for new designs.*

C = Enhanced Commercial temperature range: –20°C to +85°C junction temperature
I = Industrial temperature range: –40°C to +100°C junction temperature

Contact your local Microsemi representative for device availability: http://www.microsemi.com/soc/contact/default.aspx.

1 – IGLOO nano Device Overview

General Description

The IGLOO family of flash FPGAs, based on a 130-nm flash process, offers the lowest power FPGA, a single-chip solution, small footprint packages, reprogrammability, and an abundance of advanced features.

The Flash*Freeze technology used in IGLOO nano devices enables entering and exiting an ultra-low power mode that consumes nanoPower while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low power consumption while the IGLOO nano device is completely functional in the system. This allows the IGLOO nano device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOO nano devices the advantage of being a secure, low power, single-chip solution that is Instant On. The IGLOO nano device is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOO nano devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). The AGLN030 and smaller devices have no PLL or RAM support. IGLOO nano devices have up to 250 k system gates, supported with up to 36 kbits of true dual-port SRAM and up to 71 user I/Os.

IGLOO nano devices increase the breadth of the IGLOO product line by adding new features and packages for greater customer value in high volume consumer, portable, and battery-backed markets. Features such as smaller footprint packages designed with two-layer PCBs in mind, power consumption measured in nanoPower, Schmitt trigger, and bus hold (hold previous I/O state in Flash*Freeze mode) functionality make these devices ideal for deployment in applications that require high levels of flexibility and low cost.

Flash*Freeze Technology

The IGLOO nano device offers unique Flash*Freeze technology, allowing the device to enter and exit ultra-low power Flash*Freeze mode. IGLOO nano devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOO nano V2 devices to support a wide range of core voltage (1.2 V to 1.5 V) allows further reduction in power consumption, thus achieving the lowest total system power.

During Flash*Freeze mode, each I/O can be set to the following configurations: hold previous state, tristate, HIGH, or LOW.

The availability of low power modes, combined with reprogrammability, a single-chip and single-voltage solution, and small-footprint packages make IGLOO nano devices the best fit for portable electronics.

User Nonvolatile FlashROM

IGLOO nano devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IGLOO nano IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the AGLN030 and smaller devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The IGLOO nano development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature enables the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Microsemi Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

IGLOO nano devices (except the AGLN030 and smaller devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in the AGLN030 and smaller devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

Higher density IGLOO nano devices using either the two I/O bank or four I/O bank architectures provide designers with very flexible clock conditioning capabilities. AGLN060, AGLN125, and AGLN250 contain six CCCs. One CCC (center west side) has a PLL. The AGLN030 and smaller devices use different CCCs in their architecture (CCC-GL). These CCC-GLs contain a global MUX but do not have any PLLs or programmable delays.

For devices using the six CCC block architecture, these are located at the four corners and the centers of the east and west sides. All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

6. Click **OK** to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

Table 2-2 • Recommended Operating Conditions [1]

Symbol	Parameter		Extended Commercial	Industrial	Units
T_J	Junction temperature		–20 to + 85[2]	–40 to +100[2]	°C
VCC	1.5 V DC core supply voltage[3]		1.425 to 1.575	1.425 to 1.575	V
	1.2 V–1.5 V wide range core voltage[4,5]		1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP [6]	Programming voltage	Programming mode	3.15 to 3.45	3.15 to 3.45	V
		Operation	0 to 3.6	0 to 3.6	V
VCCPLL[7]	Analog power supply (PLL)	1.5 V DC core supply voltage[3]	1.425 to 1.575	1.425 to 1.575	V
		1.2 V–1.5 V wide range core supply voltage[4]	1.14 to 1.575	1.14 to 1.575	V
VCCI and VMV [8,9]	1.2 V DC supply voltage [4]		1.14 to 1.26	1.14 to 1.26	V
	1.2 V DC wide range supply voltage [4]		1.14 to 1.575	1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	3.3 V DC wide range supply voltage [10]		2.7 to 3.6	2.7 to 3.6	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the Libero Online Help.*
3. *For IGLOO® nano V5 devices*
4. *For IGLOO nano V2 devices only, operating at VCCI ≥ VCC*
5. *IGLOO nano V5 devices can be programmed with the VCC core voltage at 1.5 V only. IGLOO nano V2 devices can be programmed with the VCC core voltage at 1.2 V (with FlashPro4 only) or 1.5 V. If you are using FlashPro3 and want to do in-system programming using 1.2 V, please contact the factory.*
6. *V_{PUMP} can be left floating during operation (not programming mode).*
7. *VCCPLL pins should be tied to VCC pins. See the "Pin Descriptions" chapter for further information.*
8. *VMV pins must be connected to the corresponding VCCI pins. See the Pin Descriptions chapter of the IGLOO nano FPGA Fabric User's Guide for further information.*
9. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-21 on page 2-19. VCCI should be at the same voltage within a given I/O bank.*
10. *3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.*

Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature[1]

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

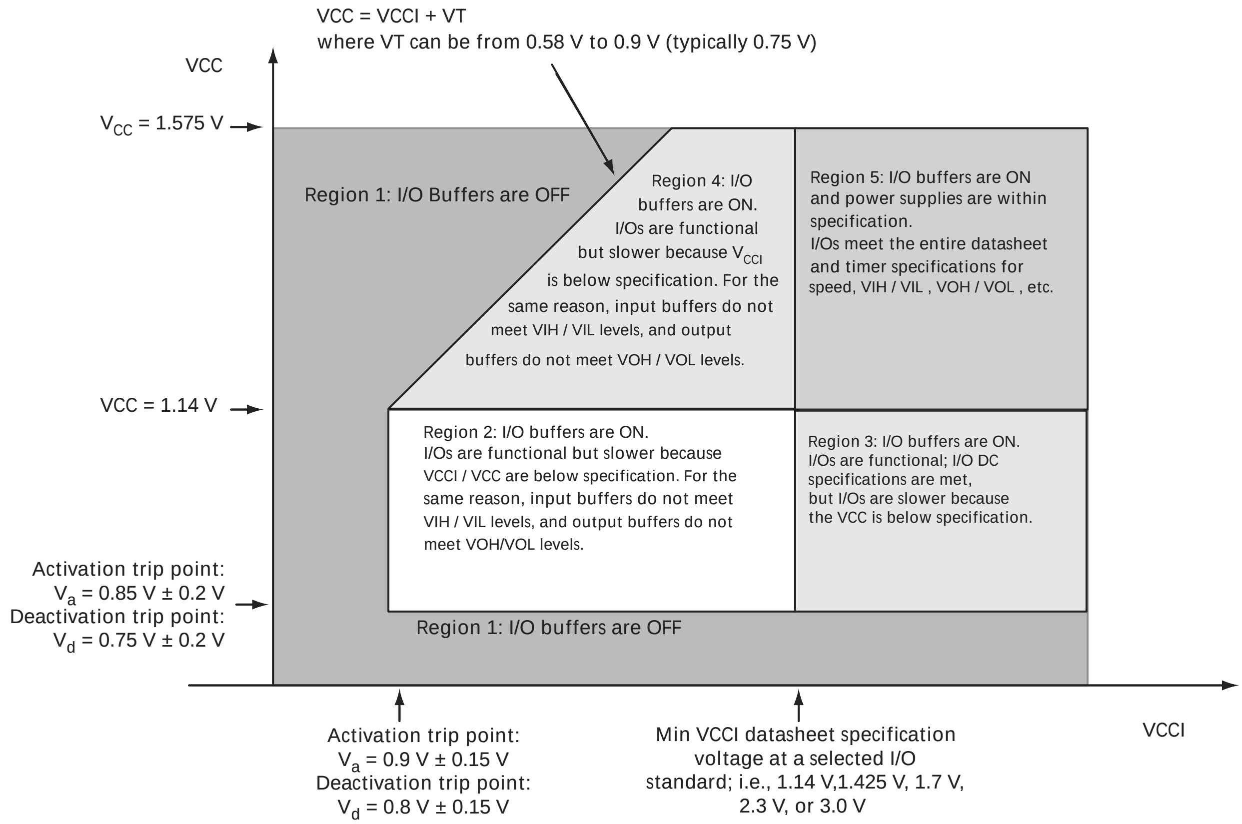

Figure 2-2 • **V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in the Microsemi Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 1

where:

T_A = Ambient temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Figure 2-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The maximum operating junction temperature is 100°C. EQ 2 shows a sample calculation of the maximum operating power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. } (°C) - \text{Max. ambient temp. } (°C)}{\theta_{ja}(°C/W)} = \frac{100°C - 70°C}{20.5°C/W} = 1.46\text{ W}$$

EQ 2

Table 2-5 • **Package Thermal Resistivities**

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 200 ft./min.	θ_{ja} 500 ft./min.	Units
Chip Scale Package (CSP)	36	TBD	TBD	TBD	TBD	C/W
	81	TBD	TBD	TBD	TBD	C/W
Quad Flat No Lead (QFN)	48	TBD	TBD	TBD	TBD	C/W
	68	TBD	TBD	TBD	TBD	C/W
	100	TBD	TBD	TBD	TBD	C/W
Very Thin Quad Flat Pack (VQFP)	100	10.0	35.3	29.4	27.1	C/W

Temperature and Voltage Derating Factors

Table 2-6 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, VCC = 1.425 V)**
For IGLOO nano V2 or V5 Devices, 1.5 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature (°C) –40°C	–20°C	0°C	25°C	70°C	85°C	100°C
1.425	0.947	0.956	0.965	0.978	1.000	1.009	1.013
1.5	0.875	0.883	0.892	0.904	0.925	0.932	0.937
1.575	0.821	0.829	0.837	0.848	0.868	0.875	0.879

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-19 on page 2-14.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-20 on page 2-14.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-20 on page 2-14. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

P_{STAT} = (PDC1 or PDC2 or PDC3) + N_{BANKS} * PDC5

N_{BANKS} is the number of I/O banks powered in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

Global Clock Contribution—P_{CLOCK}

P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + $N_{S\text{-}CELL}$ * PAC4) * F_{CLK}

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the *IGLOO nano FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the *IGLOO nano FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL}$ * (PAC5 + α_1 / 2 * PAC6) * F_{CLK}

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-14.

F_{CLK} is the global clock signal frequency.

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-41 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	STD	0.97	5.23	0.19	1.20	1.66	0.66	5.24	5.00	2.47	2.56	ns
100 µA	4 mA	STD	0.97	5.23	0.19	1.20	1.66	0.66	5.24	5.00	2.47	2.56	ns
100 µA	6 mA	STD	0.97	4.27	0.19	1.20	1.66	0.66	4.28	4.12	2.83	3.16	ns
100 µA	8 mA	STD	0.97	4.27	0.19	1.20	1.66	0.66	4.28	4.12	2.83	3.16	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-42 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	STD	0.97	3.11	0.19	1.20	1.66	0.66	3.13	2.55	2.47	2.70	ns
100 µA	4 mA	STD	0.97	3.11	0.19	1.20	1.66	0.66	3.13	2.55	2.47	2.70	ns
100 µA	6 mA	STD	0.97	2.56	0.19	1.20	1.66	0.66	2.57	2.02	2.82	3.31	ns
100 µA	8 mA	STD	0.97	2.56	0.19	1.20	1.66	0.66	2.57	2.02	2.82	3.31	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
3. *Software default selection highlighted in gray.*

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-51 • **Minimum and Maximum DC Input and Output Levels**

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL [1]	I_IH [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	17	22	10	10

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operating conditions where –0.3 < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

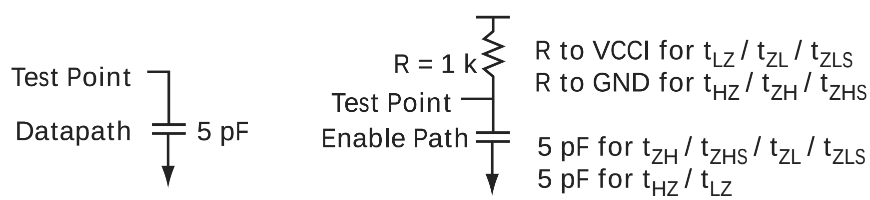

Figure 2-9 • **AC Loading**

Table 2-52 • **1.8 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.8	0.9	5

Note: **Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.*

1.2 V DC Core Voltage

Table 2-73 • Input Data Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.68	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.97	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	1.19	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	1.19	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

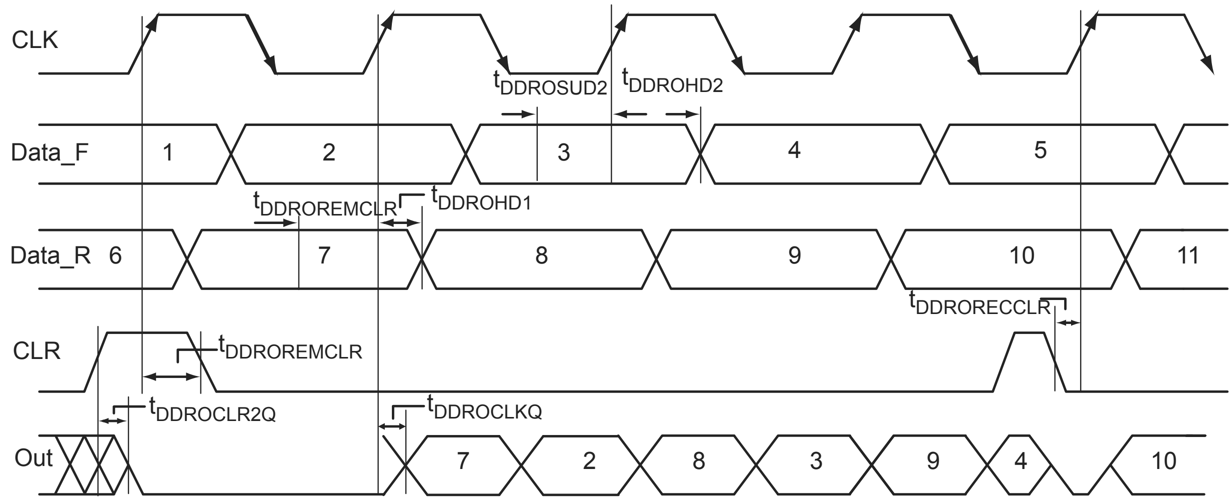

Figure 2-20 • **Output DDR Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-82 • **Output DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.07	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.67	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.67	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.38	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	250.00	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-70. Table 2-88 to Table 2-96 on page 2-68 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-88 • **AGLN010 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std. Min.[1]	Std. Max.[2]	Units
t_{RCKL}	Input Low Delay for Global Clock	1.13	1.42	ns
t_{RCKH}	Input High Delay for Global Clock	1.15	1.50	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.35	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-89 • **AGLN015 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std. Min.[1]	Std. Max.[2]	Units
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.55	ns
t_{RCKH}	Input HIgh Delay for Global Clock	1.23	1.65	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.42	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Embedded FlashROM Characteristics

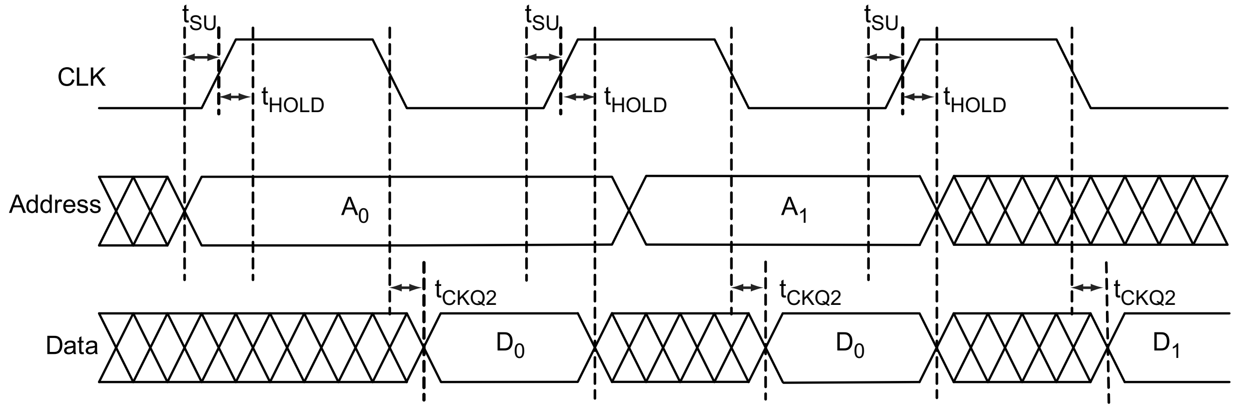

Figure 2-41 **• Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-108 **• Embedded FlashROM Access Time**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.57	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	20.90	ns
F_{MAX}	Maximum Clock Frequency	15	MHz

1.2 V DC Core Voltage

Table 2-109 **• Embedded FlashROM Access Time**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.59	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	35.74	ns
F_{MAX}	Maximum Clock Frequency	10	MHz

should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

Table 3-1 shows the Flash*Freeze pin location on the available packages for IGLOO nano devices. The Flash*Freeze pin location is independent of device (except for a PQ208 package), allowing migration to larger or smaller IGLOO nano devices while maintaining the same pin location on the board. Refer to the "Flash*Freeze Technology and Low Power Modes" chapter of the *IGLOO nano FPGA Fabric User's Guide* for more information on I/O states during Flash*Freeze mode.

Table 3-1 **• Flash*Freeze Pin Locations for IGLOO nano Devices**

Package	Flash*Freeze Pin
CS81/UC81	H2
QN48	14
QN68	18
VQ100	27
UC36	E2

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 3-2 for more information.

Table 3-2 **• Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance [1,2]
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *The TCK pin can be pulled-up or pulled-down.*
2. *The TRST pin is pulled-down.*
3. *Equivalent parallel resistance if more than one device is on the JTAG chain*

CS81	
Pin Number	AGLN060 Function
A1	GAA0/IO02RSB0
A2	GAA1/IO03RSB0
A3	GAC0/IO06RSB0
A4	IO09RSB0
A5	IO13RSB0
A6	IO18RSB0
A7	GBB0/IO21RSB0
A8	GBA1/IO24RSB0
A9	GBA2/IO25RSB0
B1	GAA2/IO95RSB1
B2	GAB0/IO04RSB0
B3	GAC1/IO07RSB0
B4	IO08RSB0
B5	IO15RSB0
B6	GBC0/IO19RSB0
B7	GBB1/IO22RSB0
B8	IO26RSB0
B9	GBB2/IO27RSB0
C1	GAB2/IO93RSB1
C2	IO94RSB1
C3	GND
C4	IO10RSB0
C5	IO17RSB0
C6	GND
C7	GBA0/IO23RSB0
C8	GBC2/IO29RSB0
C9	IO31RSB0
D1	GAC2/IO91RSB1
D2	IO92RSB1
D3	GFA2/IO80RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	GCC2/IO43RSB0
D8	GCC1/IO35RSB0
D9	GCC0/IO36RSB0
E1	GFB0/IO83RSB1
E2	GFB1/IO84RSB1
E3	GFA1/IO81RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	GCA1/IO39RSB0
E8	GCA0/IO40RSB0
E9	GCB2/IO42RSB0
F1[1]	VCCPLF
F2[1]	VCOMPLF
F3	GND
F4	GND
F5	VCCIB1
F6	GND
F7	GDA1/IO49RSB0
F8	GDC1/IO45RSB0
F9	GDC0/IO46RSB0
G1	GEA0/IO69RSB1
G2	GEC1/IO74RSB1
G3	GEB1/IO72RSB1
G4	IO63RSB1
G5	IO60RSB1
G6	IO54RSB1
G7	GDB2/IO52RSB1
G8	VJTAG
G9	TRST
H1	GEA1/IO70RSB1
H2	FF/GEB2/IO67RSB1
H3	IO65RSB1
H4	IO62RSB1
H5	IO59RSB1
H6	IO56RSB1
H7[2]	GDA2/IO51RSB1
H8	TDI
H9	TDO
J1	GEA2/IO68RSB1
J2	GEC2/IO66RSB1
J3	IO64RSB1
J4	IO61RSB1
J5	IO58RSB1
J6	IO55RSB1
J7	TCK
J8	TMS
J9	VPUMP

Notes:

1. *Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN060-CS81.*
2. *The bus hold attribute (hold previous I/O state in Flash*Freeze mode) is not supported for pin H7 in AGLN060-CS81.*

VQ100		VQ100		VQ100	
Pin Number	AGLN125Z Function	Pin Number	AGLN125Z Function	Pin Number	AGLN125Z Function
1	GND	36	IO93RSB1	71	GBB2/IO43RSB0
2	GAA2/IO67RSB1	37	VCC	72	IO42RSB0
3	IO68RSB1	38	GND	73	GBA2/IO41RSB0
4	GAB2/IO69RSB1	39	VCCIB1	74	VMV0
5	IO132RSB1	40	IO87RSB1	75	GNDQ
6	GAC2/IO131RSB1	41	IO84RSB1	76	GBA1/IO40RSB0
7	IO130RSB1	42	IO81RSB1	77	GBA0/IO39RSB0
8	IO129RSB1	43	IO75RSB1	78	GBB1/IO38RSB0
9	GND	44	GDC2/IO72RSB1	79	GBB0/IO37RSB0
10	GFB1/IO124RSB1	45	GDB2/IO71RSB1	80	GBC1/IO36RSB0
11	GFB0/IO123RSB1	46	GDA2/IO70RSB1	81	GBC0/IO35RSB0
12	VCOMPLF	47	TCK	82	IO32RSB0
13	GFA0/IO122RSB1	48	TDI	83	IO28RSB0
14	VCCPLF	49	TMS	84	IO25RSB0
15	GFA1/IO121RSB1	50	VMV1	85	IO22RSB0
16	GFA2/IO120RSB1	51	GND	86	IO19RSB0
17	VCC	52	VPUMP	87	VCCIB0
18	VCCIB1	53	NC	88	GND
19	GEC0/IO111RSB1	54	TDO	89	VCC
20	GEB1/IO110RSB1	55	TRST	90	IO15RSB0
21	GEB0/IO109RSB1	56	VJTAG	91	IO13RSB0
22	GEA1/IO108RSB1	57	GDA1/IO65RSB0	92	IO11RSB0
23	GEA0/IO107RSB1	58	GDC0/IO62RSB0	93	IO09RSB0
24	VMV1	59	GDC1/IO61RSB0	94	IO07RSB0
25	GNDQ	60	GCC2/IO59RSB0	95	GAC1/IO05RSB0
26	GEA2/IO106RSB1	61	GCB2/IO58RSB0	96	GAC0/IO04RSB0
27	FF/GEB2/IO105RSB1	62	GCA0/IO56RSB0	97	GAB1/IO03RSB0
28	GEC2/IO104RSB1	63	GCA1/IO55RSB0	98	GAB0/IO02RSB0
29	IO102RSB1	64	GCC0/IO52RSB0	99	GAA1/IO01RSB0
30	IO100RSB1	65	GCC1/IO51RSB0	100	GAA0/IO00RSB0
31	IO99RSB1	66	VCCIB0		
32	IO97RSB1	67	GND		
33	IO96RSB1	68	VCC		
34	IO95RSB1	69	IO47RSB0		
35	IO94RSB1	70	GBC2/IO45RSB0		

Revision / Version	Changes	Page
Revision 9 (Mar2010) Product Brief Advance v0.9 Packaging Advance v0.8	All product tables and pin tables were updated to show clearly that AGLN030 is available only in the Z feature grade at this time. The nano-Z feature grade devices are designated with a Z at the end of the part number.	N/A
Revision 8 (Jan 2009)	The "Reprogrammable Flash Technology" section was revised to add "250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance".	I
Product Brief Advance v0.8	The note for AGLN030 in the "IGLOO nano Devices" table and "I/Os Per Package" table was revised to remove the statement regarding package compatibility with lower density nano devices.	II, II
	The "I/Os with Advanced I/O Standards" section was revised to add definitions for hot-swap and cold-sparing.	1-8
Packaging Advance v0.7	The "UC81", "CS81", "QN48", and "QN68" pin tables for AGLN030 are new.	4-5, 4-8, 4-17, 4-21
	The "CS81"pin table for AGLN060 is new.	4-9
	The "CS81" and "VQ100" pin tables for AGLN060Z are new.	4-10, 4-25
	The "CS81" and "VQ100" pin tables for AGLN125Z are new.	4-12, 4-27
	The "CS81" and "VQ100" pin tables for AGLN250Z is new.	4-14, 4-29
Revision 7 (Apr 2009) Product Brief Advance v0.7 DC and Switching Characteristics Advance v0.3	The –F speed grade is no longer offered for IGLOO nano devices and was removed from the datasheet.	N/A
Revision 6 (Mar 2009) Packaging Advance v0.6	The "VQ100" pin table for AGLN030 is new.	4-23
Revision 5 (Feb 2009) Packaging Advance v0.5	The "100-Pin QFN" section was removed.	N/A
Revision 4 (Feb 2009)	The QN100 package was removed for all devices.	N/A
Product Brief Advance v0.6	"IGLOO nano Devices" table was updated to change the maximum user I/Os for AGLN030 from 81 to 77.	II
	The "Device Marking" section is new.	V
Revision 3 (Feb 2009) Product Brief Advance v0.5	The following table note was removed from "IGLOO nano Devices" table: "Six chip (main) and three quadrant global networks are available for AGLN060 and above."	II
	The CS81 package was added for AGLN250 in the "IGLOO nano Products Available in the Z Feature Grade" table.	VI
Packaging Advance v0.4	The "UC81" and "CS81" pin tables for AGLN020 are new.	4-4, 4-7
	The "CS81" pin table for AGLN250 is new.	4-13

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "IGLOO nano Device Status" table on page III, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

Safety Critical, Life Support, and High-Reliability Applications Policy

The Microsemi products described in this advance status document may not have completed Microsemi's qualification process. Microsemi may amend or enhance products during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any Microsemi product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult Microsemi's Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the Microsemi SoC Products Group's products is at http://www.microsemi.com/socdocuments/ORT_Report.pdf. Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local Microsemi sales office for additional reliability information.