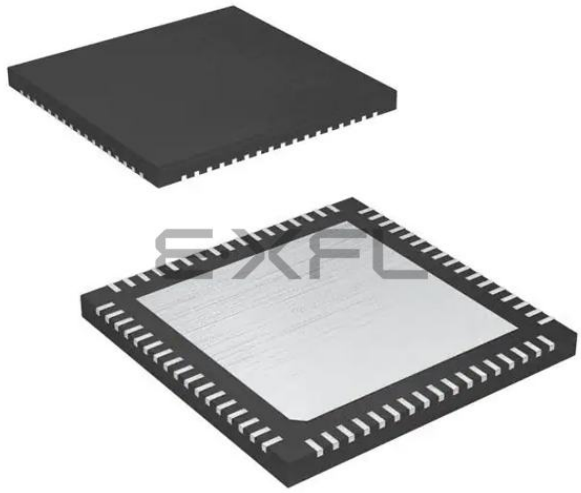


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	768
Total RAM Bits	-
Number of I/O	49
Number of Gates	30000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agln030v5-zqng68i

IGLOO nano Products Available in the Z Feature Grade

IGLOO nano-Z Devices	AGLN030Z*	AGLN060Z*	AGLN125Z*	AGLN250Z*
	QN48	–	–	–
	QN68	–	–	–
	UC81	–	–	–
	CS81	CS81	CS81	CS81
Packages	VQ100	VQ100	VQ100	VQ100

*Note: *Not recommended for new designs.*

Temperature Grade Offerings

Package	AGLN010	AGLN015*	AGLN020	AGLN030Z*	AGLN060 AGLN060Z*	AGLN125 AGLN125Z*	AGLN250 AGLN250Z*
UC36	C, I	–	–	–	–	–	–
QN48	C, I	–	–	C, I	–	–	–
QN68	–	C, I	C, I	C, I	–	–	–
UC81	–	–	C, I	C, I	–	–	–
CS81	–	–	C, I	C, I	C, I	C, I	C, I
VQ100	–	–	–	C, I	C, I	C, I	C, I

*Note: * Not recommended for new designs.*

C = Enhanced Commercial temperature range: –20°C to +85°C junction temperature
I = Industrial temperature range: –40°C to +100°C junction temperature

Contact your local Microsemi representative for device availability: http://www.microsemi.com/soc/contact/default.aspx.

The inputs of the six CCC blocks are accessible from the FPGA core or from dedicated connections to the CCC block, which are located near the CCC.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 µs (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz / f_{OUT_CCC} (for PLL only)

Global Clocking

IGLOO nano devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

I/Os with Advanced I/O Standards

IGLOO nano FPGAs feature a flexible I/O structure, supporting a range of voltages (1.2 V, 1.2 V wide range, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V).

The I/Os are organized into banks with two, three, or four banks per device. The configuration of these banks determines the I/O standards supported.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of various single-data-rate applications for all versions of nano devices and double-data-rate applications for the AGLN060, AGLN125, and AGLN250 devices.

IGLOO nano devices support LVTTL and LVCMOS I/O standards, are hot-swappable, and support cold-sparing and Schmitt trigger.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Wide Range I/O Support

IGLOO nano devices support JEDEC-defined wide range I/O operation. IGLOO nano devices support both the JESD8-B specification, covering both 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Table 2-2 • **Recommended Operating Conditions [1]**

Symbol	Parameter		Extended Commercial	Industrial	Units
T_J	Junction temperature		–20 to + 85[2]	–40 to +100[2]	°C
VCC	1.5 V DC core supply voltage[3]		1.425 to 1.575	1.425 to 1.575	V
	1.2 V–1.5 V wide range core voltage[4,5]		1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP [6]	Programming voltage	Programming mode	3.15 to 3.45	3.15 to 3.45	V
		Operation	0 to 3.6	0 to 3.6	V
VCCPLL[7]	Analog power supply (PLL)	1.5 V DC core supply voltage[3]	1.425 to 1.575	1.425 to 1.575	V
		1.2 V–1.5 V wide range core supply voltage[4]	1.14 to 1.575	1.14 to 1.575	V
VCCI and VMV [8,9]	1.2 V DC supply voltage [4]		1.14 to 1.26	1.14 to 1.26	V
	1.2 V DC wide range supply voltage [4]		1.14 to 1.575	1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	3.3 V DC wide range supply voltage [10]		2.7 to 3.6	2.7 to 3.6	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the Libero Online Help.*
3. *For IGLOO® nano V5 devices*
4. *For IGLOO nano V2 devices only, operating at VCCI ≥ VCC*
5. *IGLOO nano V5 devices can be programmed with the VCC core voltage at 1.5 V only. IGLOO nano V2 devices can be programmed with the VCC core voltage at 1.2 V (with FlashPro4 only) or 1.5 V. If you are using FlashPro3 and want to do in-system programming using 1.2 V, please contact the factory.*
6. *V_{PUMP} can be left floating during operation (not programming mode).*
7. *VCCPLL pins should be tied to VCC pins. See the "Pin Descriptions" chapter for further information.*
8. *VMV pins must be connected to the corresponding VCCI pins. See the Pin Descriptions chapter of the IGLOO nano FPGA Fabric User's Guide for further information.*
9. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-21 on page 2-19. VCCI should be at the same voltage within a given I/O bank.*
10. *3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.*

Table 2-3 • **Flash Programming Limits – Retention, Storage, and Operating Temperature[1]**

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

Table 2-10 • **Quiescent Supply Current (IDD) Characteristics, IGLOO nano Sleep Mode***

	Core Voltage	AGLN010	AGLN015	AGLN020	AGLN060	AGLN125	AGLN250	Units
VCCI= 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	µA
VCCI = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	µA
VCCI = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	µA
VCCI = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	µA
VCCI = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	µA

Note: $*I_{DD} = N_{BANKS} * I_{CCI}$.

Table 2-11 • **Quiescent Supply Current (IDD) Characteristics, IGLOO nano Shutdown Mode**

	Core Voltage	AGLN010	AGLN015	AGLN020	AGLN060	AGLN125	AGLN250	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	0	0	0	0	µA

Table 2-12 • **Quiescent Supply Current (IDD), No IGLOO nano Flash*Freeze Mode[1]**

	Core Voltage	AGLN010	AGLN015	AGLN020	AGLN060	AGLN125	AGLN250	Units
ICCA Current[2]								
Typical (25°C)	1.2 V	3.7	5	5	10	13	18	µA
	1.5 V	8	14	14	20	28	44	µA
ICCI or IJTAG Current								
VCCI / VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	µA
VCCI / VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	µA
VCCI / VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	µA
VCCI / VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	µA
VCCI / VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	µA

Notes:

1. *$IDD = N_{BANKS} * ICCI + ICCA$. JTAG counts as one bank when powered.*
2. *Includes VCC, VCCPLL, and VPUMP currents.*

Power per I/O Pin

Table 2-13 • **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to IGLOO nano I/O Banks**

	VCCI (V)	Dynamic Power PAC9 (µW/MHz) [1]
Single-Ended		
3.3 V LVTTL / 3.3 V LVCMOS	3.3	16.38
3.3 V LVTTL / 3.3 V LVCMOS – Schmitt Trigger	3.3	18.89
3.3 V LVCMOS Wide Range[2]	3.3	16.38
3.3 V LVCMOS Wide Range – Schmitt Trigger	3.3	18.89
2.5 V LVCMOS	2.5	4.71
2.5 V LVCMOS – Schmitt Trigger	2.5	6.13
1.8 V LVCMOS	1.8	1.64
1.8 V LVCMOS – Schmitt Trigger	1.8	1.79
1.5 V LVCMOS (JESD8-11)	1.5	0.97
1.5 V LVCMOS (JESD8-11) – Schmitt Trigger	1.5	0.96
1.2 V LVCMOS[3]	1.2	0.57
1.2 V LVCMOS – Schmitt Trigger[3]	1.2	0.52
1.2 V LVCMOS Wide Range[3]	1.2	0.57
1.2 V LVCMOS Wide Range – Schmitt Trigger[3]	1.2	0.52

Notes:

1. *PAC9 is the total dynamic power measured on V_{CCI}.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
3. *Applicable to IGLOO nano V2 devices operating at VCCI ≥ VCC.*

Table 2-14 • **Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] Applicable to IGLOO nano I/O Banks**

	C_{LOAD} (pF)	VCCI (V)	Dynamic Power PAC10 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	107.98
3.3 V LVCMOS Wide Range[3]	5	3.3	107.98
2.5 V LVCMOS	5	2.5	61.24
1.8 V LVCMOS	5	1.8	31.28
1.5 V LVCMOS (JESD8-11)	5	1.5	21.50
1.2 V LVCMOS[4]	5	1.2	15.22

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PAC10 is the total dynamic power measured on VCCI.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
4. *Applicable for IGLOO nano V2 devices operating at VCCI ≥ VCC.*

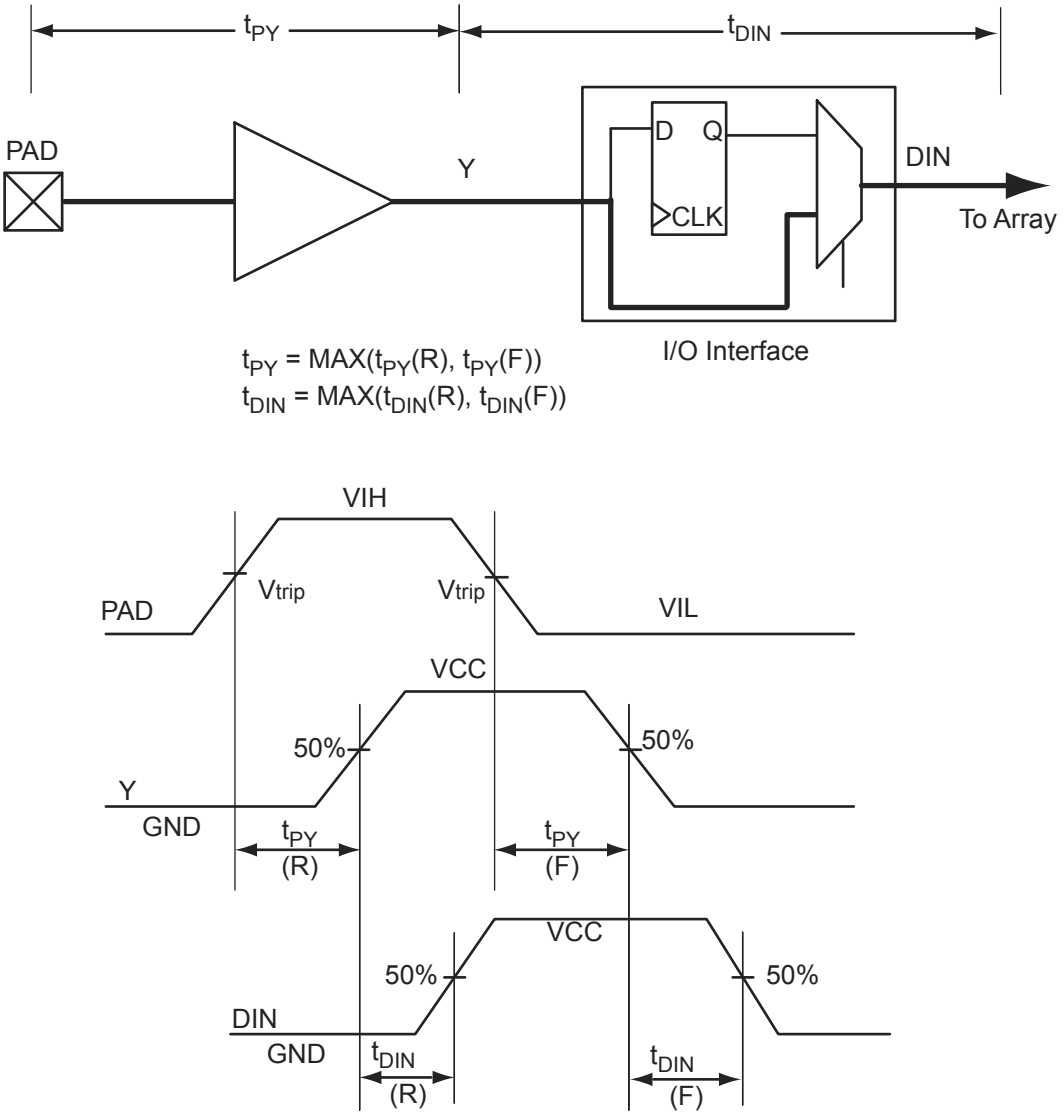


Figure 2-4 • **Input Buffer Timing Model and Delays (example)**

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 2-34 • **Minimum and Maximum DC Input and Output Levels**

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL [1]	IIH [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operating conditions where –0.3 < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

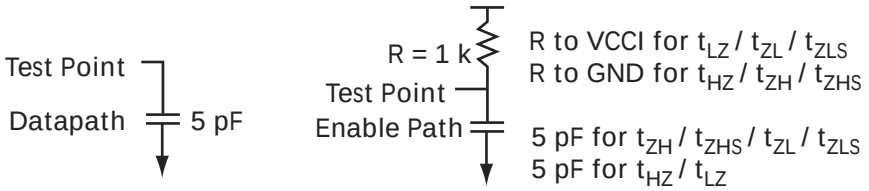


Figure 2-7 • **AC Loading**

Table 2-35 • **3.3 V LVTTL/LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	1.4	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.*

Fully Registered I/O Buffers with Asynchronous Clear

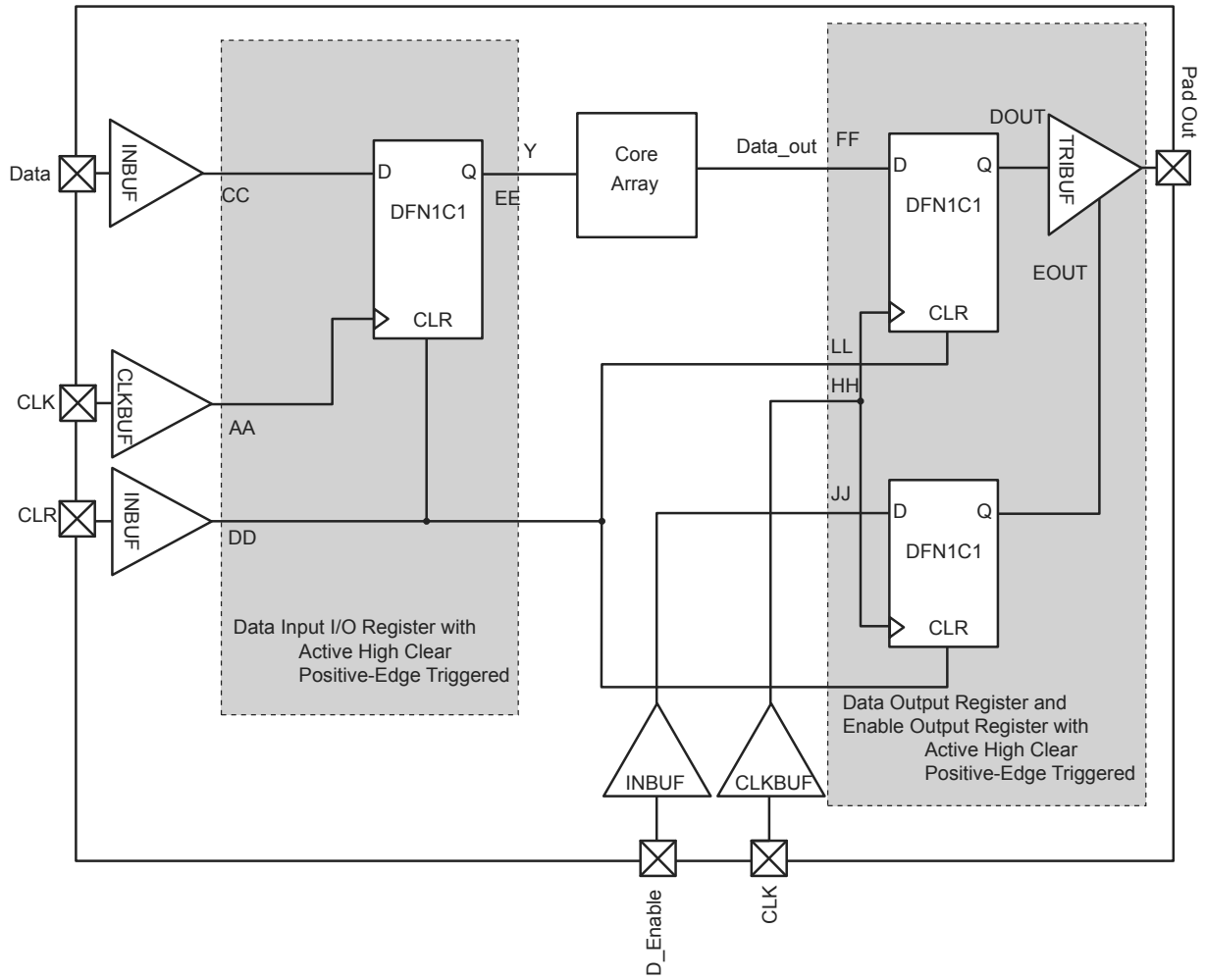


Figure 2-13 • **Timing Model of the Registered I/O Buffers with Asynchronous Clear**

1.2 V DC Core Voltage

Table 2-75 • Output Data Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	1.52	ns
t_{OSUD}	Data Setup Time for the Output Data Register	1.15	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.96	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.96	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

***Table 2-101* • IGLOO nano CCC/PLL Specification**
For IGLOO nano V2 Devices, 1.2 V DC Core Supply Voltage

Parameter		Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}		1.5		160	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}		0.75		160	MHz
Delay Increments in Programmable Delay Blocks [1, 2]			580[3]		ps
Number of Programmable Values in Each Programmable Delay Block				32	
Serial Clock (SCLK) for Dynamic PLL [4,9]				60	
Input Cycle-to-Cycle Jitter (peak magnitude)				0.25	ns
Acquisition Time					
	LockControl = 0			300	µs
	LockControl = 1			6.0	ms
Tracking Jitter [5]					
	LockControl = 0			4	ns
	LockControl = 1			3	ns
Output Duty Cycle		48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]		2.3		20.86	ns
Delay Range in Block: Programmable Delay 2 [1, 2]		0.025		20.86	ns
Delay Range in Block: Fixed Delay [1, 2]			5.7		ns
VCO Output Peak-to-Peak Period Jitter F_{CCC_OUT} [6]		Max Peak-to-Peak Period Jitter [6,7,8]			
	SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16	
0.75 MHz to 50MHz	0.50	1.20	2.00	3.00	%
50 MHz to 100 MHz	2.50	5.00	7.00	15.00	%

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for deratings.*
2. *T_J = 25°C, V_{CC} = 1.2 V.*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
4. *Maximum value obtained for a STD speed grade device in Worst-Case Commercial conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for derating values.*
5. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
6. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT, regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, no matter what the settings are for the output divider.*
7. *Measurements done with LVTTL 3.3 V 8 mA I/O drive strength and high slew rate. VCC/VCCPLL = 1.14 V, VCCI = 3.3 V, VQ/PQ/TQ type of packages, 20 pF load.*
8. *SSOs are outputs that are synchronous to a single clock domain and have their clock-to-out times within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO nano FPGA Fabric User's Guide.*
9. *The AGLN010, AGLN015, and AGLN020 devices do not support PLLs.*

Timing Waveforms

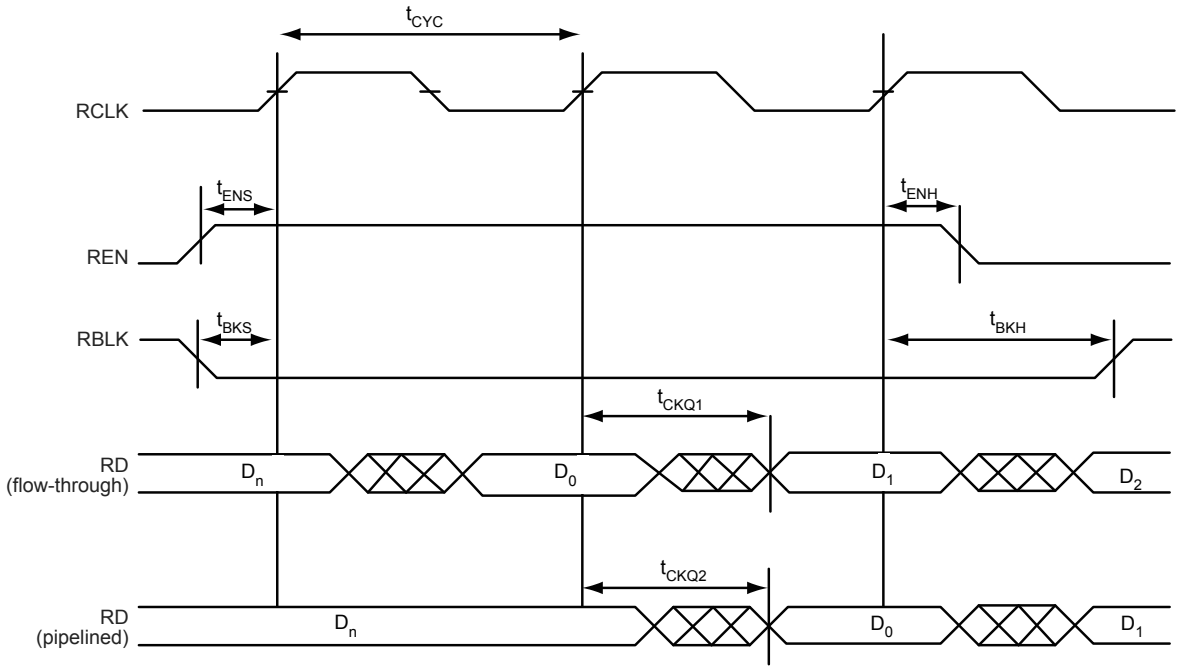


Figure 2-34 • **FIFO Read**

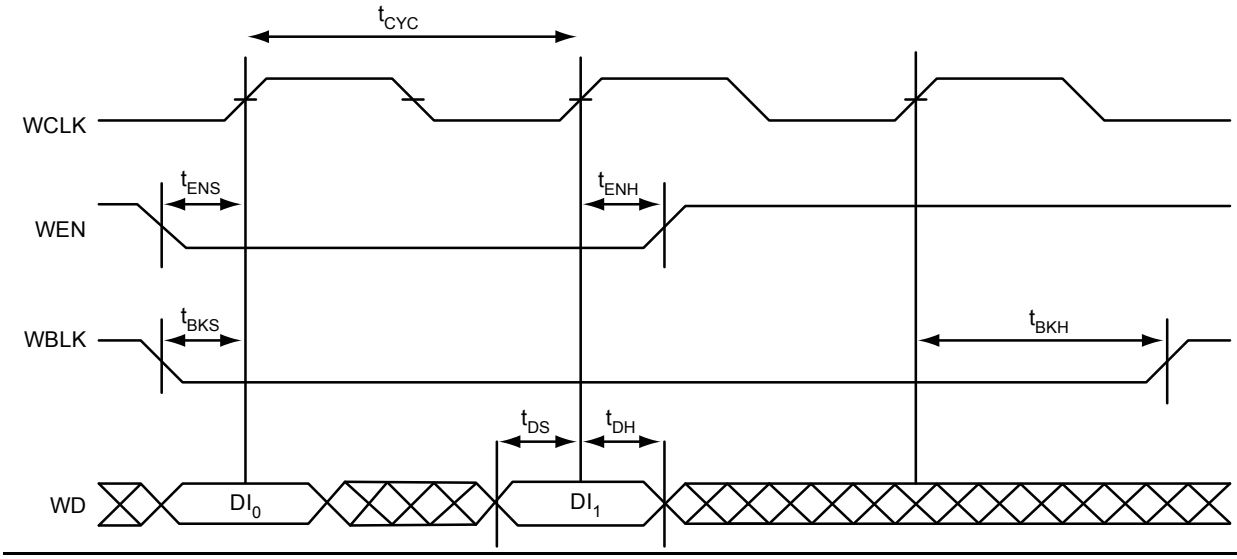


Figure 2-35 • **FIFO Write**

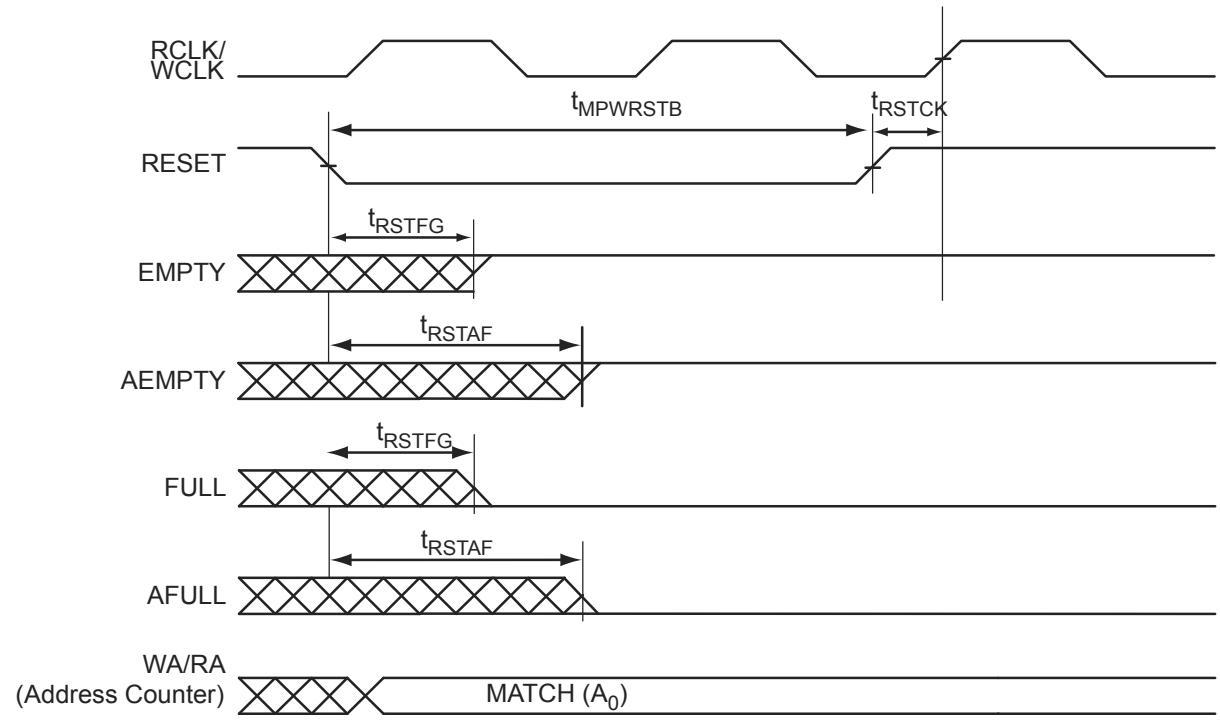


Figure 2-36 • **FIFO Reset**

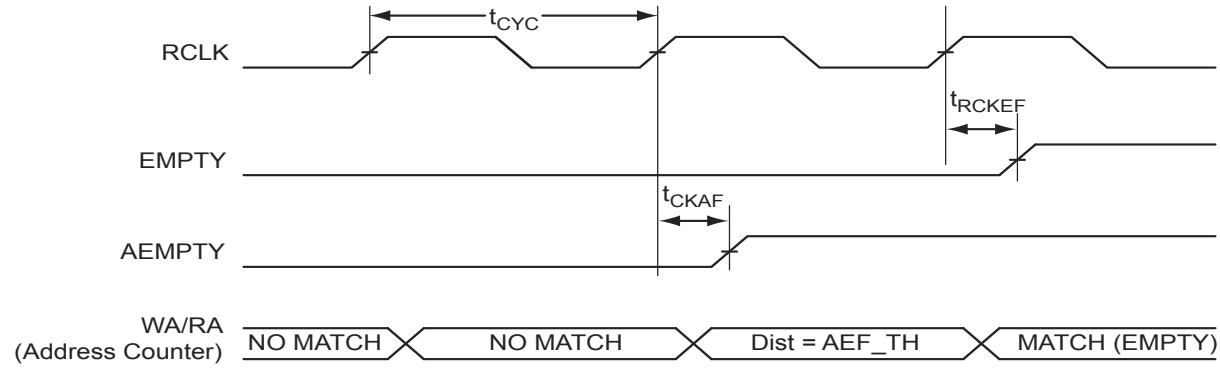
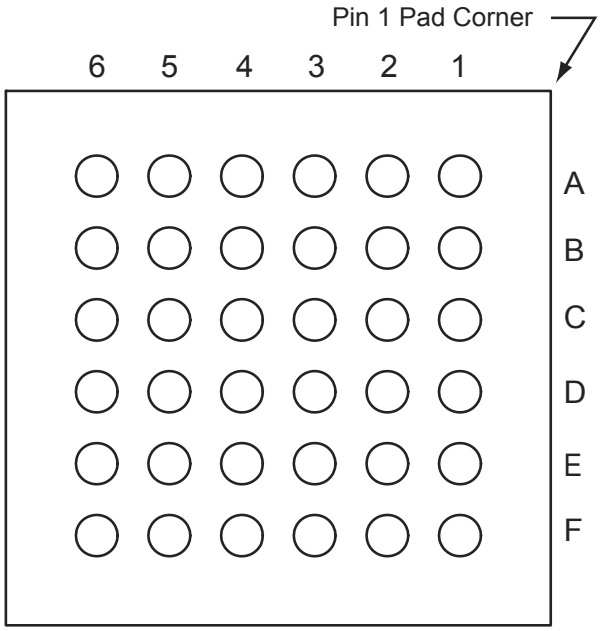


Figure 2-37 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

4 – Package Pin Assignments

UC36



Note: This is the bottom view of the package.

Note

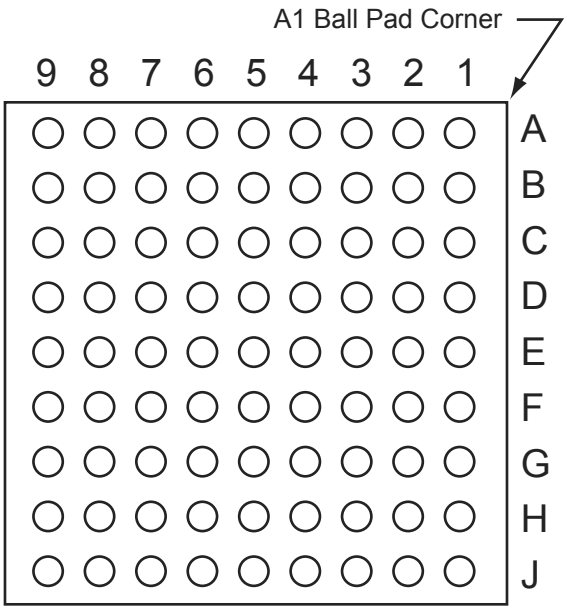
For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

UC81	
Pin Number	AGLN030Z Function
A1	IO00RSB0
A2	IO02RSB0
A3	IO06RSB0
A4	IO11RSB0
A5	IO16RSB0
A6	IO19RSB0
A7	IO22RSB0
A8	IO24RSB0
A9	IO26RSB0
B1	IO81RSB1
B2	IO04RSB0
B3	IO10RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO21RSB0
B8	IO28RSB0
B9	IO25RSB0
C1	IO79RSB1
C2	IO80RSB1
C3	IO08RSB0
C4	IO12RSB0
C5	IO17RSB0
C6	IO14RSB0
C7	IO18RSB0
C8	IO29RSB0
C9	IO27RSB0
D1	IO74RSB1
D2	IO76RSB1
D3	IO77RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	IO23RSB0
D8	IO31RSB0

UC81	
Pin Number	AGLN030Z Function
D9	IO30RSB0
E1	GEB0/IO71RSB1
E2	GEA0/IO72RSB1
E3	GEC0/IO73RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	GDC0/IO32RSB0
E8	GDA0/IO33RSB0
E9	GDB0/IO34RSB0
F1	IO68RSB1
F2	IO67RSB1
F3	IO64RSB1
F4	GND
F5	VCCIB1
F6	IO47RSB1
F7	IO36RSB0
F8	IO38RSB0
F9	IO40RSB0
G1	IO65RSB1
G2	IO66RSB1
G3	IO57RSB1
G4	IO53RSB1
G5	IO49RSB1
G6	IO45RSB1
G7	IO46RSB1
G8	VJTAG
G9	TRST
H1	IO62RSB1
H2	FF/IO60RSB1
H3	IO58RSB1
H4	IO54RSB1
H5	IO48RSB1
H6	IO43RSB1
H7	IO42RSB1

UC81	
Pin Number	AGLN030Z Function
H8	TDI
H9	TDO
J1	IO63RSB1
J2	IO61RSB1
J3	IO59RSB1
J4	IO56RSB1
J5	IO52RSB1
J6	IO44RSB1
J7	TCK
J8	TMS
J9	VPUMP

CS81



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

CS81	
Pin Number	**AGLN060 Function**
A1	GAA0/IO02RSB0
A2	GAA1/IO03RSB0
A3	GAC0/IO06RSB0
A4	IO09RSB0
A5	IO13RSB0
A6	IO18RSB0
A7	GBB0/IO21RSB0
A8	GBA1/IO24RSB0
A9	GBA2/IO25RSB0
B1	GAA2/IO95RSB1
B2	GAB0/IO04RSB0
B3	GAC1/IO07RSB0
B4	IO08RSB0
B5	IO15RSB0
B6	GBC0/IO19RSB0
B7	GBB1/IO22RSB0
B8	IO26RSB0
B9	GBB2/IO27RSB0
C1	GAB2/IO93RSB1
C2	IO94RSB1
C3	GND
C4	IO10RSB0
C5	IO17RSB0
C6	GND
C7	GBA0/IO23RSB0
C8	GBC2/IO29RSB0
C9	IO31RSB0
D1	GAC2/IO91RSB1
D2	IO92RSB1
D3	GFA2/IO80RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	GCC2/IO43RSB0

CS81	
Pin Number	**AGLN060 Function**
D8	GCC1/IO35RSB0
D9	GCC0/IO36RSB0
E1	GFB0/IO83RSB1
E2	GFB1/IO84RSB1
E3	GFA1/IO81RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	GCA1/IO39RSB0
E8	GCA0/IO40RSB0
E9	GCB2/IO42RSB0
F1[1]	VCCPLF
F2[1]	VCOMPLF
F3	GND
F4	GND
F5	VCCIB1
F6	GND
F7	GDA1/IO49RSB0
F8	GDC1/IO45RSB0
F9	GDC0/IO46RSB0
G1	GEA0/IO69RSB1
G2	GEC1/IO74RSB1
G3	GEB1/IO72RSB1
G4	IO63RSB1
G5	IO60RSB1
G6	IO54RSB1
G7	GDB2/IO52RSB1
G8	VJTAG
G9	TRST
H1	GEA1/IO70RSB1
H2	FF/GEB2/IO67RSB1
H3	IO65RSB1
H4	IO62RSB1
H5	IO59RSB1

CS81	
Pin Number	**AGLN060 Function**
H6	IO56RSB1
H7[2]	GDA2/IO51RSB1
H8	TDI
H9	TDO
J1	GEA2/IO68RSB1
J2	GEC2/IO66RSB1
J3	IO64RSB1
J4	IO61RSB1
J5	IO58RSB1
J6	IO55RSB1
J7	TCK
J8	TMS
J9	VPUMP

Notes:

1. *Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN060-CS81.*
2. *The bus hold attribute (hold previous I/O state in Flash*Freeze mode) is not supported for pin H7 in AGLN060-CS81.*

CS81	
Pin Number	**AGLN250Z Function**
A1	GAA0/IO00RSB0
A2	GAA1/IO01RSB0
A3	GAC0/IO04RSB0
A4	IO07RSB0
A5	IO09RSB0
A6	IO12RSB0
A7	GBB0/IO16RSB0
A8	GBA1/IO19RSB0
A9	GBA2/IO20RSB1
B1	GAA2/IO67RSB3
B2	GAB0/IO02RSB0
B3	GAC1/IO05RSB0
B4	IO06RSB0
B5	IO10RSB0
B6	GBC0/IO14RSB0
B7	GBB1/IO17RSB0
B8	IO21RSB1
B9	GBB2/IO22RSB1
C1	GAB2/IO65RSB3
C2	IO66RSB3
C3	GND
C4	IO08RSB0
C5	IO11RSB0
C6	GND
C7	GBA0/IO18RSB0
C8	GBC2/IO23RSB1
C9	IO24RSB1
D1	GAC2/IO63RSB3
D2	IO64RSB3
D3	GFA2/IO56RSB3
D4	VCC
D5	VCCIB0
D6	GND
D7	IO30RSB1
D8	GCC1/IO25RSB1
D9	GCC0/IO26RSB1

CS81	
Pin Number	**AGLN250Z Function**
E1	GFB0/IO59RSB3
E2	GFB1/IO60RSB3
E3	GFA1/IO58RSB3
E4	VCCIB3
E5	VCC
E6	VCCIB1
E7	GCA0/IO28RSB1
E8	GCA1/IO27RSB1
E9	GCB2/IO29RSB1
F1*	VCCPLF
F2*	VCOMPLF
F3	GND
F4	GND
F5	VCCIB2
F6	GND
F7	GDA1/IO33RSB1
F8	GDC1/IO31RSB1
F9	GDC0/IO32RSB1
G1	GEA0/IO51RSB3
G2	GEC1/IO54RSB3
G3	GEC0/IO53RSB3
G4	IO45RSB2
G5	IO42RSB2
G6	IO37RSB2
G7	GDB2/IO35RSB2
G8	VJTAG
G9	TRST
H1	GEA1/IO52RSB3
H2	FF/GEB2/IO49RSB2
H3	IO47RSB2
H4	IO44RSB2
H5	IO41RSB2
H6	IO39RSB2
H7	GDA2/IO34RSB2
H8	TDI
H9	TDO

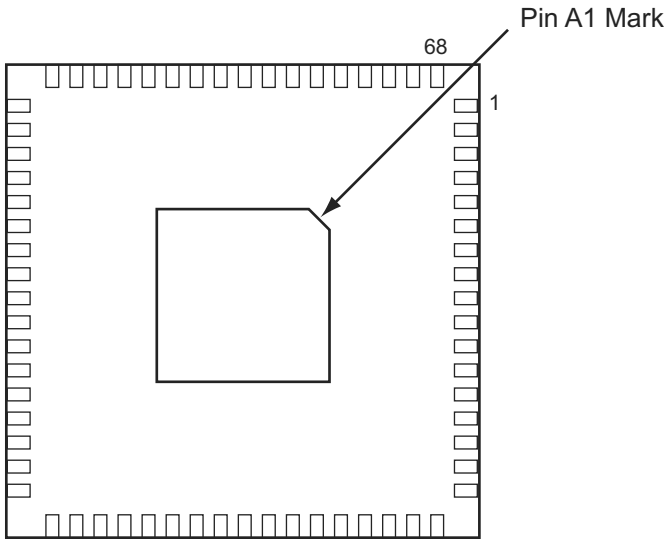
CS81	
Pin Number	**AGLN250Z Function**
J1	GEA2/IO50RSB2
J2	GEC2/IO48RSB2
J3	IO46RSB2
J4	IO43RSB2
J5	IO40RSB2
J6	IO38RSB2
J7	TCK
J8	TMS
J9	VPUMP

*Note: * Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN250Z-CS81.*

QN48	
Pin Number	**AGLN010 Function**
1	GEC0/IO37RSB1
2	IO36RSB1
3	GEA0/IO34RSB1
4	IO22RSB1
5	GND
6	VCCIB1
7	IO24RSB1
8	IO33RSB1
9	IO26RSB1
10	IO32RSB1
11	IO27RSB1
12	IO29RSB1
13	IO30RSB1
14	FF/IO31RSB1
15	IO28RSB1
16	IO25RSB1
17	IO23RSB1
18	VCC
19	VCCIB1
20	IO17RSB1
21	IO14RSB1
22	TCK
23	TDI
24	TMS
25	VPUMP
26	TDO
27	TRST
28	VJTAG
29	IO11RSB0
30	IO10RSB0
31	IO09RSB0
32	IO08RSB0
33	VCCIB0
34	GND
35	VCC

QN48	
Pin Number	**AGLN010 Function**
36	IO07RSB0
37	IO06RSB0
38	GDA0/IO05RSB0
39	IO03RSB0
40	GDC0/IO01RSB0
41	IO12RSB1
42	IO13RSB1
43	IO15RSB1
44	IO16RSB1
45	IO18RSB1
46	IO19RSB1
47	IO20RSB1
48	IO21RSB1

QN68



Notes:

1. *This is the bottom view of the package.*
2. *The die attach paddle of the package is tied to ground (GND).*

Note

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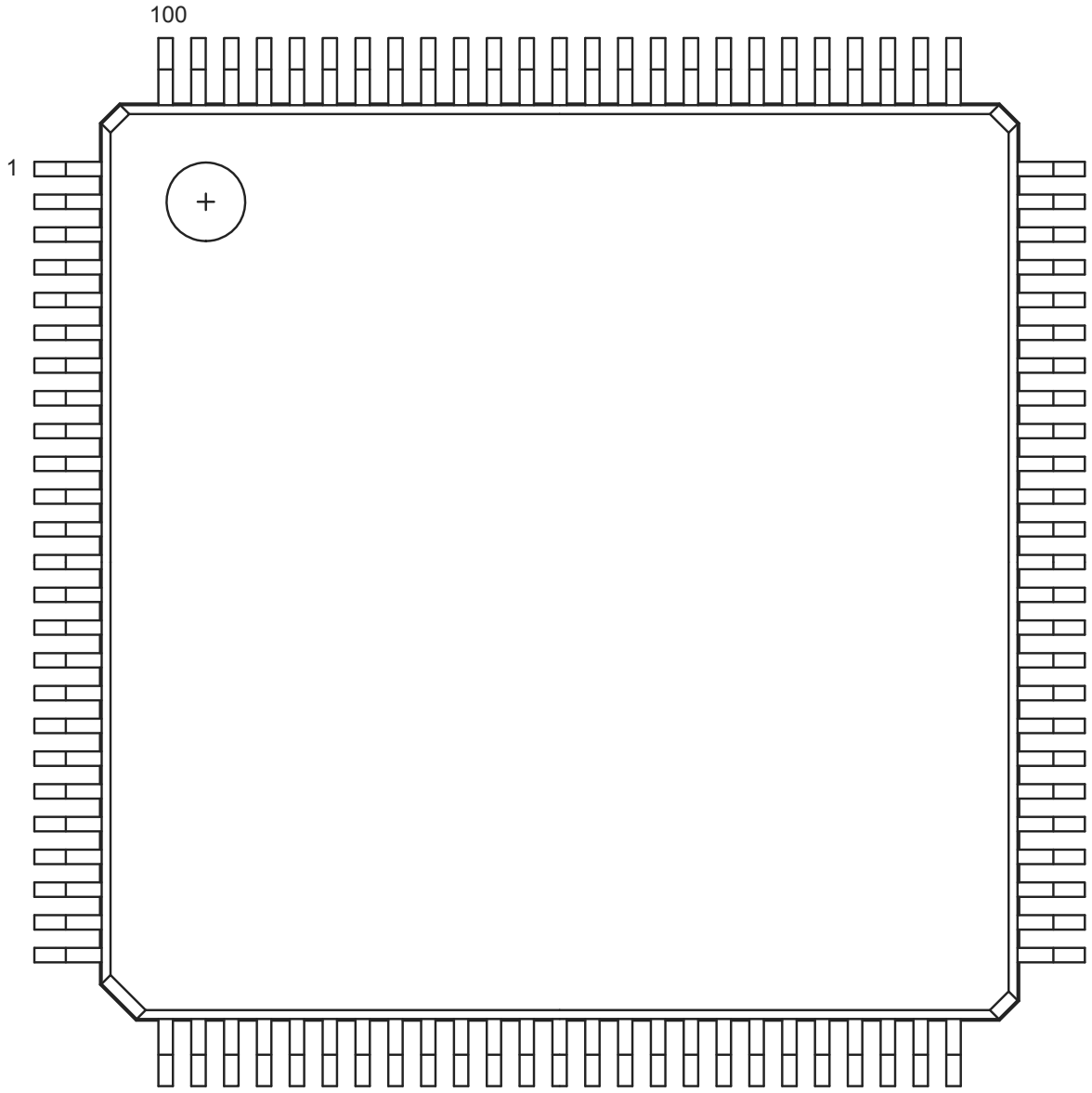
VQ100



Note: This is the top view of the package.

Note

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